Creative Compensation Enables Tiny Amplifier to Drive 200-mW Loads

By Mark Reisiger

Overview

Many applications need an amplifier that delivers a moderate amount of power to a load while maintaining good dc precision, with the size of the load determining the type of circuit required. A precision op amp can drive loads requiring less than 50 mW, and a compound amplifier with a precision-op-amp input stage and discrete-power-transistor output stage can be constructed to drive loads that require watts. However, no good solution exists in the middle of the power range. Either the op amp can't drive the load, or the circuit becomes large, complex, and expensive.

Recently this dilemma arose in the design of a Wheatstone bridge driver. The excitation voltage directly affects the offset and span, so dc precision is required. In this case, the application can tolerate less than 1 mV of error between the source voltage and the bridge. Operating with 7-V to 15-V power supplies, the circuit must drive the bridge with unity gain from 100 mV to 5 V.

To further complicate the problem, a variety of different bridge resistances can be used. Strain gages, for example, have standard impedances of 120 Ω or 350 Ω. With a 120-Ω bridge, the amplifier must source 42 mA to maintain a 5-V bridge drive. In addition, the circuit must be able to drive up to 10 nF. This accounts for both the cable and the bridge decoupling capacitor.

Amplifier Selection

The first step in designing this circuit is selecting an amplifier capable of driving the load. Its dropout voltage (V_{OH}) must be less than the available headroom for the circuit at the required load current. For this design, the minimum power supply is 7 V and the maximum output is 5 V. Providing 250 mV for margin, the available headroom ($V_{DD} - V_{OUT}$) is 1.75 V. The required load current is 42 mA.

The ADA4661-2 precision, dual op amp has rail-to-rail inputs and outputs. Its large output stage is capable of driving significant amounts of current. The data sheet specifies a 900-mV dropout voltage when sourcing 40 mA, so it should easily meet the 1.75-V headroom requirement.

While the dropout voltage limits circuit operation with low-voltage power supplies, power dissipation will limit operation with high-voltage power supplies. The die temperature rise can be calculated to determine the maximum safe operating temperature. The MSOP package simplifies prototyping, but the LFCSP package has much better thermal performance, so it should be used if possible. The thermal resistance (θ_{JA}) is 142°C/W for the MSOP and 83.5°C/W for the LFCSP. The maximum die temperature rise is calculated by multiplying the thermal resistance by the maximum power dissipation. With a 15-V supply and a 5-V output, the headroom is 10 V. The maximum current is 42 mA, which results in 420-mW power dissipation. The resulting die temperature rise (60°C for the MSOP or 35°C for the LFCSP) limits the maximum ambient temperature to 65°C for the MSOP or 90°C for the LFCSP.

The thermal performance of the die and package combination is also critical to maintaining an accurate bridge excitation voltage. Unfortunately, the performance of some op amps is severely degraded when driving large output currents. Power dissipation in the output stage causes large thermal gradients across the die, unbalancing the matched transistors and trim circuitry. The ADA4661-2 was designed to drive significant power while rejecting these thermal gradients.

Feedback Loop Stabilization

Meeting the load-capacitance specification is tricky, as most op amps can't drive 10 nF without external compensation. One classic technique for driving large capacitive loads is to use the multiple feedback topology, as shown in Figure 1, where isolation resistor R_{ISO} shields the amplifier output from load capacitor C_{LOAD}. The dc precision is maintained by feeding back output-signal V_{OUT} through feedback-resistor R_F. The loop stability is maintained by feeding back the amplifier output through capacitor C_F.

For this circuit to be effective, R_{ISO} must be large enough such that the total load impedance looks purely resistive at the amplifier's unity-gain frequency. This is difficult because of the IR drop across this resistor. The maximum size of R_{ISO} can be determined by allocating the remaining voltage headroom in the worst-case conditions. A 6.75-V power supply with a 5-V output allows for 1.75 V of total dropout. The amplifier V_{OH} takes up 900 mV of this, leaving 850 mV left to drop across the resistor. This limits the maximum value of R_{ISO} to 20 Ω. A 2-nF load capacitance places a pole at 4 MHz, which is the unity-gain crossover frequency of this amplifier. Clearly, multiple feedback will not meet the requirements.

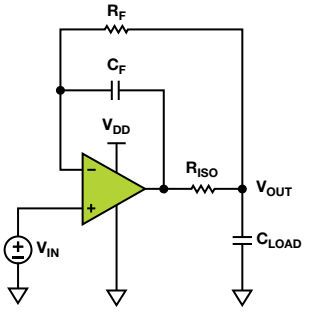

Figure 1. Multiple feedback topology.

A different technique for stabilizing a heavily loaded buffer is to use a hybrid-unity follower topology, as shown in Figure 2. Rather than trying to move the load-capacitance pole, this approach forces the feedback loop to crossover at a lower frequency by reducing the feedback factor. Stability is achieved by forcing the loop to crossover before the phase shift becomes excessive due to the load pole.

The feedback factor is the inverse of the noise gain, so one may conclude that this approach abandons the unity-gain signal path. This would be true if this were a traditional inverting or noninverting configuration, but a closer inspection of the schematic reveals that both inputs are driven. An easy way to think about this circuit is the superposition of an inverting gain of $-R_F/R_S$ and a noninverting gain of $(1 + R_F/R_S)$. The result is a circuit that operates with a signal gain of +1 and a noise gain of $(R_S + R_F)/R_S$. Independent control over the feedback factor and signal gain allows this circuit to stabilize any size load at the expense of circuit bandwidth.

The hybrid unity follower circuit has several drawbacks, however. The first problem is that the noise gain is high for all frequencies, so dc errors such as offset voltage (V_{OS}) are multiplied by the noise gain. This makes achieving the dc specifications extremely challenging. The second drawback requires some knowledge of the internal operation of the amplifier. This amplifier has a three-stage architecture with nested Miller compensation. The output stage has its own fixed internal feedback. This makes it possible for the external feedback loop to be stable while the output stage feedback loop is unstable.

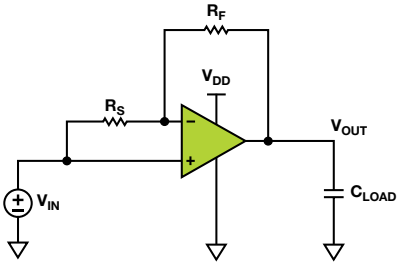

Figure 2. Hybrid-unity follower topology.

By combining the operating principles of both circuits, both issues can be overcome, as shown in Figure 3. Multiple feedback separates low-frequency and high-frequency feedback paths, adding enough capacitive load isolation to minimize output-stage stability problems. The low-frequency feedback is driven from the bridge voltage through feedback-resistor R_F. The high-frequency feedback is driven from the amplifier output through feedback-capacitor C_F.

The circuit also behaves like the hybrid unity follower at high frequency. The high-frequency noise gain, determined by the impedance of the capacitors, is equal to $(C_S + C_F)/C_F$. This noise gain allows the feedback loop to crossover at a low enough frequency where its stability is not degraded by the load capacitance. Since the low-frequency noise gain is unity, the dc precision of the circuit is maintained.

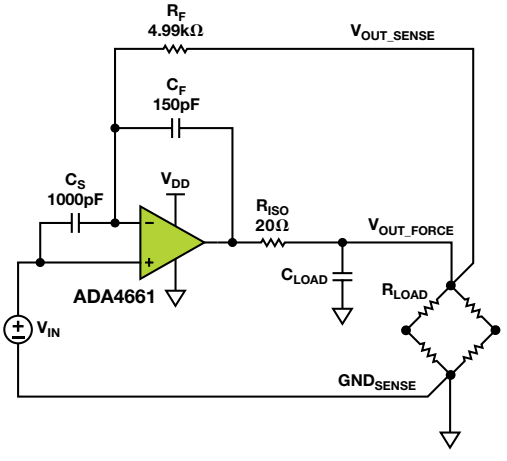

Figure 3. Bridge-driver schematic.

Maintaining the dc precision requires careful attention to the signal routing because of the large currents involved. It only takes 7 mΩ to create a 300 µV drop from the 42-mA maximum load current; this error is as large as the amplifier's offset voltage.

A practical way of dealing with this problem is the 4-wire Kelvin connection, which uses two current-carrying connections (typically called "force") to drive the load current and two voltage-measurement connections (typically called "sense"). The sense connections must be made as close to the load as possible to prevent any load current from flowing in them.

For the bridge-driver circuit, the sense connections should be made directly at the top and bottom of the bridge. None of the PCB traces or cabling should be shared between the force and sense lines. The GND_{SENSE} connection should be routed back to voltage source V_{IN}. For example, if the stimulus is a DAC, then GND_{SENSE} should be connected to REF_{GND} of the DAC. The GND_{FORCE} connection of the bridge should have its own dedicated trace all the way back to the power supply, as allowing bridge currents to flow through a ground plane will generate undesirable voltage drops.

Error Budget

The dc error budget for this circuit, shown in Table 1, is dominated by the amplifier's offset voltage and offset-voltage drift. It assumes a worst-case range of operating conditions. The total error meets the 1-mV requirement by a comfortable margin.

Table 1. Error Budget

Parameter	Conditions	Calculation	Error
Offset Voltage	0 V < V_{CM} < 5 V; 6.75 V < V_{DD} < 15 V		300 µV
Offset-Voltage Drift	0 V < V_{CM} < 5 V; 6.75 V < V_{DD} < 15 V; −40°C < T < +70°C	300 µV/°C × 110°C	341 µV
Power Dissipation	V_{DD} = 15 V; 0 V < V_{CM} < 5 V	Equation 1	168 µV
Gain Error	0 V < V_{CM} < 5 V ; −40°C < T < +125°C	5 V × 1/(105 dB + 1)	27 µV
Power-Supply Rejection	6.75 V < V_{DD} < 15 V	8.25 V/120 dB	8 µV
Total Error			844 µV

The third term in the table is the power-dissipation error. The power dissipated by the amplifier increases the die temperature, which causes the offset voltage to drift from that of ambient temperature with no load current. The worst-case error is calculated with the highest power-supply voltage, highest-output voltage, and smallest resistive load, as shown in Equation 1. Note that the worst-case voltage drop across the amplifier is reduced somewhat by the R_{ISO} resistor.

$$V_{PDISS} = V_{DROP} I_{LOAD} \Theta_{JA} TC_{VOS}$$
$$V_{PDISS} = \left[15V - 5V\left(1 + \frac{20\,\Omega}{120\,\Omega}\right)\right]\left[\frac{5V}{120\,\Omega}\right]\left[142\frac{^{\circ}C}{W}\right]\left[3.1\frac{\mu V}{^{\circ}C}\right] \quad (1)$$
$$V_{PDISS} = 168\,\mu V$$

DC Measurement Results

The error voltage is the difference between the input voltage, V_{IN}, and the load voltage, V_{OUT}. Figure 4 shows the prototype circuit's error voltage vs. load voltage. The largest error sources in the bridge-driver circuit are the offset voltage and offset-voltage drift. An additional error is dependent on the bridge voltage due to the power dissipation in the amplifier. The effect of power-supply voltage on power dissipation can be seen with the different color curves. The black curve dissipates the smallest amount of power (50 mW) with the minimum supply voltage (7 V). The die temperature rise is only 7°C, so this curve represents the room temperature offset voltage vs. common-mode voltage behavior of this part.

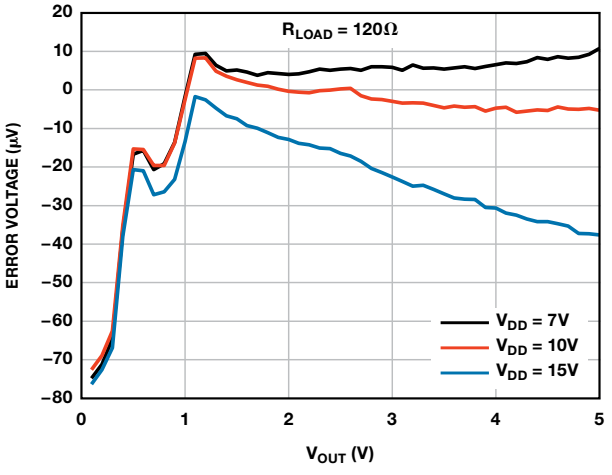

Figure 4. Error voltage vs. output voltage.

The red (10 V) and blue (15 V) curves represent the performance with maximum power dissipation of 175 mW and 385 mW, respectively. As the output voltage increases, the extra power dissipation causes the die temperature to increase by 25°C to 55°C, which causes the offset voltage to drift. The shape of this additional thermal error will be parabolic since the maximum power dissipation occurs when V_{OUT} is one-half of V_{DD}.

The strong dependence of power supply on the offset voltage suggests that the power-supply rejection of this circuit should be considered. Figure 5 shows the error voltage as the supply voltage is swept while the output voltage is fixed. The black curve shows the lightly loaded case, which is dominated by the amplifier's power-supply rejection (PSR). For this device, the 10 µV change represents 118 dB PSR. The red and blue curves show the results when the output dissipates extra power due to being loaded with typical bridge resistances of 350 Ω and 120 Ω. The effective PSRs of the red and blue curves are 110 dB and 103 dB, respectively.

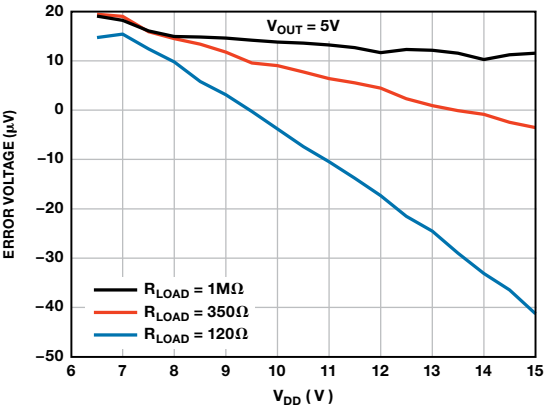

Figure 5. Error voltage vs. supply voltage.

The performance of this circuit clearly depends on the offset drift vs. temperature. So far, the TCV_{OS} specification has been used for all calculations of temperature-dependent error. This assumption must be justified because die temperature increases due to amplifier power dissipation are different than ambient temperature changes. The former creates large thermal gradients across the surface of the die, which can upset the sensitive balance of the amplifier. These gradients can result in offset voltage drifts significantly worse than the data sheet specifications. The ADA4661-2 has been specifically designed to dissipate significant power without degrading its offset-drift performance.

Figure 6 shows the measured offset drift vs. temperature. The specified performance is replicated in the black curve with low power-supply voltages and high-resistance loads (–1.2 µV/°C). The red curve shows the results for a 120-Ω bridge load. The important thing to notice is that the shape of the curve does not change; it is just shifted to the left by the die temperature rise (6.4°C). The blue curve shows the results when the power supply is increased to 15 V—the condition where the circuit's maximum power dissipation can be measured. Once again, the shape of the curve does not change, being shifted left due to the 55°C rise in die temperature. The internal power dissipation is known (385 mW), so the actual thermal impedance (θ_{JA}) of the system can be calculated (143°C/W). It is important to consider the ambient temperature range of operation. The maximum die temperature should not exceed 125°C; this means that the maximum ambient temperature is 70°C for the worst-case load.

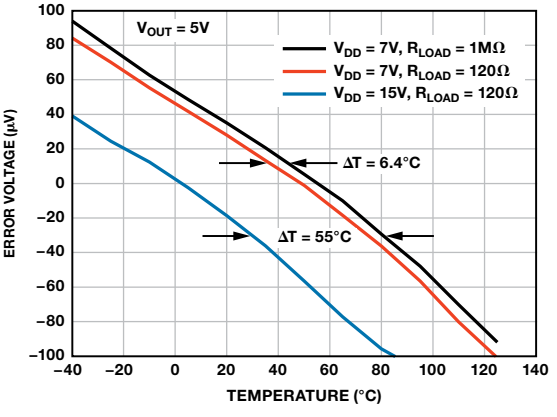

Figure 6. Error voltage vs. ambient temperature.

Transient Measurement Results

The step response of the circuit is a simple way to evaluate the loop stability. Figure 7 shows the measured step response for a range of capacitive loads for high-resistance bridges; Figure 8 shows the same measurement for low-resistance bridges. The circuit has a characteristic overshoot in the step response due to the pole-zero doublet in the feedback network. This doublet response is fundamental because the circuit's feedback factor drops from unity at low frequency to 0.13 at high frequency. Since the zero is at a higher frequency than the pole, the step response will always overshoot, even with more than adequate phase margin. In addition, the doublet has the longest time constant in the circuit, so it tends to dominate the settling time. The worst-case stability and output stage ringing is seen with high-resistance loads and 1-nF capacitive loads.

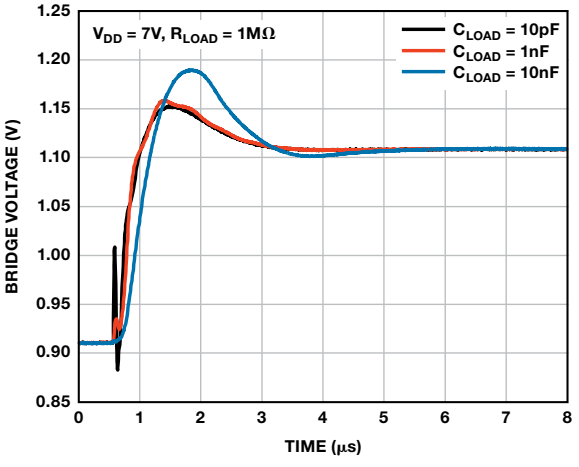

Figure 7. Unloaded step response.

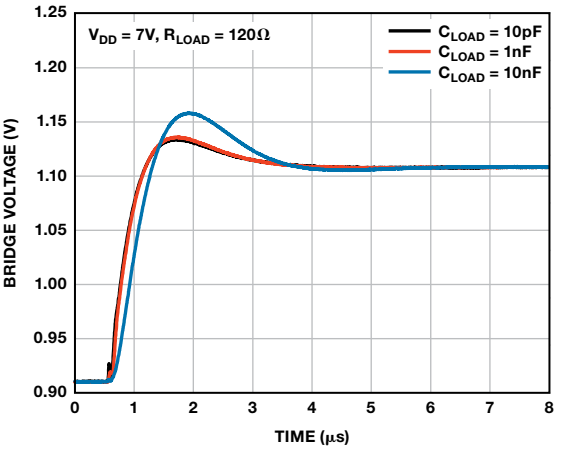

Figure 8. Loaded step response.

Conclusion

The load-driver circuit presented here can apply 5 V to resistive loads as low as 120 Ω with less than 1-mV of total error and stably drive up to 10 nF of total capacitance. The circuit meets its rated performance while operating with a wide range of power supplies from 7 V to 15 V and dissipating almost 400 mW. The basic circuit can be extended to drive positive and negative loads by powering the amplifier with ±7-V power supplies. All of this capability is accomplished with one tiny 3-mm × 3-mm amplifier and four passive components.

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