Highest Power Density, Multirail Power Solution for Space-Constrained Applications

By Maurice O'Brien

As the overall size of communications, medical, and industrial equipment continues to decrease, power management becomes an increasingly important design consideration. This article looks at applications for new highly integrated power management solutions, the advantages these new devices bring for powering RF systems, FPGAs, and processors, and a design tool that helps empower designers to quickly implement a new design.

The emergence of femtocells and picocells in communications infrastructure is driving the need for smaller base stations, which have complex requirements for powering digital baseband, memory, RF transceivers, and power amplifiers in the smallest area with the highest power efficiency, as shown in Figure 1. A typical small cell system needs a very dense power supply that can deliver large currents with fast transient response to power the digital baseband, along with low-noise, low-dropout regulators (LDOs) to power the AD9361 RF Agile Transceiver,™ temperature compensated crystal oscillator (TCXO), and other noise-critical rails. Setting the switching frequency of the switching regulators outside of the critical RF bands reduces noise, and synchronizing the switching regulators ensures that beat frequencies do not affect the RF performance. Reducing the core voltage (V_{CORE}) of the digital baseband minimizes power consumption for low-power modes, and supply sequencing ensures that the digital baseband processor is up and running before the RF transceiver is enabled. An I²C interface between the digital baseband and the power management allows the output voltages of the buck regulators to be changed. To increase reliability, the power management system can monitor its own input voltage and die temperature, reporting any faults to the baseband processor.
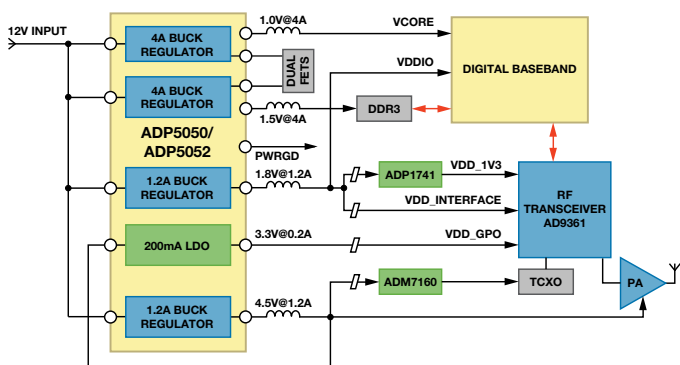

Figure 1. Small base stations require a variety of power supplies.

Similarly, the trend in medical and instrumentation devices—for example, portable ultrasound and handheld instrumentation—is toward significantly smaller form factors, so these products are driving the need for smaller, more efficient ways of powering FPGAs, processors, and memory, as shown in Figure 2. A typical FPGA and memory design needs a very dense power supply that can deliver large currents with fast transient response to power the core and I/O rails, along with a low-noise rail to power on-chip analog circuitry such as a phase-locked loop (PLL). Power supply

sequencing is critical to ensure that the FPGA is up and running before the memory is enabled. Regulators with a precision enable input and a dedicated power-good output allow power supply sequencing and fault monitoring. Power supply designers often want to use the same power IC in different applications, so the ability to change the current limits is important. This design reuse can significantly reduce time to market—a critical element in any new product development process.
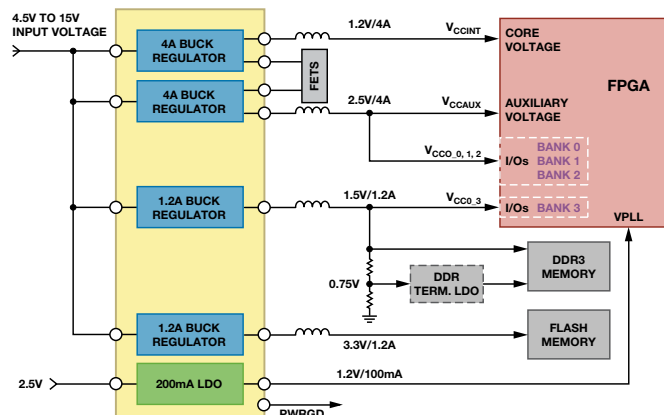

Figure 2. Powering an FPGA-based system.

Consider a common multirail power management design specification for an FPGA with a 12-V input and five outputs:
- Core: 1.2 V @ 4 A
- Auxiliary: 1.8 V @ 4 A
- I/O: 3.3 V @ 1.2 A
- DDR memory: 1.5 V @ 1.2 A
- Clock: 1.0 V @ 200 mA

A typical discrete implementation, shown in Figure 3a, connects four switching regulators to the 12-V input rail. The output of one switching regulator preregulates the LDO to reduce power dissipation. An alternative approach, shown in Figure 3b, uses one regulator to step the 12-V input down to a 5-V intermediate rail, which is then regulated down to produce each of the required voltages. This implementation has a lower solution cost, but also a lower efficiency due to the two-stage power conversion. In both cases, each regulator has to be enabled independently, so supply sequencing may require a dedicated power supply sequencer. Noise may also be an issue, unless all of the switchers can be synchronized to reduce beat frequencies.
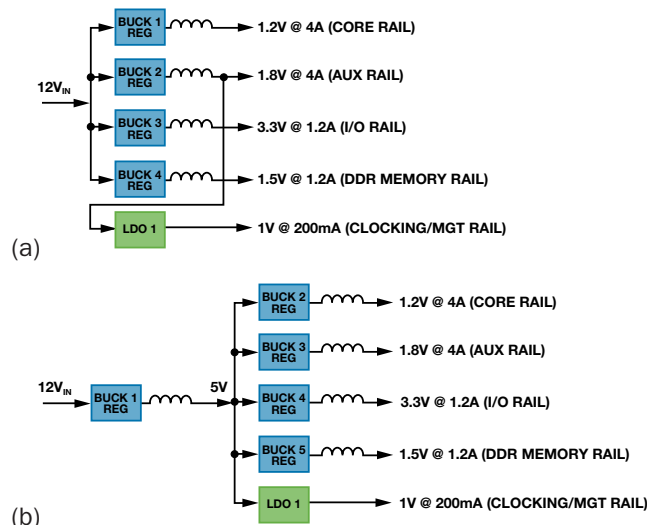

Figure 3. (a) Discrete regulator design and (b) alternative discrete regulator design.

Integrated Solution Yields High Efficiency, Small Size

Integrating multiple buck regulators and LDOs into a single package can significantly reduce the overall size of a power management design. In addition, smart integrated solutions provide many advantages over traditional discrete implementations. Reducing the number of discrete components can significantly reduce the cost, complexity, and manufacturing cost of the design. The ADP5050 and ADP5052 integrated power management units (PMUs) can implement all these voltages and features in a single IC, using significantly less PCB area and fewer components.

For highest efficiency, each of the buck regulators can be powered directly from 12 V (similar to Figure 3a), removing the need for a preregulator stage. Buck 1 and Buck 2 have programmable current limits (4 A, 2.5 A, or 1.2 A), allowing the power supply designer to quickly and easily change the currents for new designs and significantly reducing the development time. The LDO can be powered from a 1.7-V to 5.5-V supply. In this example, the 1.8-V output from one of the buck regulators powers the LDO to provide a low-noise 1-V rail for the noise-sensitive analog circuitry.

The switching frequency, f_{SW}, is set between 250 kHz and 1.4 MHz by resistor R_{RT}. The flexible switching frequency range allows the power supply designer to optimize the design, reducing the frequency for highest efficiency or increasing the frequency for smallest overall size. Figure 4 shows the relationship between f_{SW} and R_{RT}. The value of R_{RT} can be calculated as

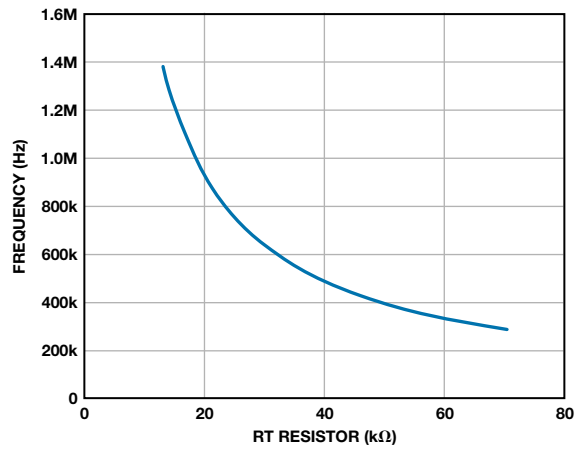$$R_{RT} = (14822/f_{SW})^{1.081}, \text{ with R in } k\Omega \text{ and } f \text{ in kHz.}$$

Figure 4. Switching frequency vs. R_{RT}.

In some designs it is desirable to have both: a lower switching frequency to provide the highest power efficiency for the higher current rails, and a higher switching frequency to reduce inductor size and minimize PCB area for the lower current rails. A divide-by-two option on the master switching frequency allows the ADP5050 to operate at two frequencies, as shown in Figure 5. The switching frequency for Buck 1 and Buck 3 can be set via the I²C port to one-half of the master switching frequency.

TOTAL PCB AREA AROUND 23mm × 13.5mm = 310mm²
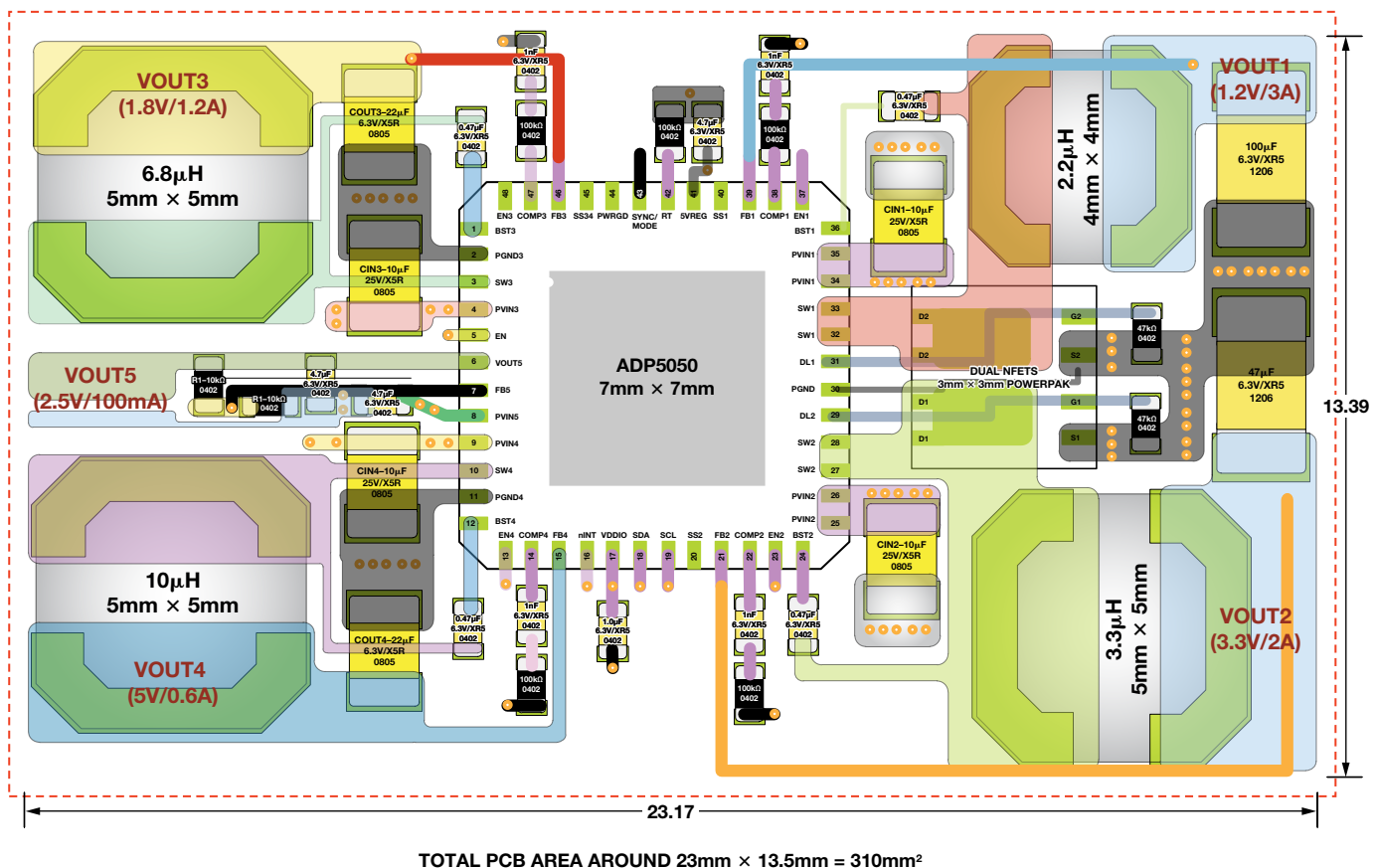
LAYOUT EXAMPLE:
V_{IN} = 12V
BUCK 1: 3A @ 600kHz
BUCK 2: 2A @ 1.2MHz
BUCK 3: 1.2A @ 600kHz
BUCK 4: 0.6A @ 1.2MHz
LDO: 0.1A

Figure 5. The ADP5050 operates at a low switching frequency for high efficiency on high-current rails and a high frequency for small inductor size on low-current rails.

Power Supply Sequencing

As shown in Figure 6, the ADP5050 and ADP5052 have four features that simplify power supply sequencing that is required for applications using FPGAs and processors: precision enable inputs, programmable soft start, a power-good output, and an active output discharge switch.

Precision Enable Inputs: Each regulator, including the LDO, has an enable input with a precise 0.8-V reference (Figure 6-1). When the voltage at an enable input is greater than 0.8 V, the regulator is enabled; when the voltage falls below 0.725 V, the regulator is disabled. An internal 1-MΩ pull-down resistor prevents errors if the pin is left floating. The precision enable threshold voltage allows easy sequencing within the device, as well as with external supplies. As an example, if Buck 1 is set to 5 V, a resistor divider can be used to set an accurate 4.0-V trip point to enable Buck 2, and so on, setting an accurate power-up sequence for all outputs.

Programmable Soft Start: Soft start circuitry ramps the output voltage in a controlled manner, limiting the inrush current. The soft start time is set to 2 ms when the soft start pins are tied to V_{REG}, or it can be increased up to 8 ms by connecting a resistor divider from the soft start pin to V_{REG} and ground (Figure 6-2). This configuration may be required to accommodate a specific start-up sequence or an application with a large output capacitor. The configurability and flexibility of the soft start enable large, complex FPGAs and processors to power up in a safe, controlled manner.

Power-Good Output: An open-drain power-good output (PWRGD) goes high when the selected buck regulators are operating normally (Figure 6-3). The power-good pins allow the power supply to signal the host system about its health. By default, PWRGD monitors the output voltage on Buck 1, but other channels can be custom ordered to control the PWRGD pin. The status of each channel (PWRGx bit) can be read back via the I²C interface on the ADP5050. A logic high on the PWRGx bit indicates that the regulated output voltage is above 90.5% of its nominal output. The PWRGx bit is set to logic low when the regulated output voltage falls below 87.2% of its nominal output for more than 50 μs. The PWRGD output is the logical AND of the internal unmasked PWRGx signals. An internal PWRGx signal must be high for at least 1 ms before PWRGD goes high; if any PWRGx signal fails, PWRGD goes low with no delay. The channels that control PWRGD (Channel 1 to Channel 4) are specified by factory fuse or by setting bits via the I²C interface.

Active Output Discharge Switch: Each buck regulator integrates a discharge switch from the switching node to ground (Figure 6-4). Turned on when its associated regulator is disabled, the switch helps the output capacitor to discharge quickly. The typical resistance of the discharge switch is 250 Ω for Channel 1 to Channel 4. The active discharge switch pulls the output to ground when the regulator is disabled, even when a large capacitive load is present. This significantly increases the robustness of the system, particularly when it is power cycled.
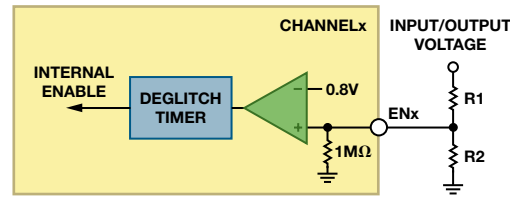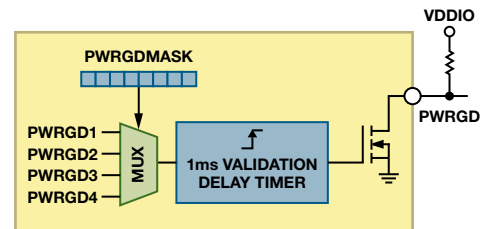

1. Precision Enabled Threshold
Above 0.8V to enable the regulator, below 0.72V (hysteresis) to shutdown the regulator.
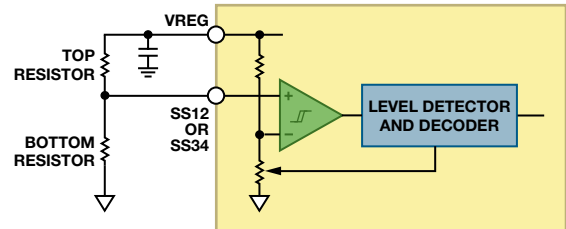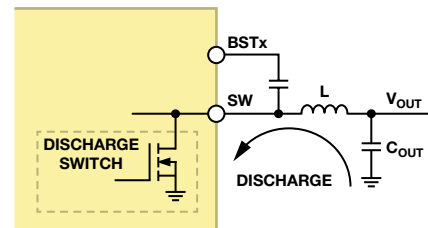

2. Programmable Soft Start
The different soft start on each channel can be programmable to be 2ms, 4ms, 8ms.

3. PWRGD Output
The desirable PWRGDx from CH1 to CH4 can be configured by the factory fuse or I²C.

4. Active Output Discharge Switch
The output discharge switch can be turned ON to shorten the discharge period of the output capacitors.

Figure 6. ADP5050 and ADP5052 simplify power supply sequencing.

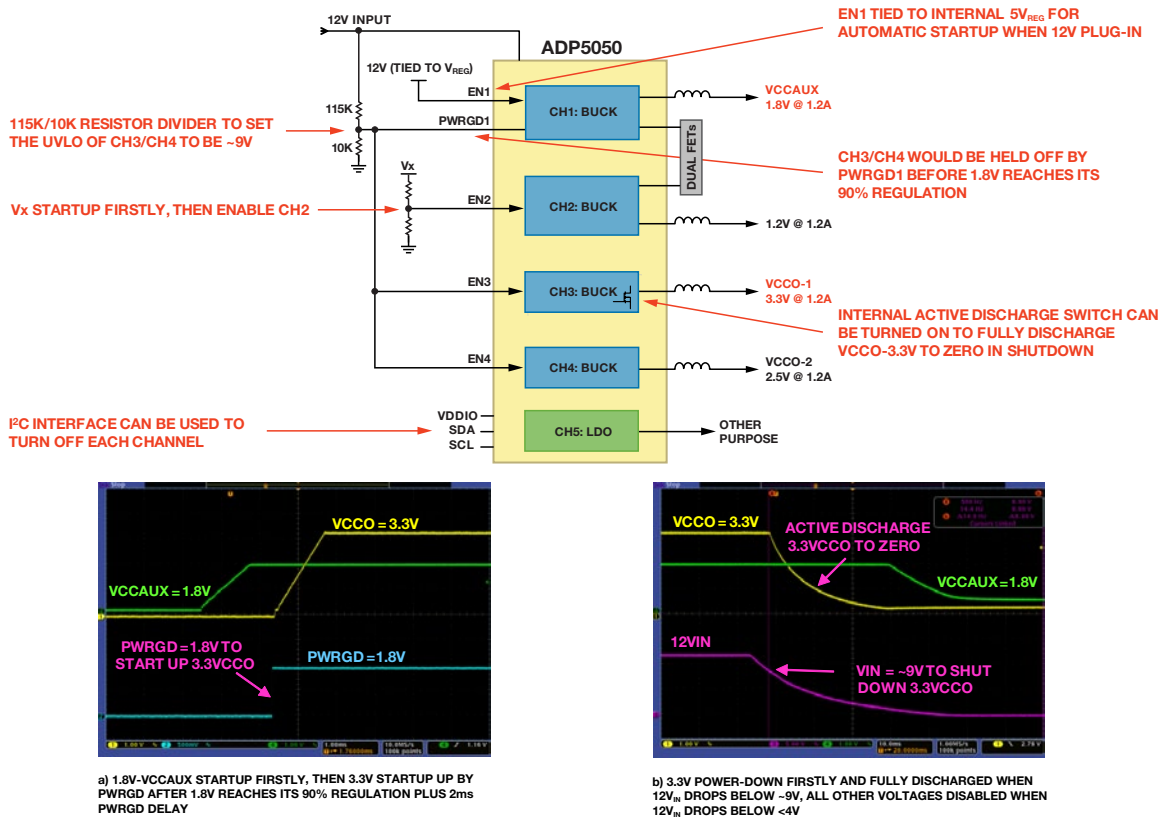Figure 7 shows a typical power-up/power-down sequence.

Figure 7. Typical power-up/power-down sequence.

I²C Interface

The I²C interface enables advanced monitoring capability and basic dynamic voltage scaling of the two buck regulator outputs (Channel 1 and Channel 4).

Input Voltage Monitor: The input voltage can be monitored for faults such as undervoltage conditions. As an example, with 12 V applied to the input, the I²C interface is configured to trigger an alert if the input voltage falls below 10.2 V. The signal on a dedicated pin (nINT) tells the system processor that a problem has occurred and shuts the system down for corrective action. The ability to monitor the input voltage increases system reliability.

Figure 8 shows the values that can be programmed to monitor the input voltage of the ADP5050.

Junction Temperature Monitor: The junction temperature can be monitored for faults such as overtemperature conditions. If the junction temperature increases above a preset level (105°C, 115°C, or 125°C), an alert is signaled on nINT. Unlike thermal shutdown, this function sends a warning signal, but does not shut down the device. The ability to monitor the junction temperature and alert the system processor to possible systems failures before they happen increases the system reliability, as shown in Figure 9.
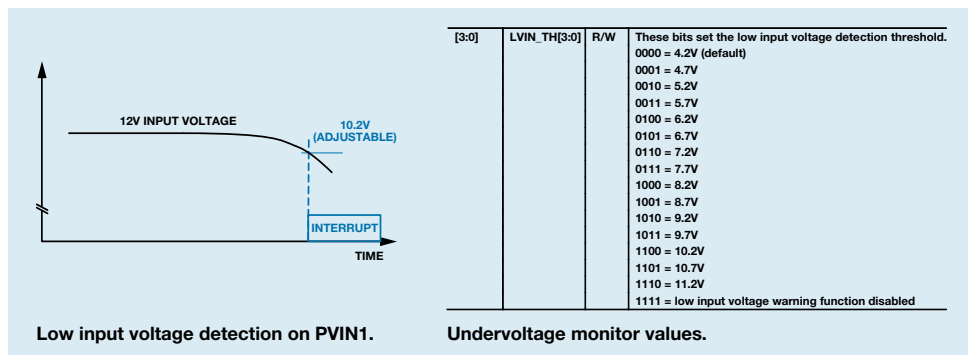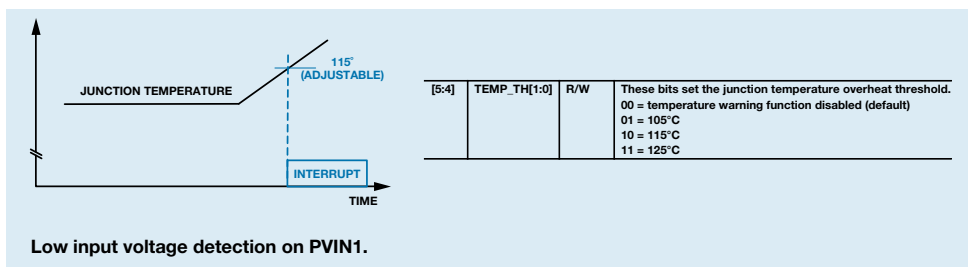

Figure 8. Input undervoltage detection.

Figure 9. Junction temperature monitoring.

Dynamic Voltage Scaling: Dynamic voltage scaling allows the system to reduce power consumption by dynamically lowering the power supply voltage on Channel 1 and Channel 4 for low-power modes, or it can dynamically change the output voltage depending on the system configuration and system loading. Also, the output voltages of all four buck regulators can be set via the I²C interface, as seen in Figure 10.
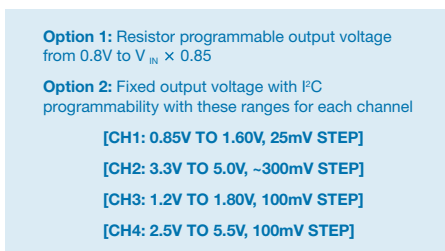

Figure 10. ADP5050 output voltage options.

Low Noise Features

Several features reduce system noise generated by the power supply:

Wide Resistor Programmable Switching Frequency Range: A resistor on the RT pin programs the switching frequency between 250 kHz and 1.4 MHz. This flexibility allows the power supply designer to set the switching frequency to avoid system noise bands.

Buck Regulator Phase Shifting: The phase shift of the buck regulators can be programmed via the I²C interface. By default, the phase shift between Channel 1 and Channel 2 and between Channel 3 and Channel 4 is 180°, as shown in Figure 11. The benefit of out-of-phase operation is reduced input ripple current and less ground noise on the power supply.
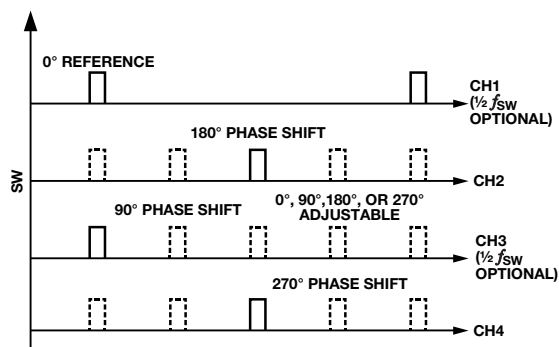

Figure 11. Phase shift of the buck regulators in the ADP5050/ADP5052.

The phase shift of Channel 2, Channel 3, and Channel 4 can be set to 0°, 90°, 180°, or 270° with respect to Channel 1 using the I²C interface, as shown in Figure 12. When parallel operation is configured to provide a single combined output of up to 8 A on Channel 1 and Channel 2, the switching frequency of Channel 2 is locked to a 180° phase shift with respect to Channel 1.
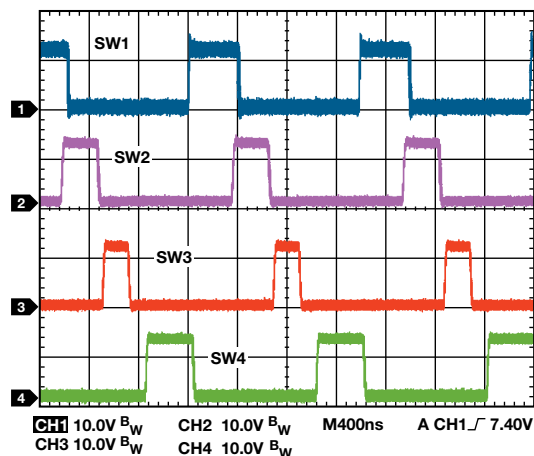

Figure 12. Phase shift of buck regulators can be configured via the I²C interface.

Clock Synchronization: The switching frequency can be synchronized to an external clock in the 250-kHz to 1.4-MHz range via the SYNC/MODE pin. This ability is important in RF and noise-sensitive applications. When an external clock is detected, the switching frequency transitions smoothly to its frequency. When the external clock stops, the device switches back to the internal clock and continues to operate normally. Synchronizing to an external clock allows the system designer to stay away from critical noise frequency bands and reduces the noise generated by multiple devices in a system.

For successful synchronization, the internal switching frequency must be programmed to a value close to that of the external clock value; a frequency difference of less than ±15% is suggested.

The SYNC/MODE pin can be configured as a synchronization clock output via a factory fuse or the I²C interface. A positive clock pulse with a 50% duty cycle is generated at the SYNC/MODE pin with a frequency equal to the internal switching frequency. A short time delay (~15% of t_{SW}) occurs between the generated synchronization clock and the Channel 1 switching node.

Figure 13 shows two devices configured in frequency synchronization mode: one device is configured as the clock output to synchronize the other device. A 100 kΩ pull-up resistor should be used to prevent logic errors if the SYNC/MODE pin is left floating.
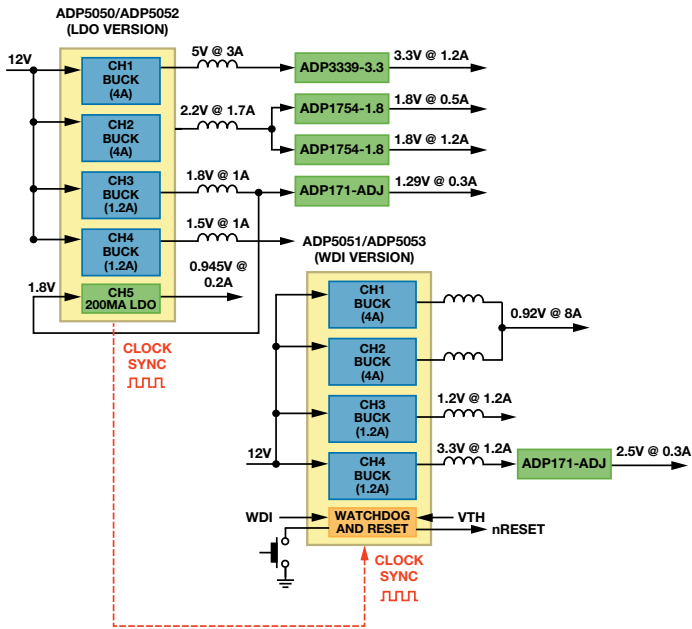

Figure 13. RF application shows two devices synchronized to reduce power supply noise.

Both devices are synchronized to the same clock, so the phase shift between Channel 1 of the first device and Channel 1 of the second device is 0°, as shown in Figure 14.
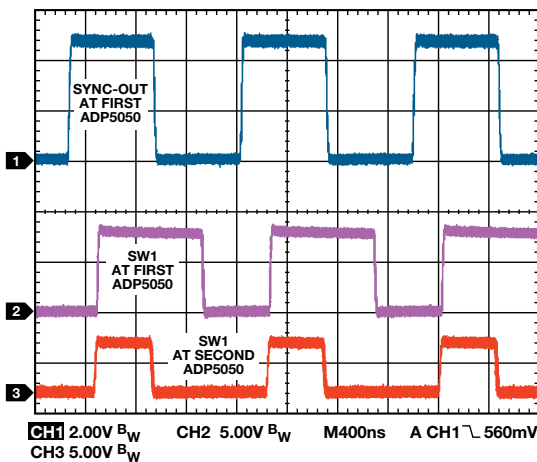

Figure 14. Waveforms of two ADP5050 devices operating in synchronized mode.

ADIsimPower Design Tool

ADIsimPower™ now supports the ADP5050/ADP5052 multichannel high-voltage PMUs, which power 4/5 channels with load current up to 4 A per channel from inputs up to 15 V. The design tool allows users to optimize the design by cascading channels, placing high-current channels in parallel to create an 8-A rail, and considering the thermal contributions of each channel. With the advanced features, users can independently specify each channel's performance for ripple and transient performance, switching frequency, and channels that support half the master frequency.

ADIsimPower allows the user to quickly and easily input the design requirements on the software interface shown in Figure 15.
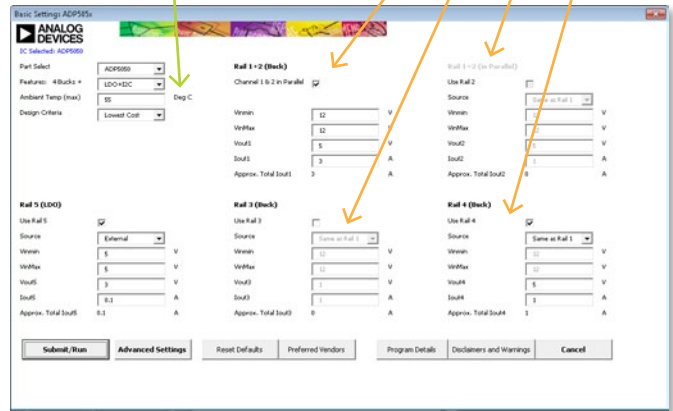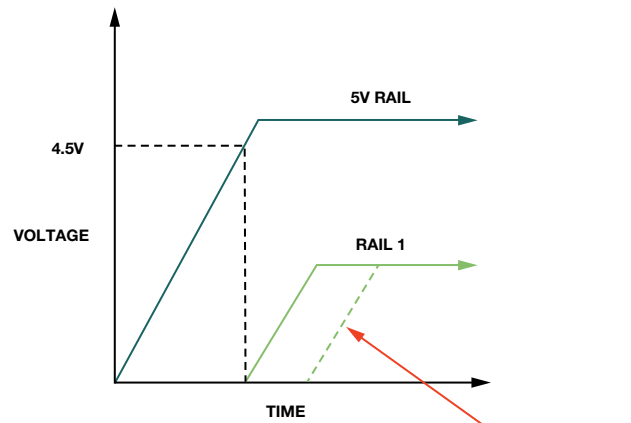

Figure 15. ADIsimPower software interface.

A full bill of materials is generated with intelligent component selection. Evaluation boards can be requested from within the tool. The design tool allows for sophisticated controls for each channel, as shown in Figure 16.

Figure 16. (a) Ripple, transient, and response can be specified for each rail. (b) Advanced sequencing requirements using precision enable.

ADIsimPower gives the power designer quick access to accurate, tested, reliable performance data, as shown in Figure 17.
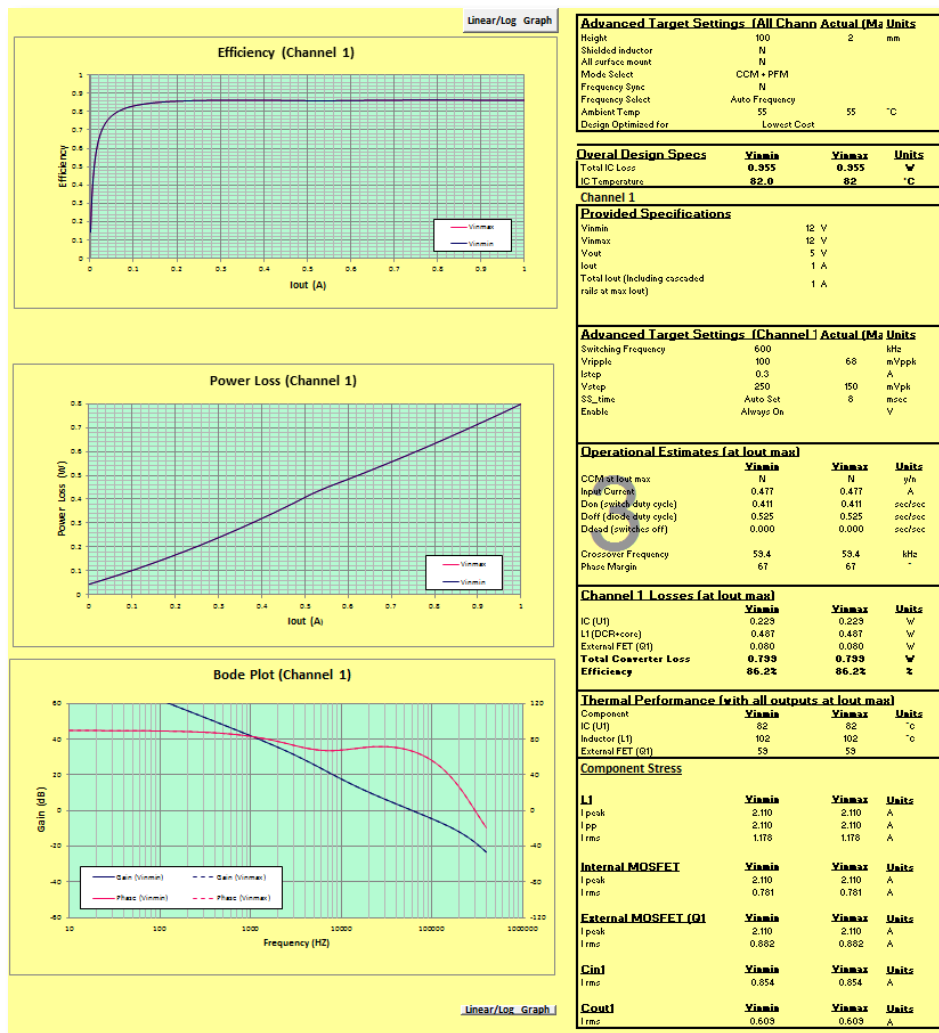

Figure 17. ADIsimPower simulation output.

Advanced Target Settings (All Chann	Actual (Ma	Units
Height	100	2 mm
Shielded inductor	N	
All surface mount	N	
Mode Select	CCM + PFM	
Frequency Sync	N	
Frequency Select	Auto Frequency	
Ambient Temp	55	55 °C
Design Optimized for	Lowest Cost	

Overal Design Specs	Vinmin	Vinmax	Units
Total IC Loss	0.955	0.955	W
IC Temperature	82.0	82	°C

Channel 1

Provided Specifications		
Vinmin	12	V
Vinmax	12	V
Vout	5	V
Iout	1	A
Total Iout (Including cascaded rails at max Iout)	1	A

Advanced Target Settings (Channel 1	Actual (Ma	Units
Switching Frequency	600	kHz
Vripple	100	68 mVppk
Istep	0.3	A
Vstep	250	150 mVpk
SS_time	Auto Set	8 msec
Enable	Always On	V

Operational Estimates (at Iout max)	Vinmin	Vinmax	Units
CCM at Iout max	N	N	y/n
Input Current	0.477	0.477	A
Don (switch duty cycle)	0.411	0.411	sec/sec
Doff (diode duty cycle)	0.525	0.525	sec/sec
Ddead (switches off)	0.000	0.000	sec/sec
Crossover Frequency	59.4	59.4	kHz
Phase Margin	67	67	

Channel 1 Losses (at Iout max)	Vinmin	Vinmax	Units
IC (U1)	0.229	0.229	W
L1 (DCR+core)	0.487	0.487	W
External FET (Q1)	0.080	0.080	W
Total Converter Loss	0.799	0.799	W
Efficiency	86.2%	86.2%	%

Thermal Performance (with all outputs at Iout max)			
Component	Vinmin	Vinmax	Units
IC (U1)	82	82	°c
Inductor (L1)	102	102	°c
External FET (Q1)	59	59	

Component Stress			
L1	Vinmin	Vinmax	Units
I peak	2.110	2.110	A
I pp	2.110	2.110	A
I rms	1.178	1.178	A
Internal MOSFET	Vinmin	Vinmax	Units
I peak	2.110	2.110	A
I rms	0.781	0.781	A
External MOSFET (Q1	Vinmin	Vinmax	Units
I peak	2.110	2.110	A
I rms	0.882	0.882	A
Cin1	Vinmin	Vinmax	Units
I rms	0.854	0.854	A
Cout1	Vinmin	Vinmax	Units
I rms	0.603	0.603	A

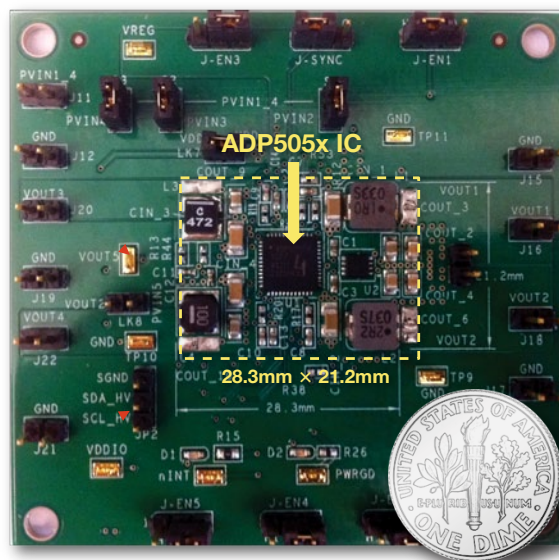The design can then be assembled on an evaluation board, as shown in Figure 18.

Figure 18. Power supply circuit using ADP5050/ADP5052.

ADP5050/ADP5052/ADP5051/ADP5053 Specifications

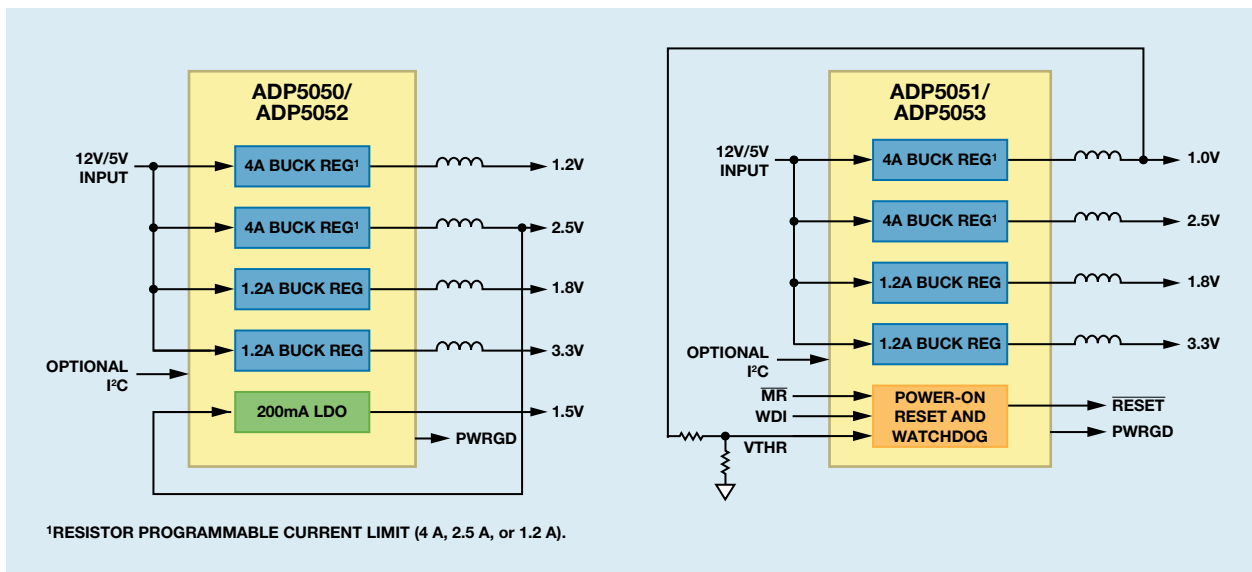| Part Number	Description	V$_{IN}$ (V)	V$_{OUT}$ (V)	Number of Outputs	Output Current (mA)	I^{2}C	Key Features	Package	Price ($U.S.)
ADP5050	Quad Buck Regulator, LDO, I^{2}C	Buck: 4.5 to 15	0.8 to 0.85 × V$_{IN}$	2 × Buck	4000, 2500, or 1200	Yes	I^{2}C interface with individual enable pins and power good	48-lead LFCSP	4.39
				2 × Buck	1200				
		LDO: 1.7 to 5.5	0.5 to 4.75	LDO	200				
ADP5051	Quad Buck Regulator, POR/WDI, I^{2}C	Buck: 4.5 to 15	0.8 to 0.85 × V$_{IN}$	2 × Buck	4000, 2500, or 1200	Yes	I^{2}C interface with individual enable pins and power good	48-lead LFCSP	4.59
				2 × Buck	1200				
ADP5052	Quad Buck Regulator, LDO	Buck: 4.5 to 15	0.8 to 0.85 × V$_{IN}$	2 × Buck	4000, 2500, or 1200	No	Individual enable pins and power good	48-lead LFCSP	3.59
				2 × Buck	1200				
		LDO: 1.7 to 5.5	0.5 to 4.75	LDO	200				
ADP5053	Quad Buck Regulator, POR/WDI	Buck: 4.5 to 15	0.8 to 0.85 × V$_{IN}$	2 × Buck	4000, 2500, or 1200	No	Individual enable pins and power good	48-lead LFCSP	3.79
				2 × Buck	1200				

Figure 19. ADP5050/ADP5051/ADP5052/ADP5053: quad buck switching regulators with LDO or POR/WDI in LFCSP.

Conclusion

New highly integrated PMUs are enabling complex power management solutions with high power efficiency, high reliability, and ultrasmall size; and new design tools combined with flexible integrated circuits reduce the time to market for these complex power supplies. The ADP505x family, the latest addition to ADI's portfolio of highly integrated multi-output regulators, allows a single IC to be used quickly and easily in many different applications, reducing power supply design time. To discuss technical aspects of these devices, please visit the EngineerZone® forum.

Author

Maurice O'Brien [maurice.obrien@analog.com] joined Analog Devices in 2002, following his graduation from the University of Limerick, Ireland, with a bachelor's degree in electronic engineering. He currently works as a product marketing manager in the Power Management product line. In his spare time, Maurice enjoys horse riding, outdoor sports, and travel.