Efficient FSK/PSK Modulator Uses Multichannel DDS to Switch at Zero Crossings

By David Brandon and Jeff Keip

Frequency-shift keying (FSK) and *phase-shift keying* (PSK) modulation schemes are used in digital communications, radar, RFID, and numerous other applications. The simplest form of FSK uses two discrete frequencies to transmit binary information, with Logic 1 representing the mark frequency and Logic 0 representing the space frequency. The simplest form of PSK is binary (BPSK), which uses two phases separated by 180°. Figure 1 illustrates the two types of modulation.

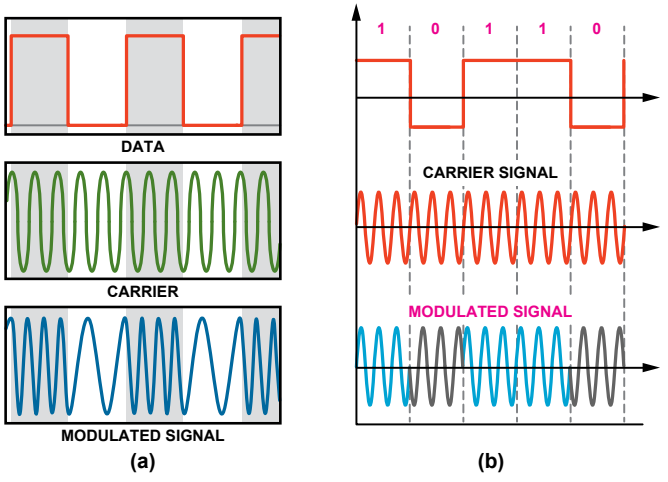

Figure 1. Binary FSK (a) and PSK (b) modulation.

The modulated output of a *direct digital synthesizer* (DDS) can switch frequency and/or phase in a *phase-continuous* or *phase-coherent* manner, as shown in Figure 1, and as described in "Multichannel DDS Enables Phase-Coherent FSK Modulation," making DDS technology well suited for both FSK and PSK modulation.

This article describes how two synchronized DDS channels can implement a *zero-crossing* FSK or PSK modulator. Here, the AD9958 two-channel, 500-MSPS, complete DDS (see Appendix) is used to switch frequencies or phases at the zero-crossing point, but any two-channel synchronized solution should be capable of accomplishing this function. In phase-coherent radar systems, zero-crossing switching reduces the amount of post processing needed for signature recognition of the target; and implementing PSK at the zero crossing reduces spectral splatter.

Although both of the AD9958 DDS-channel outputs are independent, they share an internal system clock and reside on a single piece of silicon, so they should provide more reliable channel-to-channel tracking over temperature and power-supply deviations than the outputs of multiple, single-channel devices synchronized together. The process variability that may exist between distinct devices is also larger than any process variability you might see between two channels fabricated in a single piece of silicon, making a multichannel DDS preferable for use as a zero-crossing FSK or PSK modulator.

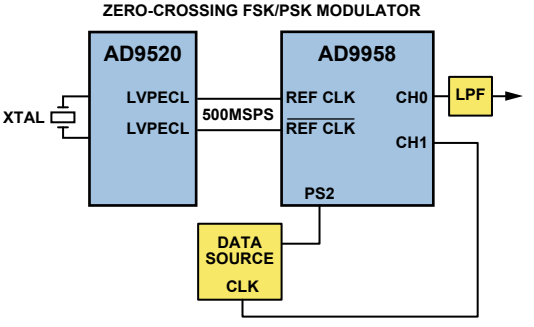

Figure 2. Setup for zero-crossing FSK or PSK modulator.

A critical element of any DDS is the phase accumulator, which, in this implementation, is 32 bits wide. When the accumulator overflows, it retains any excess value. When the accumulator overflows with no remainder (see Figure 3), the output is precisely at Phase 0, and the DDS engine starts over from where it was at Time 0. The rate at which the zero-overflow is experienced is referred to as the *grand-repetition rate* (GRR) of the DDS.

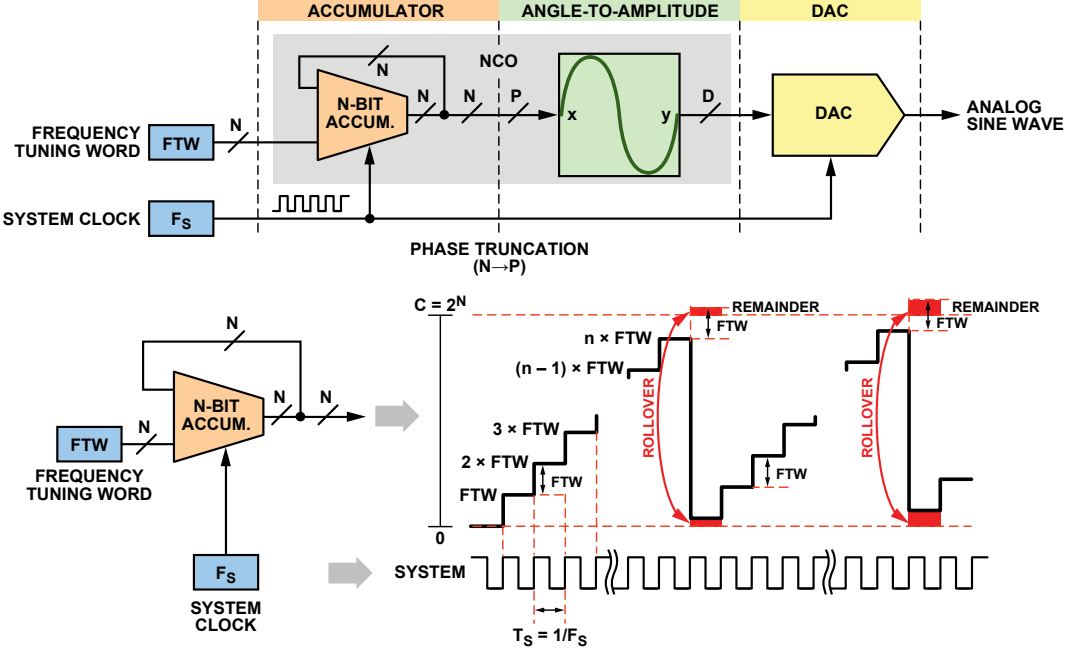

Figure 3. Basic DDS with overflowing accumulator.

The GRR is determined by the rightmost nonzero bit of the DDS *frequency tuning word* (FTW), as established by the following equation:

$$GRR = F_S/2^n$$

where:

F_S is the sampling frequency of the DDS.

n is the rightmost nonzero bit of the FTW.

For example, suppose a DDS with a 1-GHz sampling frequency employs 32-bit mark and space FTWs with the binary values shown. In this case, the rightmost nonzero bit of either FTW is the 19th bit, so GRR = 1 GHz/2^{19}, or approximately 1907 Hz.

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Mark  (CH0) 00101010 00100110 10100000 00000000
Space (CH0) 00111010 11110011 11000000 00000000
GRR   (CH1) 00000000 00000000 00100000 00000000
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A DDS inherently switches frequency in a phase-continuous manner. This means that no instantaneous phase change occurs when the frequency tuning word changes. That is, the accumulator starts accumulating the new FTW from whatever phase position it was at when the new FTW was applied. Phase coherence, on the other hand, requires an instantaneous transition to the phase of the new frequency as if the new frequency had been present all along. Therefore, in order for a standard DDS to implement a phase-coherent FSK switch, the change from a mark frequency to a space frequency must occur when both frequencies have the same absolute phase. To implement a zero-crossing switch in a phase-coherent manner, the DDS must make the frequency transition at 0 degrees (that is, when the accumulator overflows with zero excess). Therefore, we must determine the instants at which phase coherent zero-crossings occur. If the GRR of the mark and space FTWs are known, the smaller of the two GRRs (if different) will indicate the desired phase coherent zero-crossing point.

Three criteria are necessary for implementing a phase-coherent zero-crossing switch:

1. The ability to determine the smaller GRR of the mark and space FTWs associated with CH0 of Figure 2.
2. A second DDS channel (CH1 of Figure 2) synchronized to CH0 of Figure 2 and programmed with an FTW having all zeros except for the one bit corresponding to the smaller GRR.
3. The capability to use the rollover of the second channel to trigger a frequency change on CH0 of Figure 2.

Unfortunately, the latency between when a DDS accumulator hits zero and when that zero phase is represented at the output further complicates the solution. Fortunately, this latency is constant. The ideal solution necessitates that the auxiliary channel be phase adjusted to compensate for this latency. Both channels on the AD9958 have a *phase-offset* word that can be used to fix this problem.

The AD9958 two-channel DDS produced the results shown in Figure 4, Figure 5, and Figure 6. Figure 4 and Figure 5 exhibit phase-continuous FSK switching vs. zero-crossing FSK switching. Figure 5 shows both phase continuous switching and phase coherent switching. Figure 6 shows the results from a pseudorandom sequence (PRS) data stream that toggles between multiple frequencies.

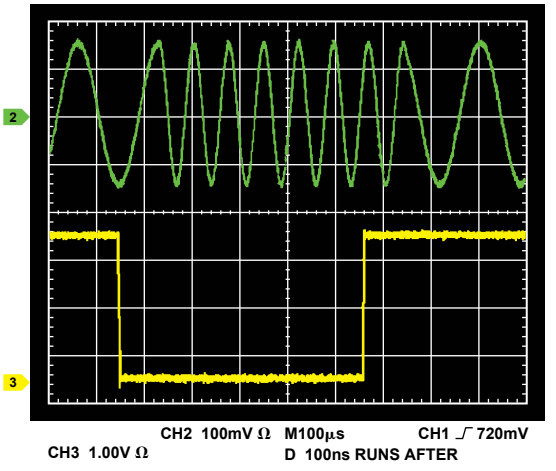

Figure 4. Phase-continuous FSK transition.

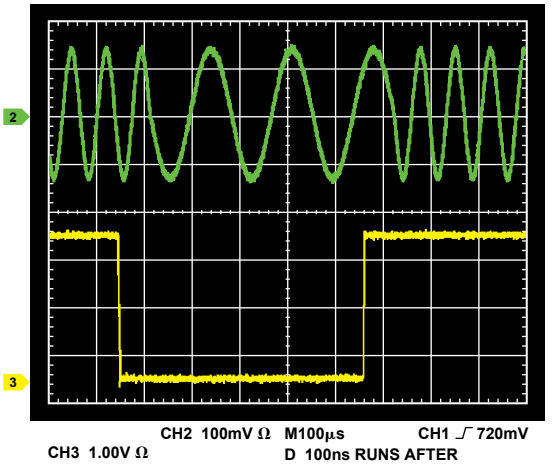

Figure 5. Zero-crossing FSK transition.

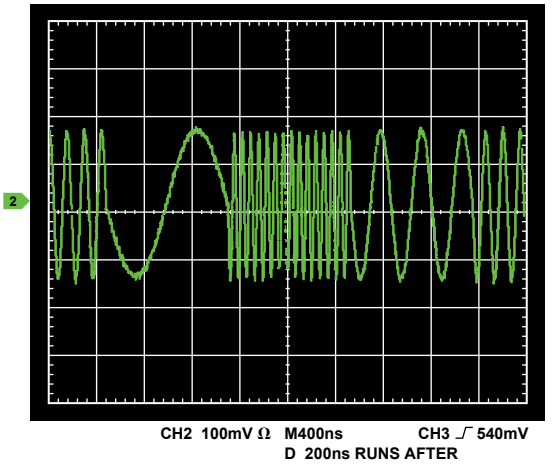

Figure 6. Zero-crossing with multi-FSK transitions.

The AD9958 two-channel DDS produced the results shown in Figure 7 and Figure 8. These figures exhibit phase-continuous BPSK switching vs. zero-crossing BPSK switching.

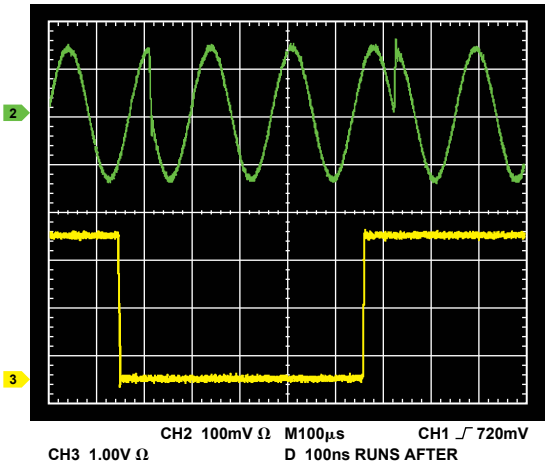

Figure 7. Phase-continuous BPSK transition.

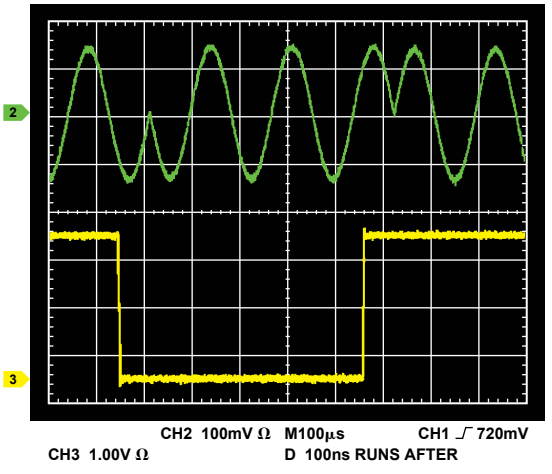

Figure 8. Zero-crossing BPSK transition.

Authors

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APPENDIX

Two-Channel, 10-Bit, 500-MSPS Direct Digital Synthesizer

The AD9958 two-channel direct digital synthesizer (DDS) comes complete with two 10-bit, 500-MSPS current-output DACs, as shown in Figure 9. Both channels share a common system clock, providing inherent synchronization; additional packages can be used if more than two channels are required. The frequency, phase, and amplitude of each channel can be independently controlled, allowing them to provide correction for system-related mismatches. These parameters can be swept linearly; or 16 levels can be chosen for FSK, PSK, or ASK modulation. Output sine waves can be tuned with 32-bit frequency resolution, 14-bit phase resolution, and 10-bit amplitude resolution. Operating with a 1.8-V core supply, plus a 3.3-V I/O supply for logic compatibility, the AD9958 consumes 315 mW with all channels *on*, and 13 mW in *power-down* mode. Specified from –40°C to +85°C, it is available in a 56-lead LFCSP package and priced at $20.24 in 1000s.

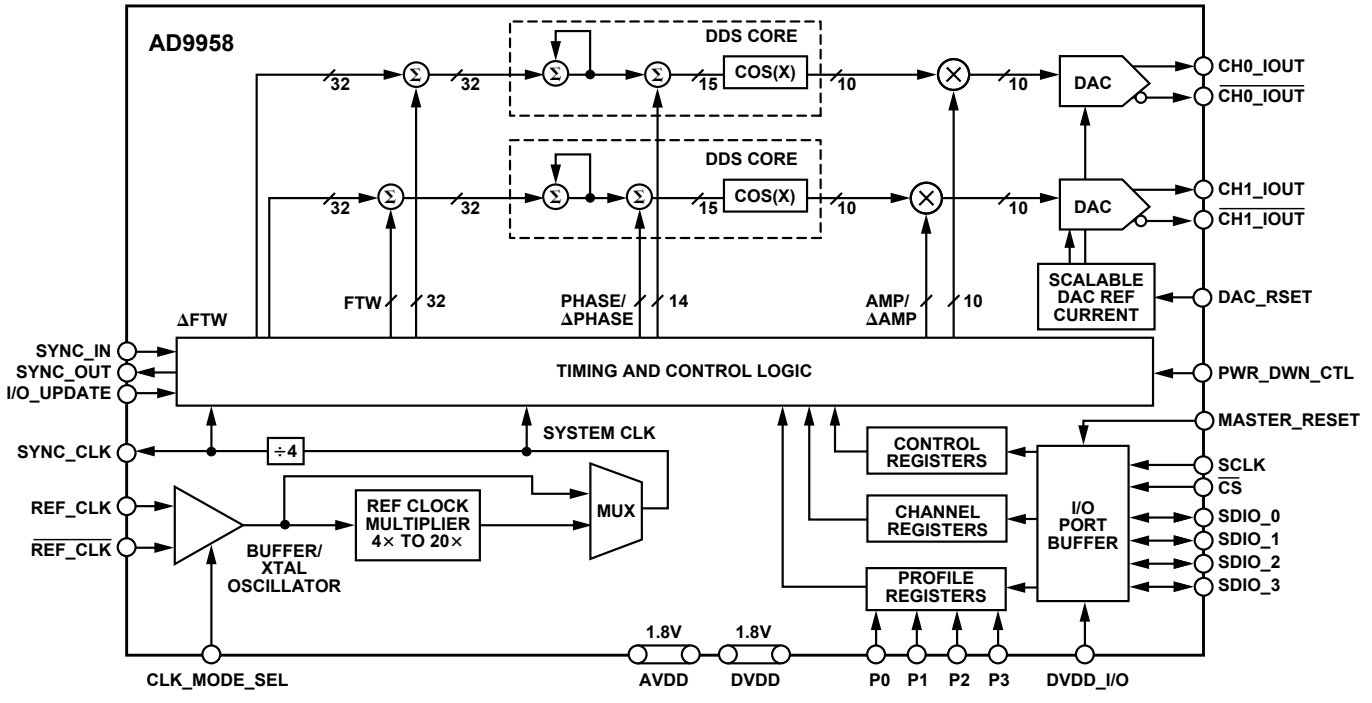

Figure 9. AD9958 block diagram.