Monitoring and Sequencing in Multirail Power-Supply Systems

By Rich Ghiorse

Introduction

Today's electronic systems are likely to have many different power supply rails. This is especially true in systems employing analog circuitry along with microprocessors, DSPs, ASICs, and FPGAs. For reliable, repeatable operation, the on-off timing, rise and fall rate, order of application, and magnitude of each of the supply voltages needs to be controlled. A given power system design may include supply sequencing, supply tracking, and supply voltage/current monitoring and control. A variety of power management ICs exists to perform the functions of sequencing, tracking, and monitoring for both power-up and power-down.

Sequencing and tracking devices can monitor and control multiple rails; their functions may include setting turn-on time and voltage ramp-up rate, undervoltage and overvoltage fault detection, *margining* (supply adjustment within a range around a nominal voltage value), and orderly shutdown. ICs for these applications may range from simple purely analog devices, with resistors, capacitors, and comparators, to highly integrated state machines and programmable devices digitally controlled via an I^2C bus. In some cases, the system's voltage regulators and controllers may include key control functions.

Another consideration for systems employing multiple switching controllers and regulators is how to minimize the system noise generated as they operate at various switching frequencies. It is often desirable to synchronize the regulators' clocks. In fact, many of today's high-performance switching controllers and regulators can be synchronized to an external clock.

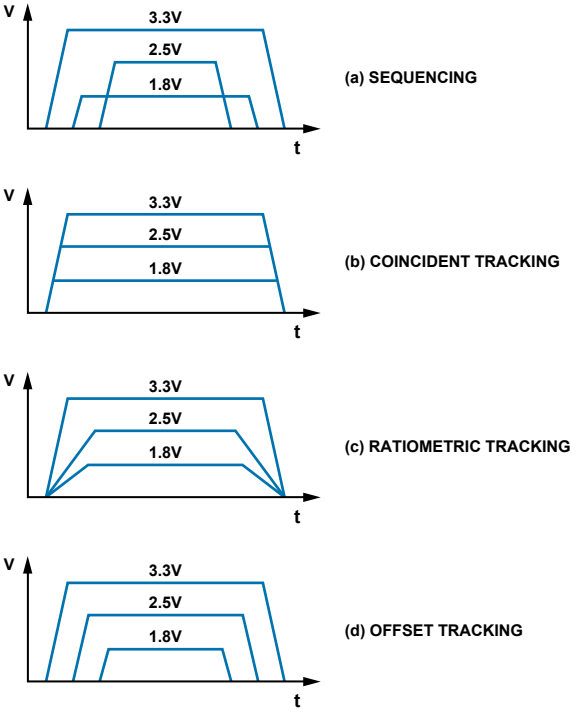

Figure 1. Types of power rail control.

Power Supply Sequencing and Tracking

Power supply *sequencing* entails turning supplies on or off in a specific order. Control of the supply sequence can be simply based on an established time order, or the turn-on time of a supply may depend on another supply reaching a programmed threshold. Power supply *tracking* is based on the fact that power supplies cannot (and generally should not) provide instantaneous changes in their voltage; this can be used advantageously by power system designers in controlling the *slew rate* of each of the various supplies in relation to other supplies in the system. Supply tracking falls into three categories: *coincident*, *ratiometric*, and *offset*. Figure 1 shows four graphs comparing sequencing, coincident tracking, ratiometric tracking, and offset tracking.

In Figure 1a, the sequence of turning the three supplies on and off is timed. Here the 3.3-V supply comes up first, and the delay-times for subsequent supplies to turn on and off depend on the needs of the application. This simple sequencing technique can ensure that the maximum ratings of active components are not exceeded if those ratings require that supplies be activated in a specific order. An example of this would be the need to guarantee that an ADC's power supply is present before the amplifier that drives it is powered up—where failure to make this provision could result in damage to the ADC's front end.

In Figure 1b, *coincident* tracking, all three supplies are turned on at the same time and brought up tracking one another at the same rate, so that the lowest supply voltages are established before higher ones are applied. Power-down is done in the reverse manner. This is a good example of how supplies might be brought up in older FPGA or microprocessor applications, where lower core voltages should be active before auxiliary or I/O supplies are brought up. An example of coincident tracking for a Xilinx Virtex-5 FPGA is shown later in this article.

In Figure 1c, the supplies are brought up at different slew rates. As noted earlier, the ability to control the slew rate, dV/dt, of supplies is very useful to prevent damage from large, decoupling-capacitor inrush currents (charging currents) in the circuit. Inrush currents can greatly exceed normal operating currents if not contained. Slew-rate limiting can prevent latch-up of active devices, shorting of capacitors, potential damage to PCB tracks, and blowing of in-line fuses.

In Figure 1d, the supplies all have the same slew rate, but their times of application are determined by predetermined offset voltages. This type of tracking is appropriate for devices that require the difference between the supply voltages to be limited; often appearing in the maximum rating sections of mixed-signal components such as DACs and ADCs. This approach can prevent permanent damage to the parts.

FPGA-Based Design Example

The powering of a system that uses an FPGA provides an excellent object lesson on the subject of handling multiple supply systems. Proper control of FPGA supplies can make the difference between a reliable, repeatable design, and a possibly catastrophic failure in the lab or, worse, in the field. Most FPGAs have multiple rails, commonly labeled V_{CCO}, V_{CCAUX}, and V_{CCINT}. These supplies are respectively used to power the FPGA core, *auxiliary circuits* (such as clocks and PLLs), and *interface logic*.

The considerations for these power supply rails can be categorized as:

- Sequencing of the rails
- Tolerance requirements for the rail voltages
- The possible need for soft start, or slew-rate control, of the supplies.

As an illustrative example, consider the power supply requirements for the Xilinx Virtex-5 family of FPGAs, a family that offers a wide range of features—including logic programmability, signal processing, and clock management. According to the data sheet, the Virtex-5 requires a power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. The ramp times for these supplies relative to ground are 200 µs min to 50 ms max. The recommended operating conditions are shown in Table 1.

The Virtex-5, as noted earlier, requires coincident voltage tracking. In addition, the supplies must fall within specific recommended operating tolerances—and also must ramp up and down within specified ranges of *dV*/*dt*.

But the FPGA is only part of a larger system. To elaborate on this example, assume that there is a high-current, 5-V, main system rail. The 1-V supply that powers the FPGA core has a tolerance of ±5% (±50 mV) and is required to deliver currents up to 4 A. The 3-V supply is a general logic supply with a ±5% tolerance and, in this example, is required to supply 4 A to power the FPGA I/O and other logic devices in the design. The 2.5-V supply is an analog supply that must deliver 100 mA with low noise.

A good solution for this application employs the ADP1850 dual buck controller for the 1-V and 3-V high-current supplies. Among the ADP1850's features are soft-start control, coincident tracking, and the ability to sequence a slave supply from a master supply. Power-on ramp-up rates are controlled by capacitors on the SS1 and SS2 pins. In this example, the 3-V digital supply is the master supply. For the 2.5-V analog supply, an ADP150 ultralow noise low-dropout regulator (LDO) is an excellent choice; it can be sequenced from the ADP1850's PGOOD2 signal. A simplified diagram of the system, showing the general flow of sequencing, appears in Figure 2 (for full details, see the ADP1850 data sheet).

The above example illustrates a common use of sequencing and tracking; it can be extended to many of today's multiple-supply systems, including microprocessor-based systems and those that involve mixed-signal technologies—with ADCs and DACs.

Analog Voltage and Current Monitoring (ADM1191)

For high-reliability applications that require precise *monitoring* of multiple system power-supply currents and voltages, easy-to-deploy analog monitoring circuits are available. For example, the ADM1191 digital power monitor, with 1% measurement accuracy, includes a 12-bit ADC for current and voltage readback, a precision current-sense amplifier, and an ALERTB output that provides an overcurrent interrupt. Figure 3 shows the ADM1191 in an application with a host controller, such as a microprocessor or microcontroller.

Table 1. Xilinx Virtex-5 Power Rail Requirements

	Voltage Range	Voltage Min/Max	Current	Start-Up Time (Min)	Start-Up Time (Max)	
V_{CCINT}	1 V ± 5%	−0.5 V to +1.1 V	4 A	200 µs	50 ms	On before V_{CCAUX}/V_{CCO}
V_{CCAUX}	2.5 V ± 5%	−0.5 V to +3.0 V	~50 mA	200 µs	50 ms	On before V_{CCO}
V_{CCO}	3 V ± 5%	−0.5 V to +3.75 V	<50 mA	200 µs	50 ms	

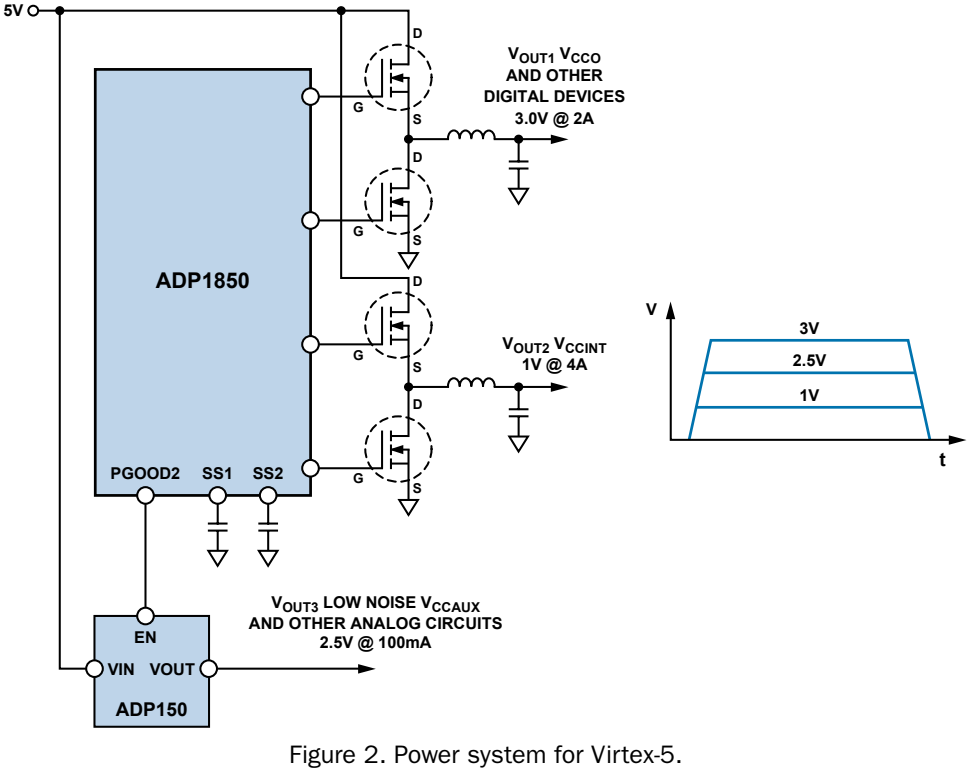

Figure 2. Power system for Virtex-5.

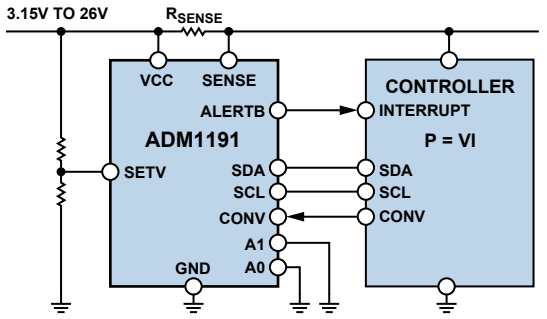

Figure 3. A simple power-supply voltage and current monitor.

The ADM1191 communicates over the I²C bus to the host controller. A total of 16 devices can be addressed in the same system by configuring the logic input levels of their A0 and A1 pins. The local controller can compute the power consumption on the rail by multiplying together the measured voltage and current. The ALERTB signal gives quick notification of an overcurrent condition via an interrupt to the controller—a rapid warning of a fault condition to help protect the system from damage.

Combining Sequencing and Monitoring

Large fixed systems, and even some high-performance plug-in cards, have many power rails that need to be controlled and monitored. Figure 4 deals with a complex power system that has eight supply rails. The heart of the system is an ADM1066, a flexible highly integrated Super Sequencer® that provides complete power control. Features include sequencing, monitoring, margining, and programmability. Other devices in the ADM106x family add temperature monitoring and a watchdog function.

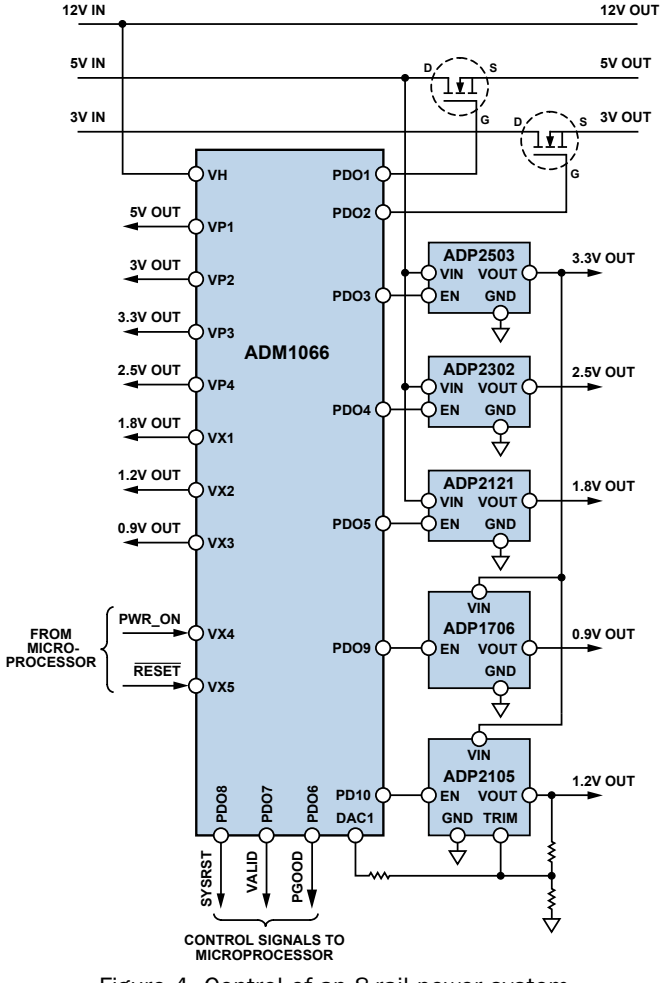

Figure 4. Control of an 8-rail power system.

The 8-rail system has three main power rails: 12 V, 5 V, and 3 V. The other rails are derived from these using switching regulators and LDOs. Each of the regulators has an enable input that is driven by one of the 10 *programmable driver* (PD) outputs of the ADM1066, thus allowing the user to bring all the power rails up in a controlled sequence. The ADM1066 has an on-board charge pump to step up six of the PD output voltages to provide a high-voltage drive for external N-MOSFETS that act as power-rail switches in cases where it is necessary to control higher-voltage supplies.

The ADM1066 has on-board EEPROM to store power system control parameters. Device configuration is facilitated with a utility program available from Analog Devices, Inc. This makes the task of getting up and running much easier, eliminating time-consuming code development. As a system evolves and new parts are added to the design, adjustments to supply sequences are easily handled. Timing parameters and voltage trip points are easily reprogrammed. This valuable feature saves development time and reduces the risk of possible board spins.

The digital output signals—PWRGD (power good), VALID, and SYSRST (system restore)—are generated by the ADM1066 to inform the system microcontroller of the status of the power system, either when polled or via interrupts or digital inputs, so that action can be taken if fault conditions exist. Such quick notification can prevent catastrophic damage from shorted capacitors and other dangerous conditions. PWR_ON and $\overline{\text{RESET}}$ are digital inputs to the ADM1066 from the system controller, completing the overall system control loop.

Supply Margining with the ADM1066

The on-chip DACs of the ADM1066 are useful for performing supply margining during system development, when it is necessary for the designer to adjust supply voltages, either to optimize their levels or move them away from nominal values. This margining feature allows a system to be fully characterized over supply limits without the use of external instrumentation. The function is typically performed during an in-circuit test (ICT), for example, when a manufacturer wants to guarantee that a product under test functions correctly at nominal supply voltages within limits of ±5%. Starting with the circuit in Figure 4, the user can implement margining on many of the supply rails.

Open-Loop Supply Margining

The simplest method of margining a supply, such as a dc-to-dc converter or an LDO, is to switch extra resistors into the feedback node of the power module to alter the voltage at the feedback or trim node, forcing the output voltage to margin up or down by the desired amount using a DAC. With such an attenuator in place (Figure 5), the ADM11066 can be remotely commanded to margin a supply, using the SMBus, by updating the values on the relevant DAC output. The process can be implemented using an open-loop technique, independently of the system control loop.

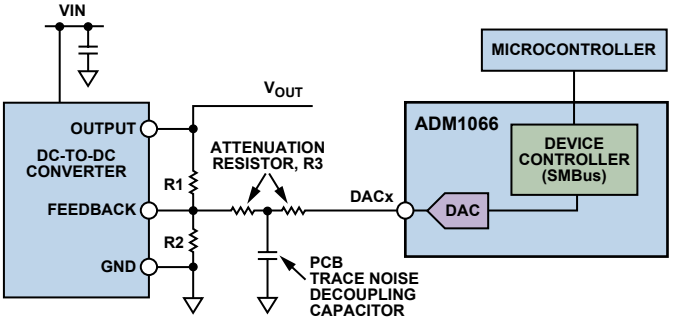

Figure 5. Open-loop margining.

The ADM1066 can perform open-loop margining for up to six supplies, using the six on-board voltage-output DACs (DAC1 to DAC6) to drive into the feedback pins of the power modules being margined. The simplest circuit to implement this function is an attenuation resistor (R3) that connects the DACx pin to the feedback node of a dc-to-dc converter. When the DACx output voltage is set equal to the feedback voltage, no current flows into the attenuation resistor, and the dc-to-dc converter output voltage does not change. Taking DACx above the feedback voltage forces current into the feedback node, and the output of the dc-to-dc converter must fall to compensate for this. To raise the dc-to-dc converter output, the DACx output voltage is set lower than the feedback node voltage. For noise reduction, as shown here, the series resistor can be split into two resistors, and the node between them can be decoupled with a capacitor to ground at the dc-to-dc converter.

Closed-Loop Supply Margining

A more accurate and comprehensive method of margining uses a similar circuit in a closed-loop system. An example is shown in Figure 4 for the 1.2-V output. The voltage on the rail to be margined can be read back via VX2 to accurately margin the rail to the target voltage. The ADM1066 incorporates all the circuits required to do this, with the 12-bit successive-approximation ADC reading the level of the supervised voltages, and the six voltage-output DACs adjusting supply levels as described above. These circuits can be used along with other intelligence, such as a microcontroller, to implement a closed-loop margining system that allows any dc-to-dc converter or LDO supply to be set to any voltage, accurate to within ±0.5% of the target.

To implement closed-loop margining on the rail to be tested, use the following steps:

1. Disable the six DACx outputs.
2. Set the DACx output voltage equal to the voltage on the feedback node.
3. Enable the DAC.
4. Read the voltage at the dc-to-dc converter output that is connected to one of the VPx, VH, or VXx pins.
5. If necessary, modify the DACx output voltage up or down to adjust the dc-to-dc converter output voltage. Otherwise stop; the target voltage has been reached.
6. Set the DAC output voltage to a value that alters the supply output by the required amount (for example, ±5%).
7. Repeat the process until the required voltage for that rail is reached.

Steps 1 to 3 ensure that when each DACx output buffer is turned on, it has little immediate effect on the dc-to-dc converter output. The DAC output buffer is designed to power up without transient "glitches" by first powering up the buffer to follow the pin voltage. It does not drive the pin at this time. Once the output buffer is properly enabled, the buffer input is switched over to the DAC, and the output stage of the buffer is turned on, all but eliminating output glitching.

Synchronization of Switching Regulators

In systems with multiple rails that use more than one switching regulator or controller, the possibility exists for these devices to interact due to differences in their internal switching frequencies. This can cause beat harmonics that can greatly increase supply noise and wreak havoc with EMI testing. Fortunately, many switching controllers and regulators are designed to allow their internal clocks to be synchronized. LDOs do not share this problem, but it is not always desirable to use them due to their limited current output and, in most cases, poor efficiency.

The ADP2116 dual switching regulator is a good example of a synchronizable device. Its SYNC/CLKOUT pin can be configured as an input SYNC pin or an output CLKOUT pin via the SCFG pin. As an input SYNC pin, it synchronizes the ADP2116 to an external clock; the two channels switch at half the external clock frequency and are 180° out of phase with one another.

As a CLKOUT pin, it provides an output clock that is twice the switching frequency of the channels and 90° out of phase. Thus a single ADP2116 configured for the CLKOUT option can act as the master converter and provide an external clock for all other dc-to-dc converters—including other ADP2116 devices (Figure 6). Configured as slaves, they accept the master's external clock and synchronize to it. By synchronizing all dc-to-dc converters in the system, this approach prevents beat harmonics that can lead to EMI issues.

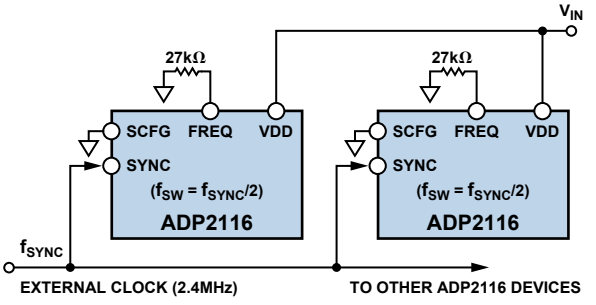

Figure 6. Synchronizing ADP2116s from an external clock.

Conclusion

This article discusses ways of handling multiple power supply systems. The high level of functional integration provided by sequencers, monitors, regulators, and controllers enables designers to address potential power problems without employing a board full of discrete ICs—a capability that provides designers with good value and increases the odds of successful designs with minimal redesigns and board spins.

References

Moloney, Alan. "Power Supply Management—Principles, Problems, and Parts." *Analog Dialogue*. 40-2. May 2006.

Author

Rich Ghiorse [rich.ghiorse@analog.com] started with ADI in 1980. He has worked in various disciplines, from product- and test- to design-, and now, applications engineering. He holds BSEE and MSEE degrees from Northeastern University. Currently, Rich is a senior applications engineer in the Analog Devices Customer Interaction Center in Wilmington, Massachusetts.