Power Management Design for PLLs

By Austin Harney and Grzegorz Wawrzola

Abstract

The phase-locked loop (PLL) is a fundamental building block of modern communication systems. PLLs are typically used to provide the local-oscillator (LO) function in a radio receiver or transmitter; they are also used for clock-signal distribution and noise reduction—and, increasingly, as the clock source for high-sampling-rate analog-to-digital or digital-to-analog conversion.

As the noise performance of PLLs is improving with each generation, the impact of power supply noise is becoming increasingly evident, and can even limit noise performance in some cases.

This article considers the basic PLL scheme shown in Figure 1 and examines the power-management requirements for each building block.

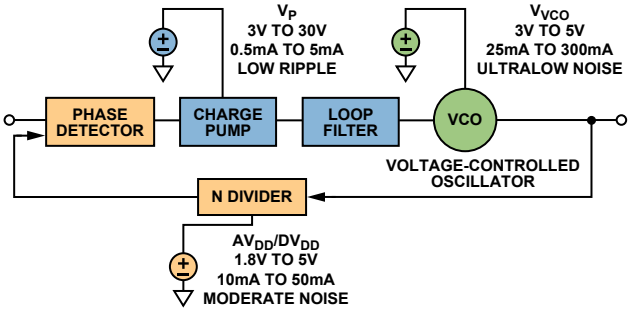

Figure 1. A basic phase-locked loop showing the various power-management requirements.

In a PLL, the feedback control loop drives a voltage-controlled oscillator (VCO) to make the oscillator frequency (or phase) accurately track a multiple of an applied reference frequency. Many good references, for example, Best's *Phase-Locked Loops*,[1] explain the mathematical analysis of the PLL; and simulation tools, such as Analog Devices' ADIsimPLL™, can be helpful in understanding the loop transfer functions and calculations. Let us now look at the PLL building blocks in turn.

The VCO and VCO Pushing

The *voltage-controlled oscillator* converts the error voltage from the phase detector into an output frequency. Its "gain," defined as K_{VCO}, is usually specified in MHz/V. A voltage-controlled variable-capacitance diode (*varactor*) is often used to adjust frequency in VCOs. The gain of the VCO is usually large enough to provide adequate frequency coverage, but not so large as to degrade phase noise—since any varactor noise will be amplified by K_{VCO} and contribute to output phase noise.

The advent of multiband integrated VCOs, such as that used in the ADF4350 frequency synthesizer with integrated VCO, obviates the trade-off between K_{VCO} and frequency coverage, allowing the PLL designer to use an IC containing several moderate-gain VCOs, with intelligent band switching routines to select the appropriate band, depending on the programmed output frequency. This partitioning of the frequency band provides wide overall range *and* lower noise.

In addition to the desired translation from input voltage change to output frequency change (K_{VCO}), power-supply variation can produce an unwanted component of output frequency change. The sensitivity of the VCO to power-supply variation is defined as the *VCO pushing* ($K_{pushing}$), usually a fraction of the wanted K_{VCO}. For example, $K_{pushing}$ is usually 5% to 20% of K_{VCO}. Thus, for high-gain VCOs, the pushing effect becomes larger, and the noise contribution from the VCO supply source becomes more critical.

VCO pushing is measured by applying a dc tuning voltage to the VTUNE pin, varying the power supply voltage, and measuring the frequency change. The pushing figure is the ratio of frequency change to voltage change, as shown in Table 1, using the ADF4350 PLL.

Table 1. ADF4350 VCO Pushing Measurements

VCO Band (MHz)	V_{tune} (V)	f_1 (MHz) at V_{VCO} = 3 V	f_2 (MHz) at V_{VCO} = 3.3 V	$K_{pushing} = \Delta f/\Delta V$ (MHz/V)
2200	2.5	2233.446	2233.061	1.28
3300	2.5	3331.112	3331.799	2.3
4400	2.5	4462.577	4464.242	5.55

Another method, mentioned in Reference 2, is to dc-couple a low-frequency square wave into the supply, while observing the *frequency-shift-keyed* (FSK) modulation peaks on either side of the VCO spectrum (Figure 2). The frequency deviation between the peaks divided by the amplitude of the square wave yields the VCO pushing number. This can be a more accurate measure than the static dc test, as it removes any thermal effects associated with a change in dc input voltage. Figure 2 shows a spectrum analyzer plot of the ADF4350 VCO output at 3.3 GHz with a 10 kHz, 0.6 V p-p square wave applied to the nominal 3.3-V supply. The resulting deviation is 3326.51 MHz – 3324.89 MHz = 1.62 MHz, for a pushing number of 1.62 MHz/0.6 V or 2.7 MHz/V. This compares to the static measure of 2.3 MHz/V given in Table 1.

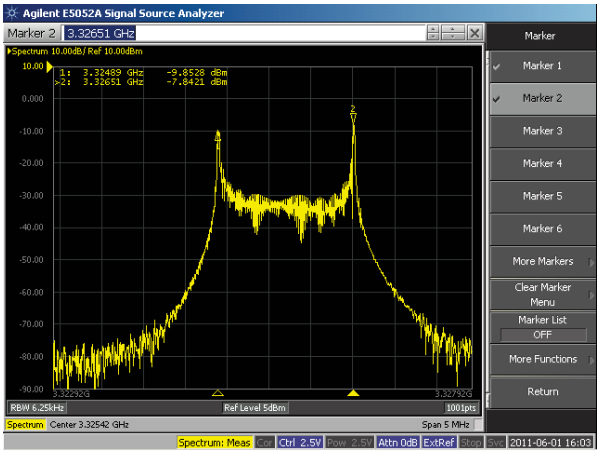

Figure 2. A spectrum-analyzer plot of ADF4350 VCO response to supply modulation by a 10-kHz, 0.6-V p-p square wave.

In a PLL system, higher VCO pushing means greater multiplication of VCO power-supply noise. A low-noise power supply is required to minimize the impact on VCO phase noise.

Reference 3 and Reference 4 provide good examples of how different low-dropout regulators (LDOs) can affect PLL phase-noise. For example, a comparison was made between the ADP3334 and ADP150 LDOs in powering an ADF4350. The integrated rms noise of the ADP3334 regulator is 27 µV (over four decades,

from 10 Hz to 100 kHz). This compares to 9 µV for the ADP150, the LDO used on the ADF4350 evaluation board. The difference in measured PLL phase-noise spectral density can be seen in Figure 3. The measurement was taken with a 4.4-GHz VCO frequency, where the VCO pushing was maximum (Table 1), so this is a worst-case result. The ADP150 regulator noise was low enough so that its contribution did not measurably add to the VCO noise, as was confirmed by repeating the measurement with two (presumably "noiseless") AA batteries.

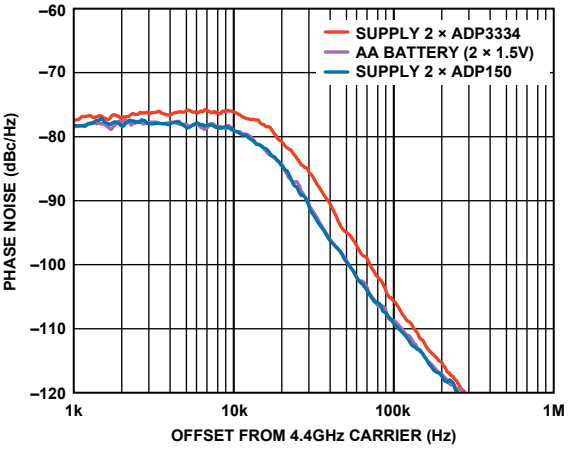

Figure 3. ADF4350 phase noise comparison at 4.4 GHz when powered with pairs of ADP3334 and ADP150 LDOs—and AA batteries.

Figure 3 emphasizes the importance of a low-noise power source for the ADF4350, but how do you specify the noise requirement of the power supply or LDO?

In a manner similar to VCO noise, the phase noise contribution of the LDO can be modeled as an additive component, $\Phi_{LDO}(t)$, as shown in Figure 4. Reusing the VCO excess phase expression yields:

$$\Phi_{LDO}(t) = K_{pushing} \int V_{LDO}(t)dt$$

or, in the frequency domain

$$\Phi_{LDO}(f) = \frac{K_{pushing} v_{LDO}(f)}{f}$$

where $v_{LDO}(f)$ is the voltage noise spectral density of the LDO.

The single-sideband power spectral density $S\Phi(f)$ in a 1-Hz bandwidth is given by

$$S\Phi(f) = \Phi^2{}_{LDO}(f)/2$$

Expressing this in dB, the formula for calculating the phase noise contribution due to the power supply noise is:

$$L_{LDO} = 10\log\left[\frac{(K_{pushing} \times v_{LDO}(f))^2}{2 \times f^2}\right]$$

$$L_{(LDO)} = 20\log\left[\frac{K_{pushing} \times v_{LDO}(f)}{\sqrt{2} \times f}\right] \quad (1)$$

where $L_{(LDO)}$ is the noise contribution from the regulator to the VCO phase noise (in dBc/Hz), at an offset f; $K_{pushing}$ is the VCO pushing figure in Hz/V; and $v_{LDO}(f)$ is the noise spectral density at a given frequency offset in V/√Hz.

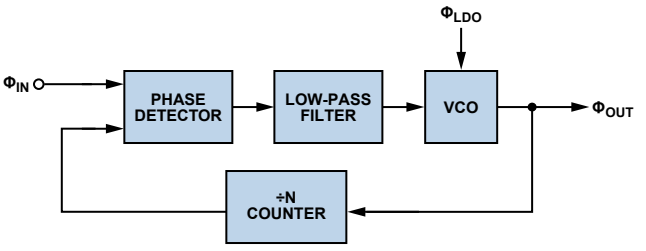

Figure 4. Small-signal additive VCO supply noise model.

In a free-running VCO, the total noise is the *root-sum-square* (rss) of L_{LDO} and the VCO noise. Thus, expressed in dB:

$$L_{TOTAL} = 10\log\left[\log^{-1}\left(\frac{L_{LDO}}{10}\right) + \log^{-1}\left(\frac{L_{VCO}}{10}\right)\right]$$

For example, consider a VCO with a pushing number of 10 MHz/V and a measured phase noise of –116 dBc/Hz at 100 kHz offset: what is the required noise spectral density of the power supply so as to not degrade the VCO noise performance at 100 kHz? The supply noise and VCO noise add as the root-sum-square, so the supply noise should be at least 6 dB less than the VCO noise to minimize its contribution. Thus, L_{LDO} should be less than –122 dBc/Hz. Using Equation 1,

$$\log^{-1}\left(-\frac{122}{20}\right) = \frac{10\ \text{MHz/V} \times v_{LDO}(f)}{\sqrt{2} \times 100\ \text{kHz}}$$

solving for $v_{LDO}(f)$,

$$v_{LDO}(f) = 11.2\ \text{nV}/\sqrt{\text{Hz}}\ \text{at 100-kHz offset}$$

The LDO noise spectral density at a given offset can usually be read from the LDO data sheet's typical performance curves.

When the VCO is connected in a negative-feedback PLL, the LDO noise, L_{LDO}, is high-pass filtered by the PLL loop filter, in a similar manner to VCO noise. Thus, the above formula only applies to frequency offsets greater than the PLL loop bandwidth. Within the PLL's loop bandwidth, the PLL can successfully track and filter the LDO noise, reducing its contribution.

LDO Filtering

To improve LDO noise, there are typically two choices: use an LDO with less noise or post-filter the LDO's output. The filtering option can be a good choice when the noise requirements without a filter are beyond the capability of affordable LDOs. A simple LC π-filter is often sufficient to reduce out-of-band LDO noise by 20 dB (Figure 5).

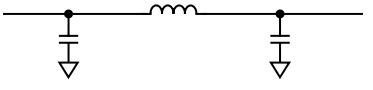

Figure 5. LC π-filter to attenuate LDO noise.

Care is needed in the choice of components. A typical inductor will be in the microhenry range—with a ferrite core—so it is necessary to consider its *saturation current* (I_{SAT}), specified in inductor data sheets as the dc current level at which the inductance drops by 10%. The current drawn by the VCO should be less than I_{SAT}. *Effective series resistance* (ESR) is also a concern, as this will cause an IR drop across the filter. For a microwave VCO drawing 300-mA dc, an inductor with ESR less than 0.33 Ω would be needed to yield an IR drop of less than 100 mV. A low, but nonzero, ESR is also desirable to damp the filter response and improve LDO stability. It can be practical to choose a capacitor with very low parasitic

ESR and add a dedicated series resistor for this purpose. This can all be simulated easily in SPICE using a downloadable component evaluator such as NI Multisim™.

Charge Pump and Filter

The charge pump converts the phase detector error voltage into current pulses, which are integrated and smoothed by the PLL loop filter. The charge pump can typically operate at up to 0.5 V below its supply voltage (V_P). For example, if the maximum charge pump supply is 5.5 V, the charge pump could only operate at an output voltage up to 5 V. If the VCO requires higher tuning voltages, an active filter is typically required. Useful information and a reference design of an actual PLL can be found in Circuit Note CN-0174,[5] and ways of dealing with high-voltage are discussed in "Designing High-Performance Phase-Locked Loops with High-Voltage VCOs,"[6] which appeared in *Analog Dialogue* Volume 43, Number 4 (2009). The alternative to an active filter is to use a PLL with a charge pump designed for higher voltage, such as the ADF4150HV. The ADF4150HV can operate with charge-pump voltages as high as 30 V, thus avoiding the need for active filters in many cases.

The low current drawn by the charge pump makes it look attractive to use a boost converter to generate the high charge-pump voltage from a lower supply voltage, but the switching-frequency ripple associated with this type of dc-to-dc converter could produce unwanted spurious tones at the output of the VCO. High PLL spurs can potentially cause failure of a transmitter emission mask test or degrade sensitivity and out-of-band blocking in a receiver system. To help guide the specification of converter ripple, a comprehensive power supply rejection plot vs. frequency was taken for various PLL loop bandwidths, using the measurement setup of Figure 6.

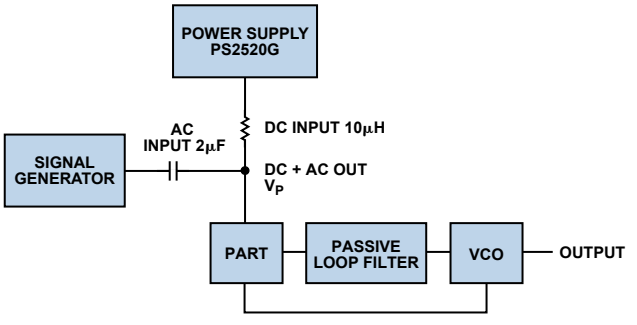

Figure 6. Setup for measuring charge pump power-supply rejection.

A ripple signal of 17.4 mV (–22 dBm) was ac-coupled to the power supply voltage and swept over a frequency range. At each frequency the spurious level was measured and the PSR calculated as the difference in dB between the –22-dBm input and the spurious output level. The 0.1-µF and 1-nF charge pump supply decoupling capacitors, which were left in place, provided some attenuation of the coupled signal, so the signal level at the generator was increased until 17.4 mV was measured directly at the pin at each frequency point. The results are shown in Figure 7.

The power supply rejection gets worse initially as the frequency increases within the PLL loop bandwidth. As the frequency approaches the PLL loop bandwidth, the ripple frequency gets attenuated in a similar manner to reference noise, and PSR improves. This plot shows that a boost converter with higher switching frequency—ideally greater than 1 MHz—is desirable to minimize switching spurs. Also, the PLL loop bandwidth should be minimized wherever possible.

With a switching speed of 1.3 MHz, the ADP1613 is a good example of a suitable boost converter. With the PLL loop bandwidth set to 10 kHz, a PSR of about 90 dB is possible; with a loop bandwidth of 80 kHz, the PSR is 50 dB. Starting with the PLL spurious level requirements, one can work backward to determine the ripple level needed at the boost converter output. For example, if the PLL requires spurs less than –80 dBm, and the PSR is 50 dB, then the ripple power at the input to the charge pump supply needs to be less than –30 dBm, or 20 mV p-p. These levels of ripple voltage can easily be achieved with ripple filters, if sufficient decoupling capacitance is placed close to the charge pump supply pin. For example, a 100-nF decoupling capacitor provides more than 20 dB of ripple attenuation at 1.3 MHz. Care should be taken to use capacitors with the appropriate voltage rating; for example, if the boost converter generates an 18-V supply, use capacitors with a 20-V or higher rating.

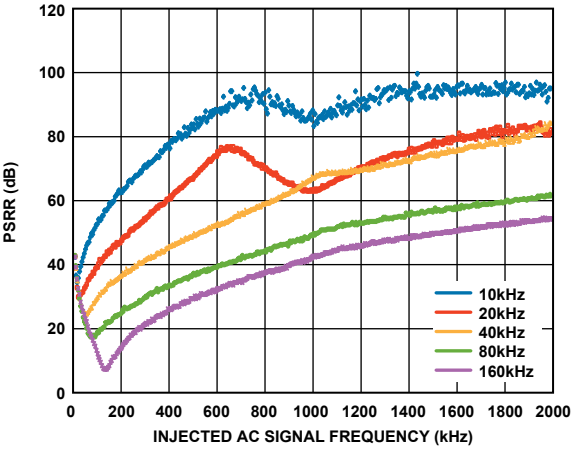

Figure 7. ADF4150HV charge pump power-supply rejection plot.

Design of the boost converter and ripple filter is simplified using the ADP161x Excel-based design tool. Figure 8 shows the user inputs for an illustrative 5-V in to 20-V out design. To minimize voltage ripple at the output of the converter stage, the noise filter option was selected, and the V_{OUT} ripple field was set to its minimum. The current drawn by the high-voltage charge pump is 2 mA maximum, so an I_{OUT} of 10 mA was typed in to provide margin. This design was tested with the ADF4150HV evaluation board, using a PLL loop bandwidth of 20 kHz. From Figure 7, a PSR of about 70 dB might be expected. Due to the excellent PSR, this setup showed no evident switching spurs (< –110 dBm) at the VCO output—even when the noise filter was omitted.

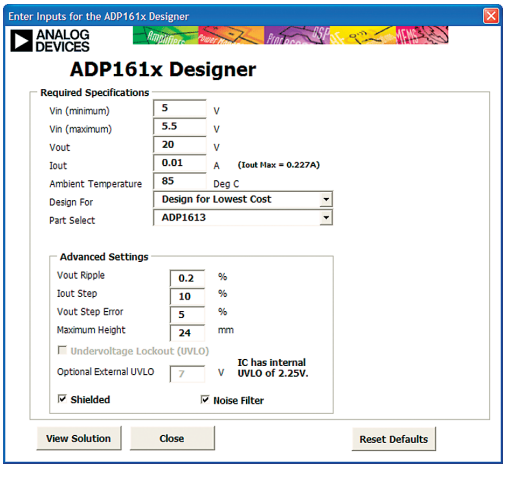

Figure 8. ADP1613 boost converter Excel design tool.

As a final experiment, the PSR of the high-voltage charge pump was compared to that of an active filter, the topology most commonly used today to generate high VCO tuning voltages. To make the measurement, an ac signal with an amplitude of 1 V p-p is injected into the charge pump supply (V_P) of the ADF4150HV, using a passive loop filter—as in the measurement setup in Figure 6. The same measurement is repeated with an active filter in place of the passive filter of equal bandwidth. The active filter used was type CPA_PPFFBP1, as described in ADIsimPLL (Figure 9).

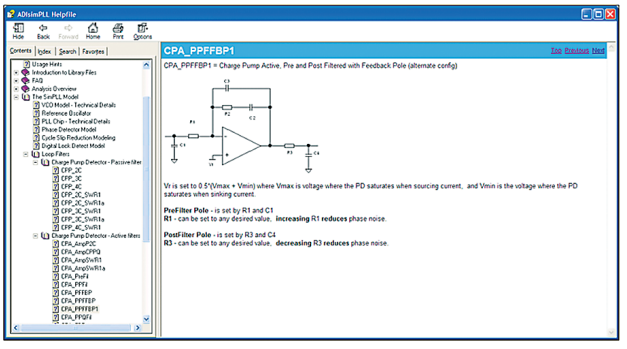

Figure 9. Screen view of CPA_PPFFBP1 filter design in ADIsimPLL.

Decoupling is the same on the charge pump and op amp supply pins, to provide a fair comparison—10 µF, 10 nF, and 10 pF capacitors in parallel. The measured result is plotted in Figure 10: the high-voltage charge pump has a 40-dB to 45-dB reduction in switching spur level when compared to the active filter. The improved spur levels with the high-voltage charge pump can be partially explained by the smaller loop filter attenuation seen by the active filter, where the injected ripple is after the first pole, in contrast to the passive filter, where the injected ripple is at the input.

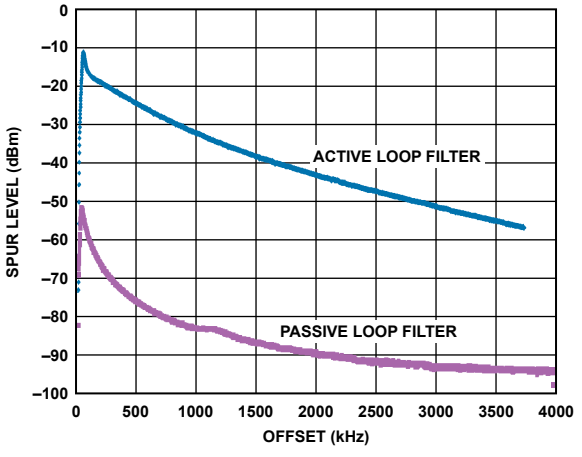

Figure 10. Power supply ripple level for active loop filter vs. high-voltage passive filter.

A final note: the third power rail shown in Figure 1—the divider supply, AV_{DD}/DV_{DD}—has less stringent supply requirements compared to the VCO and charge pump supply, as the RF sections of the PLL (AV_{DD}) are typically bipolar ECL logic stages with stable band-gap-referred bias voltages, and so are relatively supply immune. Also, by their nature, the digital CMOS blocks (DV_{DD}) are more immune to power supply noise. Thus, it is advisable to choose a medium performance LDO that meets both the voltage and current requirements for this rail and apply sufficient decoupling close to all power pins; 100 nF in parallel with 10 pF is usually sufficient.

Conclusion

The power-management requirements for the main PLL blocks were discussed, and specifications were derived for the VCO and charge pump supplies. Analog Devices provides multiple design-in support tools for power management and PLL ICs, including reference circuits and solutions, and simulation tools like ADIsimPLL and ADIsimPower. With an understanding of the impact of power supply noise and ripple on PLL performance, designers can work back to derive specifications for power management blocks and achieve PLL designs with the best possible performance.

References

[1]Best, Roland E. *Phase Locked Loops*: *Design, Simulation, and Applications*. 6th edition. 2007. McGraw-Hill. ISBN 9780071493758.

[2]Colin, Dennis. *Externally Induced VCO Phase Noise*. Micronetics, Inc. Reprint: *Microwave Journal*. Feb 2002.

[3]http://www.radio-electronics.com/analysis/rf-technology-design/2010-11/integrated-plls-vcos-02.php.

[4]Circuit Note CN-0147, *Powering a Fractional-N Voltage-Controlled Oscillator (VCO) with Low Noise LDO Regulators for Reduced Phase Noise*. Analog Devices. 2010.

[5]Circuit Note CN-0174, *Low Noise, 12 GHz, Microwave Fractional-N Phase-Locked Loop (PLL) Using an Active Loop Filter and RF Prescaler*. Analog Devices. 2010.

[6]Harney, Austin. "Designing High-Performance Phase-Locked Loops with High-Voltage VCO." Analog Dialogue, 43-12. 2009.

Authors

Austin Harney [austin.harney@analog.com] graduated in 1999 with a BEng from University College, Dublin, Ireland, and an MBA from the University of Limerick in 2006. For 12 years he worked in various RF roles at Analog Devices, and is currently an applications engineer for ADI's PLL and VCO product family.

Grzegorz Wawrzola [grzegorz.wawrzola@analog.com] graduated with honors in 2006 with an MSc in electronics and telecommunications from Wroclaw University of Technology, Wroclaw, Poland. He worked for five years as a design evaluation engineer for PLLs and VCOs in the RF group at Analog Devices before moving to RF applications in August 2011.