Multichannel DDS Enables Phase-Coherent FSK Modulation

By David Brandon

Common single-channel direct-digital synthesizers (DDS) produce phase-continuous frequency transitions, as shown in Figure 1. In applications such as coherent pulse Doppler radar and NMR/MRI spectrometry for medical and material analysis, however, phase-coherent transitions are preferred. This article demonstrates how to configure the AD9958/AD9959 multichannel DDS as a robust phase-coherent frequency-shift keyed (FSK) modulator by summing the DDS outputs.

A multichannel DDS virtually eliminates channel-to-channel temperature and timing issues encountered when synchronizing multiple single-channel devices. Multichannel DDS outputs, though independent, share the same system clock, allowing them to track better over temperature and power-supply deviations than the outputs of multiple single-channel devices. As a result, a multichannel DDS is better suited for producing phase-coherent frequency transitions at the summed output.



Figure 1. Phase-continuous and phase-coherent frequency transitions.

Circuit Description

The AD9520 clock distribution device drives the AD9958 DDS with a high-performance reference clock, while providing the same clock to the source for the FSK data stream. The AD9520 provides multiple output logic choices and adjustable delays to meet setup- and hold times between the FSK data stream and SYNC_CLK of the multichannel DDS.

The AD9958's two independent channels operate at preprogrammed frequencies F1 and F2. Wiring the outputs together sums them. The profile pins, which drive the multiplier at each DAC input to control the output amplitude, switch the channel outputs on or off to select the desired frequency. To accomplish this, each multiplier has two preprogrammed profile-selectable settings, zero- and

full scale. Logic low on the profile pins shuts off the sine wave while logic high passes it to the output. The operation requires two complementary input data streams to alternate between frequencies. Note that the two DDS channels continuously generate F1 and F2. The off feature mutes the appropriate DDS output, thereby producing a phase-coherent FSK signal.



Figure 2. Setup for phase-coherent FSK modulator.

The AD9959 4-channel DDS produced the results shown in Figure 3. Its two additional channels serve as a phase reference for the two switched frequencies at the summed output, making it easier to demonstrate the phase-coherent switching. The summed output, shown in the upper trace, exhibits phase-coherent switching. The middle two traces show reference signals F1 and F2. The bottom trace shows the pseudo-random sequence (PRS) data stream that selects between the two frequencies. Note the edges of the PRS data stream do not align exactly with the frequency transitions of the summed outputs due to the pipeline delay within the device.



Figure 3. Measured phase-coherent FSK transition.

Figure 4 shows an example of phase-continuous FSK switching, also produced by the AD9959. This type of operation requires less bandwidth, but does not maintain phase memory between transitions.



Figure 4. Measured phase-continuous FSK transition.

Analog Devices offers a variety of direct digital synthesizers, clock distribution chips, and clock buffers to build a DDS-based clock generator. Refer to www.analog.com/dds and www.analog.com/ clock for more information.

Multichannel, 10-Bit, 500-MSPS Direct Digital Synthesizers

The 2-channel AD9958 (Figure 5) and 4-channel AD9959 direct digital synthesizers (DDS) include two/four 10-bit, 500-MSPS current-output DACs. All channels share a common system clock, providing inherent synchronization; interconnecting multiple devices enables higher channel counts. Independent control of each channel's frequency, phase, and amplitude allows the devices to correct for system-related mismatches. All parameters can be swept linearly; or 16 levels can be chosen for FSK, PSK, or ASK modulation. Output sine wave tuning has 32-bit frequency resolution, 14-bit phase resolution, and 10-bit amplitude resolution. Operating with a 1.8-V core supply, plus a 3.3-V I/O supply for logic compatibility, the AD9958/AD9959 consume 315 mW/540 mW with all channels *on*, and 13 mW in *power-down* mode. Specified from -40° C to $+85^{\circ}$ C, they are available in 56-lead LFCSP packages and priced at \$20.48/\$37.59 in 1000s.



Figure 5. AD9958 functional block diagram.

Clock Generator Has 12 LVPECL/24 CMOS Outputs

The AD9520-x clock generator (Figure 6) derives up to 12 LVPECL or 24 CMOS clocks from a single reference frequency. Integrating a complete PLL with VCO, programmable dividers,

and configurable output buffers, it performs with subpicosecond jitter. Four options provide an on-chip VCO with center frequencies ranging from 1.45 GHz to 2.95 GHz; a fifth option operates with an external VCO at frequencies up to 2.4 GHz. Accepting one differential- or two single-ended references, at frequencies up to 250 MHz, the devices provide four groups of three LVPECL clocks at frequencies up to 1.6 GHz. Programmable dividers, with a divide ratio of 1 to 32, set the output frequency and the coarse delay for each group. Each LVPECL output can be reconfigured to provide two 250-MHz CMOS outputs. Operating on a single 3.3-V supply, the AD9520-x consume 1.5 W max; separate output-driver and charge-pump supplies can be used for logic compatibility and to support VCOs having an extended tuning range. Available in 64-lead LFCSP packages, they are specified from -40° C to $+85^{\circ}$ C and priced at \$12.65 in 1000s.



Figure 6. AD9520 functional block diagram.

Further Reading

- 1. AN-837 Application Note, DDS-Based Clock fitter Performance vs. DAC Reconstruction Filter Performance.
- 2. Kester, Walt. *The Data Conversion Handbook*. Analog Devices. Chapters 6 and 7. 2005.
- 3. Kester, Walt. *High Speed System Applications*. Analog Devices. Chapters 2 and 3. 2006.
- 4. MT-101 Tutorial, Decoupling Techniques.
- 5. MT-031 Tutorial, Grounding Data Converters and Solving the Mystery of AGND and DGND.

Author

David Brandon [david.brandon@analog.com] has supported DDS products since the first DDS released back in 1995. His career spans 28 years at ADI, with the last 11 years as an applications engineer in the Clock and Signal Synthesis Group. He has authored a number of application notes and a couple of magazine articles.

