Differential-Output Difference Amplifier System with G = \frac{1}{2}

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Designed on small-geometry processes, high-performance ADCs typically run on a single 1.8-V to 5-V supply or dual \pm 5-V supplies. To process real-world signals of \pm 10 V or larger, the ADC is often preceded by an amplifier that attenuates the signal to keep it from saturating or damaging the ADC inputs. These amplifiers usually have single-ended outputs, but differential outputs would be preferable to capture the full benefits of the differential-input ADC, including increased dynamic range, improved common-mode rejection, and reduced noise sensitivity. Figure 1 shows a differential-output amplifier system with gain of $\frac{1}{2}$.



Figure 1. Functional block diagram of differential-output difference amplifier with $G = \frac{1}{2}$.

Differential amplifier A1 is configured for a gain of $\frac{1}{2}$. The output of this amplifier is fed into the noninverting input of amplifier A2 and the inverting input of amplifier A3. Amplifiers A2 and A3 also operate at a gain of $\frac{1}{2}$. Their outputs, 180 degrees out of phase, form a differential output. The differential output voltage, $V_{OUT}A2 - V_{OUT}A3$, is equal to $V_{IN}/4 - (-V_{IN}/4)$, or a total differential output voltage of $V_{IN}/2$, as desired.

The V_{OFFSET} terminal can be used to offset the output and increase the dynamic range of the ADC. The differential gain from V_{OFFSET} to the output is -1. Connect this node to ground if offset adjustment is not required.

The V_{CM} terminal sets the common-mode voltage of the differential output. This is particularly useful when driving single-supply ADCs, as the common-mode output of the circuit can be set to midsupply. The gain from V_{CM} to the output is 1. Connect this node to ground if common-mode adjustment is not required.

Figure 2 demonstrates the circuit's performance. The input is a 25-kHz, 20-V p-p sine wave. Channel 1 is the noninverting output; Channel 2 is the inverting output; Channel 3 is the input. The Math Channel is the difference between the two outputs. Each output is $\frac{1}{4}$ of the input signal; the two outputs are inverted with respect to each other; and their difference is $\frac{1}{2}$ of the input signal.



Figure 2. Differential output is ½ of the input signal.

Figure 3 shows the gain vs. frequency response of the circuit, demonstrating that it is stable, with less than 1-dB peaking over a 1-MHz bandwidth.



Figure 3. Frequency response of differential-output difference amplifier.

Figure 4 demonstrates that the circuit's response to large squarewave inputs has no appreciable overshoot and a quick settling time. The differential output slews twice as fast as the individual outputs because each amplifier carries only half of the signal.



Figure 4. Large-signal performance of the differential-output difference amplifier.

The AD8279¹ dual difference amplifier is available in a narrowbody 14-lead SOIC package. The AD8278² is available in an 8-lead MSOP package. Because the precision laser-trimmed resistors are integrated onto the same chip as the amplifiers, their offset, gain, common-mode errors—and drift over temperature—are minimized, making for a high-precision system. Despite the low power consumption of the AD8278 (200 μ A) and AD8279 (200 μ A per amplifier), the system has a 1-MHz bandwidth and a 2.4-V/ μ s slew rate. The AD8278 and AD8279 can operate over a very large supply voltage range, from a single 2.5-V supply to dual ±18-V supplies. The inputs can swing well beyond the supply rails, enabling them to measure large signals (±20 V or more) in the presence of large common-mode voltages and noise, making this an ideal front end for high-performance, low-voltage ADCs.

References

¹ www.analog.com/en/amplifiers-and-comparators/differenceamplifiers/ad8279/products/product.html.

² www.analog.com/en/amplifiers-and-comparators/differenceamplifiers/ad8278/products/product.html.

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