

High Speed Op Amp Drives a 16-Bit, 1-MSPS Differential-Input A/D Converter

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INTRODUCTION

Modern high resolution analog-to-digital converters (ADCs) usually require input buffer amplifiers (ADC *drivers*), because they often present a dc load of several hundred ohms or more—and a high frequency dynamic load—to the source that is driving them. If the source is a transducer or a typical low frequency preamplifier, significant errors may occur.

The ADC driver is a high performance fast-settling op amp with input impedance of (at least) several megohms and a low impedance output circuit that is capable of driving dynamic loads with minimal errors. In addition to buffering, the driver can also provide input scaling (gain) and low-pass filtering to reduce system noise. Some designs can also translate from single-ended sources to differential-input ADCs.

In order for the ADC driver to maintain system accuracy, its settling time, noise, and total harmonic distortion (THD) must be considerably better than that of the ADC itself. This is a significant challenge for the designer in systems employing fast 16- or 18-bit successive approximation (SAR-type) A/D converters.

Settling-time requirements

In order to use the full sampling rate of which an ADC is capable, the combined settling time for the op amp and ADC for a full-scale step input to within 1 LSB must be less than the ADC's specified sampling rate. This is especially critical in applications where the amplifier and ADC are acquiring diverse input values from several multiplexed sources. This window can be as short as 1 μ s when using fast, high resolution ADCs, such as the 16-bit, 1-MSPS AD7677 (true differential input) and AD7671 (true bipolar input)—or about 1.25 μ s with the 18-bit, 800-kSPS AD7674.

In the search for an amplifier to use as an ADC driver, it is unfortunate that—because of the extreme care required in measuring settling time—most op amp data sheets specify the settling time to only 0.1% or 0.01% of full scale, rather than the 0.0015% required for 16-bit accuracy—or the 0.0004% required for 18-bit accuracy. Thus, actually settling to within 1 LSB of 16 bits will normally require significantly more time than the data sheet specification. The AD8021 op amp, with a nominal settling time of 23 ns to 0.01%, allows the user to custom-compensate it (see Appendix) to achieve the maximum bandwidth, lowest noise, and minimum THD (total harmonic distortion) for a given closed-loop gain. This combination also allows it to meet stringent settling time specifications, even when operated at gains substantially higher than unity.

Noise requirements

The noise generated by an ADC driver amplifier needs to be kept as low as possible in order to avoid worsening the signal to noise ratio (SNR) and the transition noise performance of the 16-bit ADC. When using the AD7671, the op amp driver noise is first scaled down by the resistive divider inside the ADC. The noise is then filtered by the ADC's analog input circuitry.

The net SNR degradation (in dB) due to the amplifier will be:

$$SNR_{LOSS} = 20 \log \left(\frac{N_{ADC}}{\sqrt{N_{ADC}^2 + \frac{\pi}{2} f_{-3dB} \left(\frac{2.5 N e_n}{FSR} \right)^2}} \right)$$

where:

N_{ADC} is the rms noise of the ADC in microvolts

f_{-3dB} is the -3-dB input bandwidth of the ADC in MHz (or the cutoff frequency of the ADC input filter, if used)

N is the noise gain of the amplifier (1 if in unity-gain buffer configuration).

e_n is the equivalent input noise voltage spectral density of the op amp in nV/ $\sqrt{\text{Hz}}$.

FSR is the full-scale input span of the ADC (e.g., 5 V for a ± 2.5 -V range).

For example, assume that the 16-bit AD7671 is being driven by an AD8021 op amp. The ADC has 28- μ V rms noise, 9.6-MHz bandwidth, and a 0-to-5-V input range. The op amp has an equivalent input noise of 2 nV/ $\sqrt{\text{Hz}}$, and a noise gain of +1, when configured as a unity gain buffer, so the SNR of the ADC will be degraded by only 0.08 dB.

Distortion requirements

The input source usually needs a buffer amplifier with low output impedance for isolation from the ADC's input impedance. This buffer's output impedance affects the ac performance of the ADC, especially the level of *total harmonic distortion* (THD). A high source impedance increases THD, because the input impedance of an ADC with inputs swinging 2.5 V will usually have tangible nonlinear input capacitance.

The THD is degraded proportionally to the source impedance. The maximum allowable source impedance in series with the ADC's input depends on the amount of total harmonic distortion (THD) that can be tolerated. The ADC driver also needs to have very low inherent THD, well below that of the ADC (i.e., better than 16-bit accuracy). The combined THD level of the AD7671/AD8021 is typically -100 dB at both 20 kHz and 250 kHz. Figure 1 is a typical plot of THD and the major distortion components as a function of input level for this pair, with the ADC driven from 0 V to 2.5 V.

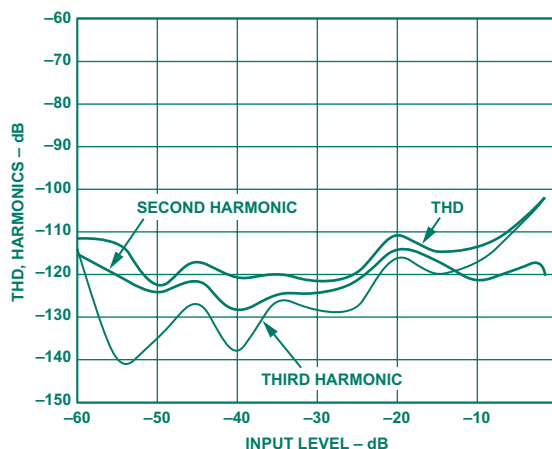


Figure 1. THD, second and third harmonics vs. input level for AD7671/AD8021 ADC/driver combination.

A differential 16-bit ADC driver circuit

The AD7677 is a 16-bit ADC that accepts and processes differential input voltages. Its reference, interface, and power-supply connections are all essentially the same as for the single-ended ADC, as shown in Figure 2. The use of a true-differential input signal will always result in the lowest possible system noise and therefore provide the highest resolution. However, when the input signal is differential, it is essential to use a very low noise op amp input buffer, such as the AD8021, to provide common-mode noise rejection.

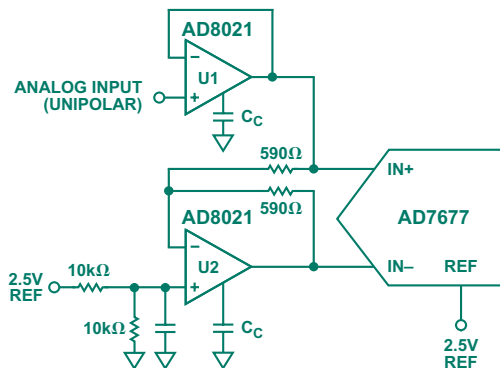


Figure 5. A single-ended to differential-input ADC driver circuit.

The circuit of Figure 5 allows the use of a single-ended transducer with this differential-input ADC. It uses two AD8021 op amps. U1 functions as a unity gain buffer. The output of U1 drives the IN+ input of the AD7677 ADC. (A similar circuit can be used to drive the 18-bit AD7674 ADC, which is pin compatible with the AD7677.) The output of U1 also drives the inverting input of the second op amp, U2, which inverts the signal and drives the IN- input pin of the ADC. U2 is operated at a noise gain of 2, a gain low enough to minimize noise without sacrificing THD performance. The offset reference is applied to the noninverting input of U2 through a 2:1 voltage divider. With a 0 to 2.5-V source, this circuit provides a ± 2.5 -V differential input swing (U1: 0 to +2.5 V and U2: +2.5 V to 0). The mid-scale common-mode offset voltage is 1.25 V. Figure 6 shows the AD7677's typical common-mode rejection (CMR = 20 logCMRR) as a function of frequency.

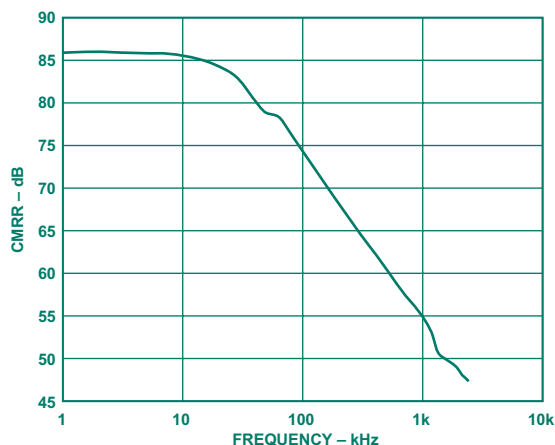


Figure 6. Typical CMR vs. frequency—AD7677/AD8021 combination.

During the acquisition phase, the AD7677 ADC looks like a one-pole RC filter for ac input signals; it consists of internal analog input resistors, R_+ and R_- , nominally 168 ohms, and an internal capacitance, C_S . The resistors, R_+ and R_- , consist of

some series resistance plus the on resistance of the switches. The ADC's sampling capacitor, C_S , is typically 60 pF. This filter, with a typical -3 -dB cutoff frequency of 15.8 MHz, reduces undesirable aliasing effect and reduces high frequency noise coming from the external input circuitry.

Because the input impedance of the AD7677 is very high, the AD7677 can be driven directly by a low impedance source without gain error. This allows further filtering, using (for example) an external one-pole passive RC filter between the outputs of the amplifiers and the input of the ADC. This further improves reduces the noise reaching the ADC's analog input circuit.

Layout, decoupling, and grounding:

Guidelines for high resolution data acquisition

Most high performance ADCs, such as the AD7671, AD7677, and AD7674, have very good immunity to noise on the power supplies. However, the printed circuit board (PCB) that houses the ADC should be designed so that the analog and digital sections are separated, each confined to different areas of the board. Digital and analog ground planes should also be separated, with only one common connection point—preferably underneath the PC board, and located as close as possible to the ADC. Crossover of digital and analog signal wiring should be avoided.

If the ADC is in a system containing multiple analog and digital ground connections, these should still have only a single connection point, using a “star ground”—again located as closely as possible to the ADC. Also, avoid running any digital lines under the ADC, as these may couple noise onto the IC. Instead, run the analog ground plane under the ADC.

High speed clock signals and other waveforms with fast edges should be connected to other circuitry using shielded lines. Close traces on the PC board should run at right angles to each other. The power supply lines should use as large a trace as possible, to provide a low inductance path. Power-supply decoupling capacitors, typically 100 nF ceramic, should bypass the IC, wired as closely as possible to its power supply and ground pins. Additionally, 10- μ F bypass capacitors should be used, to further reduce low frequency ripple. The location of the reference-voltage decoupling capacitor is also important. It should be close to the ADC and connected with short, large traces to minimize any parasitic inductance.

The ADC's ground pins also require attention to detail. ADCs such as the AD7671 and AD7677 each have five different ground pins: INGND, REFGND, AGND, DGND, and OGND. Each is used to sense an individual input or reference line. INGND (analog input ground) is used to sense the analog input signal. REFGND (reference input analog ground) senses the reference voltage; it should be a low impedance return to the reference, because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane, depending on the configuration. The OGND (input/output interface digital power ground) is connected to the digital system ground.

APPENDIX

About custom-compensated op amps

Almost all op amps produced today use internal frequency compensation. This usually consists of an internal compensation capacitor, which provides negative voltage feedback. It is, in effect, part of a single-pole low-pass filter, which causes the op amp's open-loop gain to roll off at a rate of 20 dB (10 \times) per decade as frequency increases. Since most op amps are designed to operate

over a wide range of closed-loop gains, including full feedback, this internal capacitor needs to be made large enough so that the amplifier is always stable. Because of this conservative design for stability at unity-gain operation (or for the op amp's minimum specified gain)—and the inverse gain-bandwidth relationship—the capacitance limits the bandwidth excessively if the amplifier is to be operated at higher gains.

For example, if the usual internally-compensated op amp has a -3-dB bandwidth of 200 MHz operating at unity gain, its bandwidth at a gain +10 will only be about 20 MHz. However, if this same op amp had used a much smaller compensation capacitor, it could have provided full bandwidth at this higher gain, but it would be unstable and oscillate if operated at lower gains. So, this need to maintain stability at low gains sacrifices both bandwidth and slew rate at higher gains. Although so-called “current-feedback” op amps do tend to maintain their bandwidth over a wide range of gains, they typically will have far higher noise levels than a voltage-feedback amplifier. They also have unbalanced input impedances (the plus input is, in effect, a transistor base circuit; and the minus input is an emitter).

The AD8021 is a “custom-compensated” op amp that solves this gain vs. bandwidth performance dilemma. It uses a small internal compensation capacitance of about 1.5 pF to provide stability at gains of 10 or greater. It also features a *compensation pin* to allow the user to add the optimum external capacitance for any desired gain or load condition.

The ability to custom compensate this op amp provides an unbeatable performance combination of wide bandwidth, high slew rate, and low noise. The tradeoff between bandwidth and the ability to drive capacitive loads may also be optimized for a particular application.

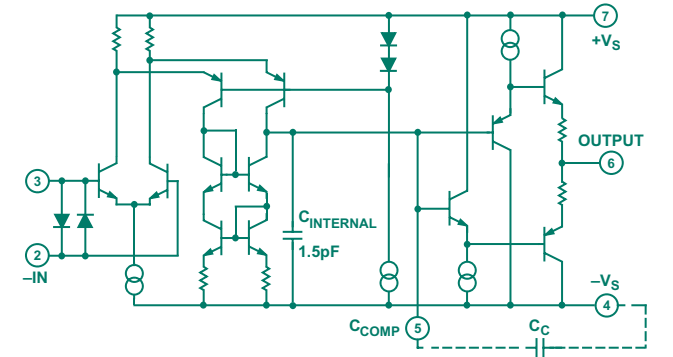


Figure 7. AD8021 simplified schematic.

Figure 7 shows a simplified schematic of the AD8021. The input stage is an NPN differential pair operating at 1.6-mA total collector current. This current level provides high input-stage transconductance with low input noise (2.1 nV/√Hz @50 kHz). The input stage drives a folded cascode and a current mirror to provide the usual differential to single-ended conversion. The external compensation capacitor is connected between a high impedance node, at Pin 5, and the negative supply line. The output stage has a current gain of 5,000, which maintains the high impedance at Pin 5, even when the amplifier is driving heavy loads. Two internal diode-clamps protect the inputs (Pins 2 and 3) from large input transient voltages, which might otherwise cause an emitter-base breakdown—and increase input offset voltage and input bias current.

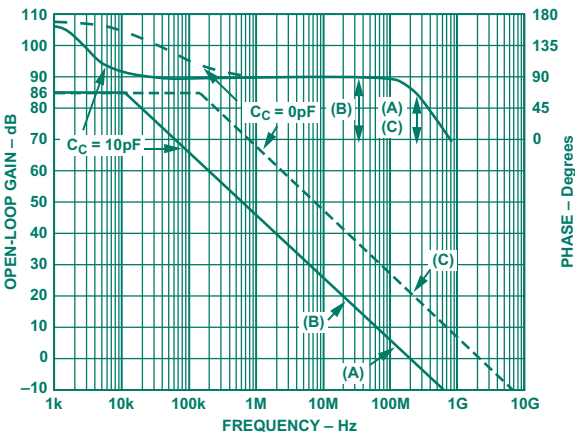


Figure 8. AD8021 open-loop gain and phase vs. frequency.

Table I lists recommended values of resistance and compensation capacitance, and corresponding dynamic performance, for several common closed-loop gain values. Note that the value of the compensation capacitor depends on the circuit noise gain, i.e., its net gain for signals applied to the + input.

As with any high speed op amp, printed circuit board layout is critically important. The use of a hand-wired prototyping board or through-hole components will most likely cause the AD8021 to oscillate, because of excess lead inductance. For this reason, the use of a low cost evaluation board (part number AD8021AR-EVAL) and surface-mount components is highly recommended. The NP0 ceramic chip-capacitors (0805 size) specified in Table 1 are available from Digi-Key Corporation, part numbers PCC020CNCT-ND (2 pF), PCC070CNCT-ND (7 pF), PCC100CNCT-ND (10 pF).

Table I. Recommended Component Values.

See Test Circuit 2. CF = CL = 0, RL = 1 kΩ, RIN = 49.9 Ω

Noise Gain	RS (Ω)	RF (Ω)	RG (Ω)	C _{COMP} (pF)	Slew Rate (V/s)	-3 dB SS BW (MHz)	Output Noise (AD8021 only) (nV/√Hz)	Output Noise (AD8021+R's) (nV/√Hz)
1	75	75	NA	10	120	490	2.1	2.8
2	49.9	499	499	7	150	205	4.3	8.2
5	49.9	1 k	249	2	300	185	10.7	15.5
10	49.9	1 k	110	0	420	150	21.2	27.9
20	49.9	1 k	52.3	0	200	42	42.2	52.7
100	49.9	1 k	10	0	34	6	211.1	264.1