AD9873 Mixed-Signal Front End (MxFE) for Broadband Digital Set-Top Boxes

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Widespread deployment of TV cable has led to extensive research in providing better quality and increased variety in TV programming and cable-modem functionality. This effort resulted in the development of digital set-top boxes from several established vendors, including Scientific Atlanta and Motorola (General Instrument). Instead of analog *vestigial-sideband* modulated (VSB) channels, digital set-top boxes receive TV programming and exchange information with the head-end station using *quadrature amplitude modulation* (QAM). Transmitting analog information in digital bits is not only more robust but also makes use of available bandwidth more efficiently. Figure 1 shows a digital set-top box connected to the head-end and to various devices inside the residence (or office).

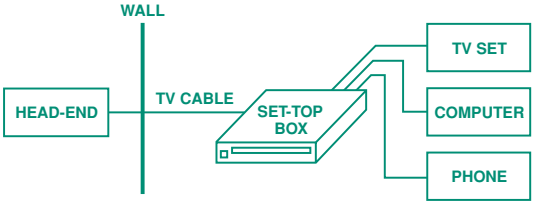

Figure 1. Cable set-top box gateway configuration.

Several services can be unified in this fashion, including Internet access, cable TV and even phone services. High data rates allow streaming-in MPEG movies as well as high-quality telephony (voice-packet) service.

A digital set-top box, like that shown in Figure 2, comprises several major subsystems to implement such functions as a TV tuner, base-band transceivers, a channel 3/4 modulator (for compatibility with analog TV sets), MPEG and NTSC decoders and encoders, physical layer (PHY), and media access control (MAC) for cable modems. Since Internet access implies an upstream channel, a cable driver is included; it can be implemented using a member of the AD832x family. The box can also include an *out-of-band* (OOB) control channel and a phone line interface.

The multiplicity and complexity of all these blocks impose significant challenges on designers at both the component and board levels. The large amount of digital processing required, combined with the high-quality reception requirements of high-definition digital TV, pose numerous challenges to digital set-top box architects. In addition, compatibility with analog TV calls for clean analog signal processing from the wall TV cable outlet to the TV set. Therefore, selecting a proper partition for integrated functions becomes a key requirement for combining high-quality TV reception and high data rates in a cable modem at low cost.

The mixed-signal front end, which can be implemented using the AD9873, is central to the set-top box (Figure 2).

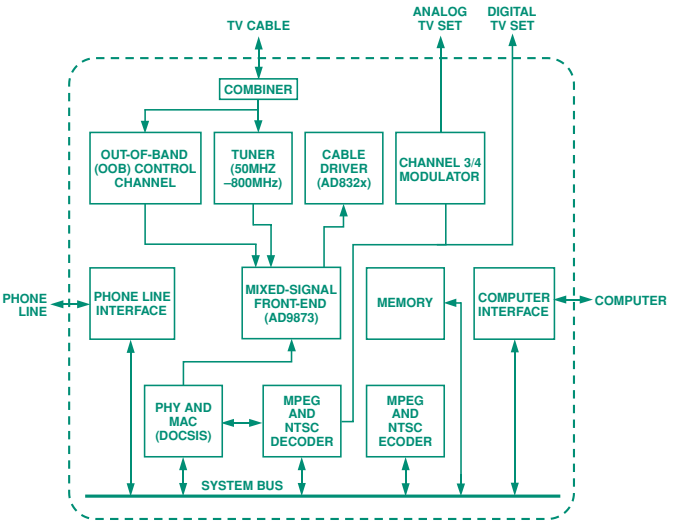

Figure 2. Inside a typical digital set-top box.

Mixed-Signal Front End

The definition of a mixed-signal front end for a set-top box must take into account the amount of functionality required from the *transmit* and *receive* data paths. Low cost is of vital importance, so selecting a proper technology is key to a successful design. In addition, time to market is equally important for both the IC vendor and the OEM. ASICs that include significant digital and analog content are often difficult to schedule due to the time needed to handle the inherent design challenges and the frequent need for customer feedback. The designers of the Analog Devices AD9873 took advantage of both their experience in set-top-box technology and their inventory of high-performance topological block core designs of the kind that would be needed to integrate the essential high-performance analog and mixed-signal functions on a single chip.

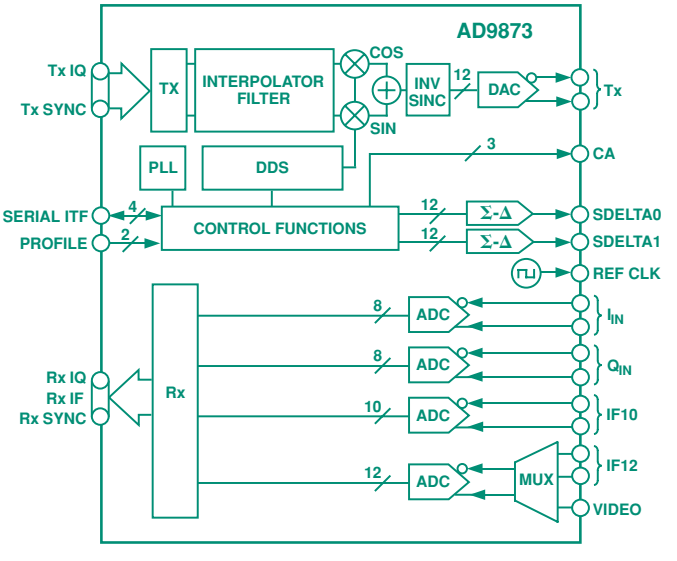

Figure 3. AD9873 functional block diagram.

Figure 3 is a block diagram of the AD9873 Analog Front End Converter for Set-Top Boxes and Cable Modems. The *receive* data path contains several analog-to-digital converters (ADCs) to accommodate the various set-top box functions described earlier. A pair of 8-bit ADCs is used to convert quadrature inputs from the demodulated OOB channel. They are designed for modest

performance—better than 7 effective number of bits (ENOB) when sampling at less than 16 MHz—since the OOB data utilizes low-complexity modulation (QPSK) in a narrow-band channel (<1 MHz). A tighter specification is required from the 10-bit ADC, due to its major role in digitizing cable modem data. This type of data is broadcast using higher-order QAM modulation, which requires a higher signal-to-noise ratio. Hence, the converter needs to exhibit better than 9 ENOB when sampling an input signal of up to 10 MHz at 33 MSPS. The fourth ADC, a 12-bit converter, sampling at 33 MHz and providing better than 10.5 ENOB for inputs up to the Nyquist rate, can digitize high-definition TV signals. For single-ended video signals multiplexed to the same input, a programmable black-level clamp is provided. The outputs of all these converters are multiplexed to reduce the number of package pins.

The *transmit* data path contains a demultiplexed interface, which receives I/Q baseband data, typically sampled at about 13 MHz (up to 16 MHz). Since interpolation is a powerful tool for reducing DAC output filter requirements (used successfully in the AD9772 and AD9856), three interpolation filters are used. The interpolation factor can be programmed for 12 or 16, bringing the data rate up to 230 MHz. The overall interpolator frequency response is determined by two half-band filters and a cascaded integrator comb filter (CIC). Following the interpolator, a quadrature modulator is implemented using *direct digital synthesis* (DDS) to generate the sine and cosine waveforms. Before being fed into the DAC, the signal can be compensated for the $\sin(x)/x$ roll-off, which results from the D/A conversion process. This operation is optional, since the roll-off becomes noticeable only toward the end of the synthesized carrier frequency range. The DDS can produce a low-spurious-content complex carrier at frequencies up to approximately one-third of the sampling rate, that is, up to 70 MHz.

The ADCs are clocked directly from a low-frequency crystal; its frequency is stepped up by an on-board programmable phase-locked-loop (PLL) to provide the high-speed clock required for the DAC. This approach reduces undesirable clock jitter when sampling the ADCs and eliminates the problems and expense of an off-chip high-frequency oscillator. The programmable PLL also provides the system clock to other blocks within the set-top box. Auxiliary digital sigma-delta outputs facilitate automatic gain control or timing recovery functions. Many of the device parameters are programmable through a 3- or 4-pin serial interface.

In order to seamlessly interface with a member of the AD832x cable driver family, a separate 3-wire interface is included, and several profile registers (which can be loaded through the serial interface) are designed to speed up changes in transmit gain data and carrier frequency. This can be achieved by using dedicated external pins that address a particular profile register bank. Figure 4 shows how the AD9873 would be used in a complete digital set-top box application.

Designers of broadband modems require the combination of small form factors, high performance levels, and low cost. Because of the cost and area impact of heat management within the box, they cannot afford to dissipate watts of power in the transmit or receive path. To build the large-scale digital integrated circuits that meet these requirements in broadband modem designs, state of the art, low-voltage lithographies are needed. However, they are not suitable for high-performance analog and mixed-signal circuitry. Products like the AD9873 provide a solution to this problem by offering the possibility of using two small highly integrated chips—a digital ASIC and a mixed-signal "everything else"—that appropriately partition the large scale digital IC from the high-performance mixed-signal component.

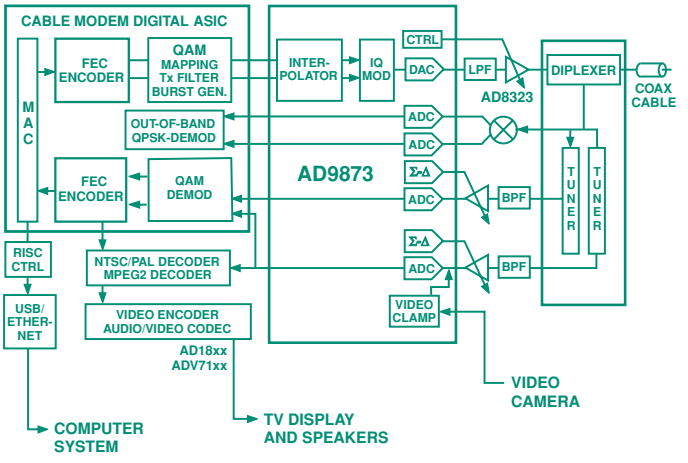

Figure 4. Intelligent system partitioning helps to solve the challenge of optimizing price, performance, size, and power in broadband modem designs.

Figure 5 demonstrates how this approach leads the trend in broadband communication applications away from single-chip solutions that unsuccessfully attempt to integrate the large scale digital processing with the high-performance mixed-signal devices. Emerging broadband modems require both more powerful digital processing (>MIPS) and higher performance mixed-signal (> dynamic range and bandwidth) devices. The large scale integrated digital devices used in these applications need the utmost state-of-the-art (fine geometry), low voltage, CMOS processes, while the mixed-signal devices depend on higher voltage CMOS processes that are optimized for handling mixed signals with high performance. As the first device of a new family of broadband MxFEs, the AD9873 will allow designers to take advantage of "smart partitioning."

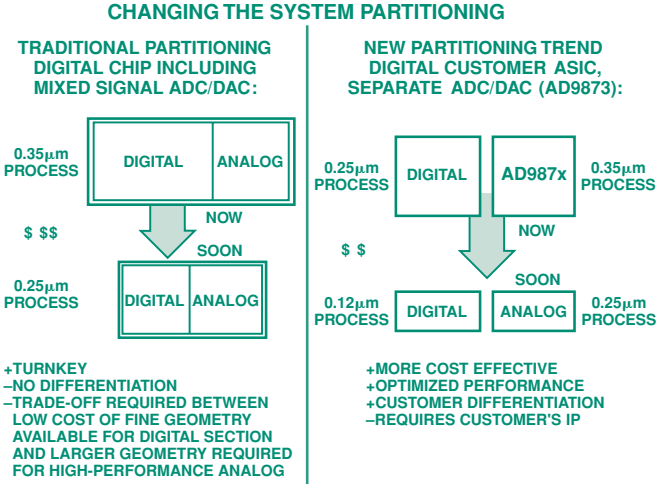

Figure 5. Smart partitioning model.

Here's why it works: Deep submicron geometry processes do not readily support the voltage levels required by high-performance D/A and A/D converters, and coupling of digital noise into the analog signal chain will corrupt signal fidelity. There are times when trying to put everything on a single chip results in a higher-price and/or lower-performance solution. Trying to mix high-speed and wide dynamic range mixed-signal devices with very large scale digital processing is a perfect case in point. It will always require compromises either in digital area (cost), power consumption, or mixed-signal performance. The AD9873 broadband Mixed-Signal Front End, and the other MxFE products that will follow in its wake, gives designers the benefit of high integration, low cost, and low power consumption, without compromising performance.

The AD9873 applies this optimized mixed-signal technology and "smart" partitioning to provide excellent dynamic performance for a variety of modulation formats—FSK, QPSK, 16/32/64/256 QAM, OFDM, spread spectrum, etc. The digital ASIC, which includes the modulation encoding, can be implemented on the most cost effective and finest geometry possible. With this cost-effective approach, system designers can keep more "value added" in their own digital ASIC, making best use of their system expertise, proprietary algorithms, and intellectual property. The AD9873's mixed-signal partitioning resolves the cost and performance trade-off issues related to integrating mixed-signal circuits within VLSI digital ASICs by getting them off the chip.

Other Applications for the AD9873 Mixed-Signal Front End

Besides cable set-top boxes, the AD9873 is well suited for a variety of other standard and proprietary broadband communications applications, as depicted in Figure 6. Here is a list of other applications where the AD9873 can be used:

- Cable Modem
- Digital Communications
- Data and Video Modems
- Power Line Modem
- Satellite Systems
- PC Multimedia
- Broadband Wireless Communication
- Home Networking

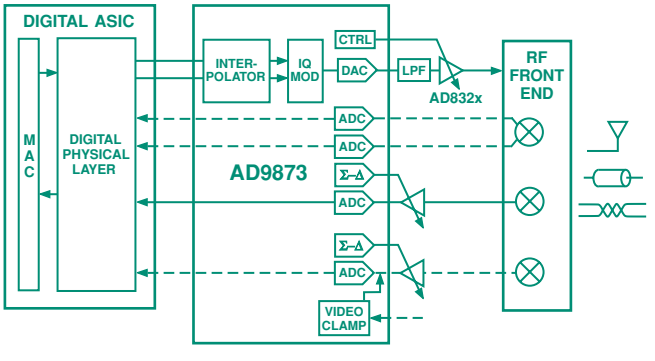

Figure 6. Broadband modems over cable, power line, or wireless, using the AD9873.

AD9873 Key Features and Performance

- 232 MHz Quadrature Digital Upconverter:
  - DC to 70 MHz Output Bandwidth
  - 12-Bit Direct IF D/A Converter
  - Direct Digital Synthesis
  - Interpolation and Sin(X)/X Filters
- 12-Bit 33 MSPS Direct IF ADC
- 10-Bit 33 MSPS Direct IF ADC
- Dual 8-Bit 16.5 MSPS I&Q ADCs
- Dual 12-Bit Sigma-Delta Control DACs
- Video Input with Clamp Circuitry
- Direct Interface to AD8321/AD8313 PGA Cable Driver
- Programmable PLL Clock Multiplier
- Single 3.3 V Supply Operation
- Power-Down Modes
- 100-Lead MQFP

Performance of the AD9873 was characterized with respect to the commercial temperature range; however, it can be safely used from –40°C to +75°C. Figure 7 shows a spectral plot of the 12-bit ADC performance with a 10-MHz input.

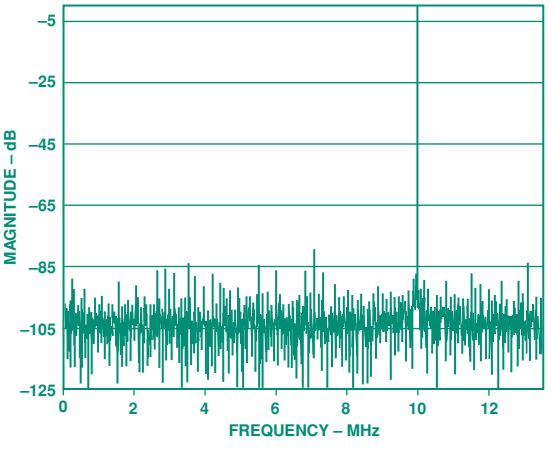

Figure 7. AD9873's 12-bit ADC performance plot with 10-MHz input.

Figure 8 shows the spectral plot of the DAC producing a 42-MHz 16-QAM signal. Figure 9 shows the constellation and eye diagram of a 64-QAM signal generated by the AD9873.

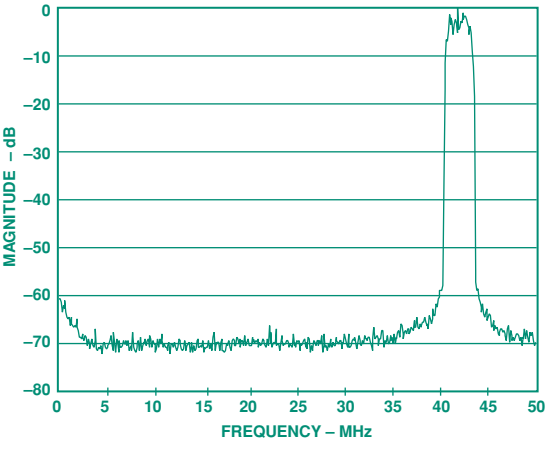

Figure 8. AD9873 DAC performance plot.

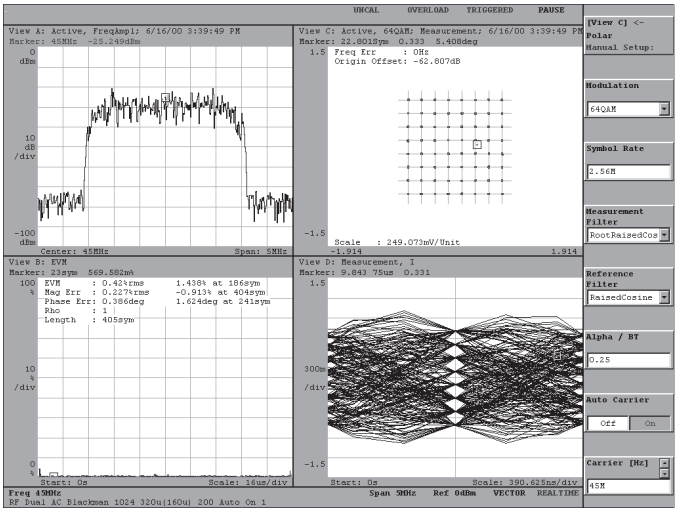

Figure 9. AD9873 64-QAM constellation plot.

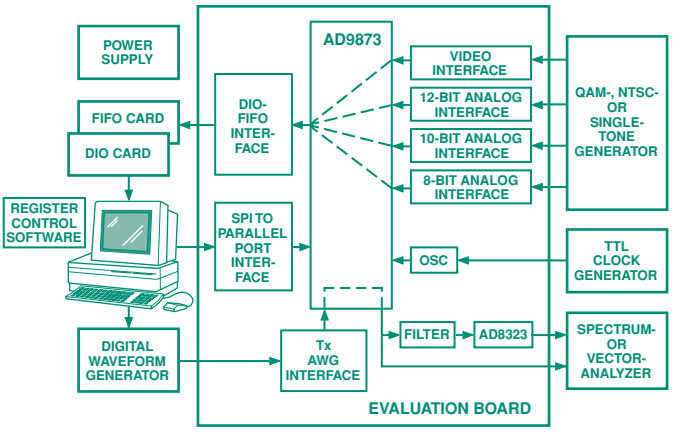

Figure 10. AD9873 evaluation setup.

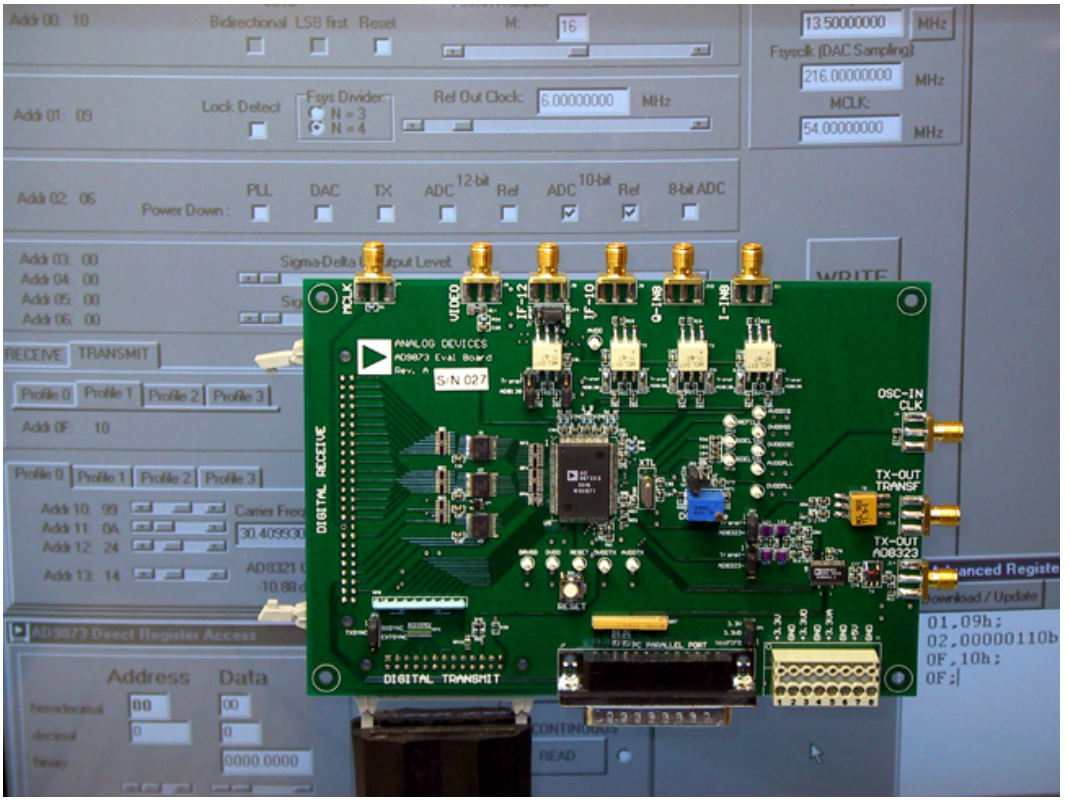

Figure 11. AD9873 evaluation board and software interface.

Evaluation Board and Software

The AD9873 Evaluation board and software allow users to easily program and quickly evaluate the AD9873 for a specific modem application.

Availability

The AD9873 was released to production in summer 2000. It is available in a 100-lead MQFP package, is priced at $16.58 (1000s), and sells for less then $10 in high volume.