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StudentZone—ADALM2000 Activity: Amplifier Output Stages

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Objective

The objective of this activity is to investigate the output stages (class B and AB) of a simple push-pull amplifier.

Background

The role of an output stage is to provide power gain. It should have high input impedance and low output impedance. An obvious choice for this stage is the emitter follower. However, in order to provide both current sourcing and sinking capabilities, two complementary followers are needed: an NPN type to source and a PNP type to sink current. The result is known as the push-pull configuration—Figure 1 shows a simple example. Here R1 and R2 are used to sense the collector currents of Q1 and Q2, as well as to limit these currents in case of output overloading.

Materials

- ADALM2000 Active Learning Module
- Solderless breadboard
- Jumper wires
- Two 100 Ω resistors
- One 2.2 kΩ resistor
- Two 10 kΩ resistors
- Two small signal NPN transistors (SSM2212 with matching V_{BE} preferred)
- Two small signal PNP transistors (SSM2220 with matching V_{BE} preferred)

Directions

Before starting, make sure the power supplies on the ADALM2000 are turned off. The circuit and the connections to the lab hardware are as indicated in Figure 1. Oscilloscope Input 1 should be connected to the junction of Q1 and Q2 bases. Oscilloscope Input 2 should be connected to the junction of Q1 and Q2 emitters.

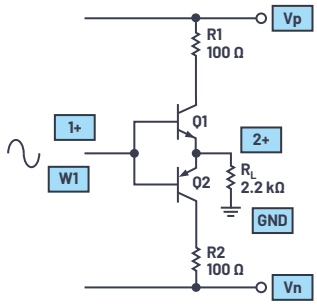

Figure 1. A push-pull output stage.

Hardware Setup

Channel 1 of the oscilloscope should be connected to display the output of the first generator, and both channels (1 and 2) should be set to display 1 V per division. The breadboard connections are shown in Figure 2.

Procedure

The waveform generator, W1, should be configured for a 1 kHz sine wave with approximately 6 V amplitude peak-to-peak and 0 offset. Set the positive power supply (Vp) to +5 V and the negative power supply (Vn) to −5 V. Use Oscilloscope Channel 1 to observe the input at W1 and Oscilloscope Channel 2 to observe the output of the amplifier at R_L. A Scopy plot example is presented in Figure 3.

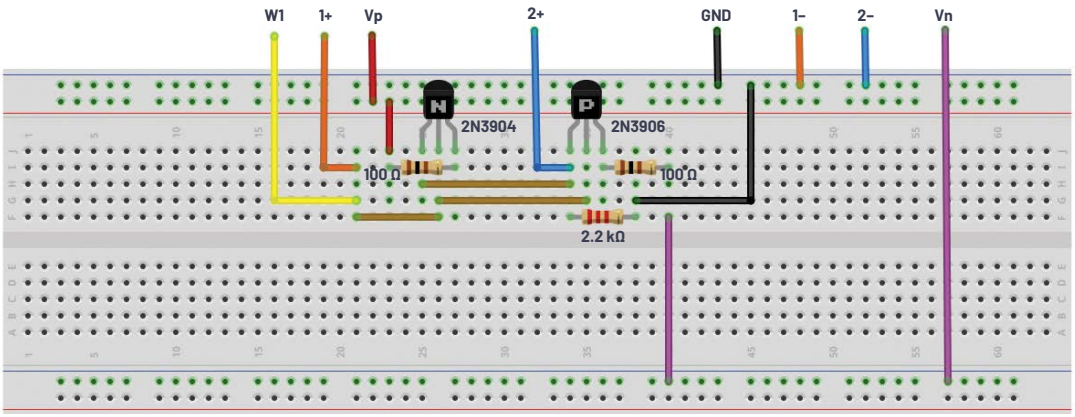

Figure 2. A push-pull output stage breadboard circuit.

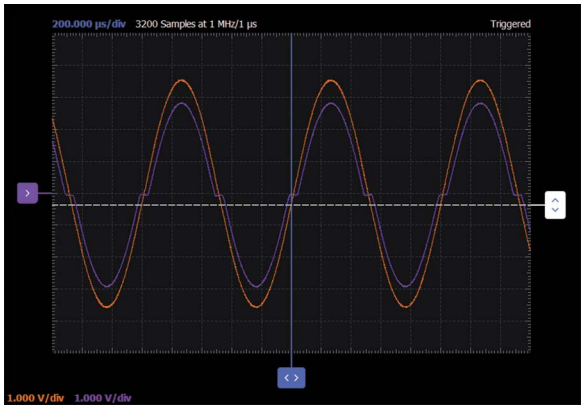

Figure 3. Push-pull output stage waveforms.

Next, apply power and adjust the waveform generator so that W1 is a 100 Hz triangle wave with 0 V offset and 3 V amplitude peak-to-peak. Use the oscilloscope in x-y mode to observe the voltage-transfer curve of the circuit. A Scopy XY plot example is presented in Figure 4.

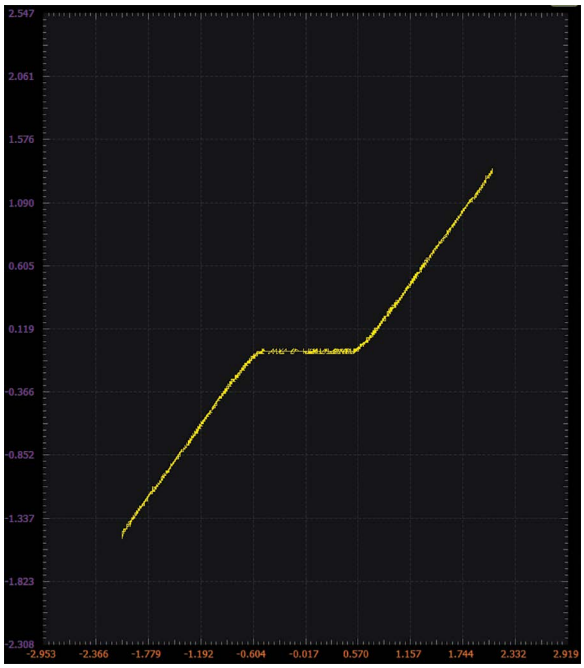

Figure 4. Voltage-transfer curve.

Reducing Output Distortion

The large amount of distortion at the zero-crossings in the basic push-pull stage of Figure 1 is a result of a dead zone when both the NPN and PNP emitter followers are off. The waveform's dead zone at the zero-crossings is dramatically reduced if we pre-bias the BJTs with two V_{BE} drops, as shown in Figure 5. Here, the pre-bias function is provided by diode connected NPN Q1 and PNP Q3. Resistors R1 and R2 provide bias current and set the idle current that flows in the output devices Q2 and Q4.

Directions

With the power turned off, assemble the circuit of Figure 5, keeping leads as short and neat as possible. NPN transistors Q1 and Q2 and PNP transistors Q3 and Q4 should be selected from the available devices with the best matching of V_{BE}. Transistors fabricated in the same package, such as the SSM2212 or the CA3046, tend to match much better than individual devices.

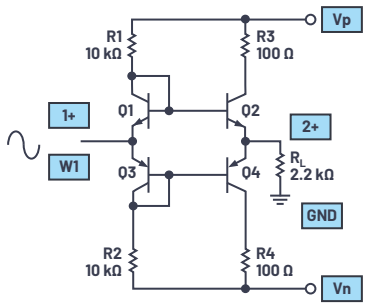

Figure 5. The push-pull output stage with zero-crossing distortion elimination.

If we examine, in Figure 5, the loop formed by the base emitter voltages of Q1, Q2, Q3, and Q4, we know that the voltage drops around the loop must sum to zero. Thus, if Q1 is identical to Q2 and Q3 is identical to Q4, the voltage around the loop will be zero only when the current in Q1 is identical to the current in Q2 and the current in Q3 is identical to the current in Q4. When the output is at zero volts—that is, there is no current in R_L—the input must also be at zero volts.

Hardware Setup

Channel 1 of the oscilloscope should be connected to display the output of the first generator, and both channels (1 and 2) should be set to display 1 V per division. The breadboard connections are shown in Figure 6.

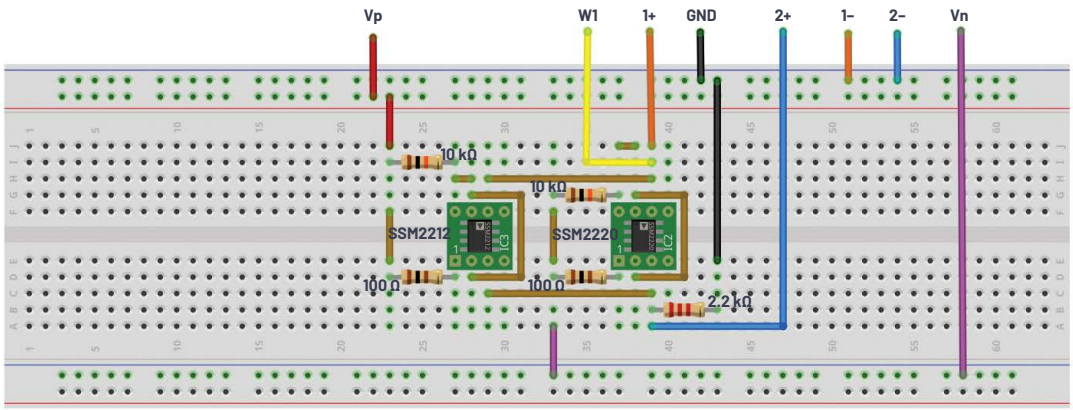

Figure 6. The push-pull output stage with a zero-crossing distortion elimination breadboard circuit.

Procedure

The waveform generator, W1, should be configured for a 1 kHz sine wave with approximately 6.0 V amplitude peak-to-peak and 0 offset. Use Oscilloscope Channel 1 to observe the input at W1 and Oscilloscope Channel 2 to observe the output of the amplifier at R_L.

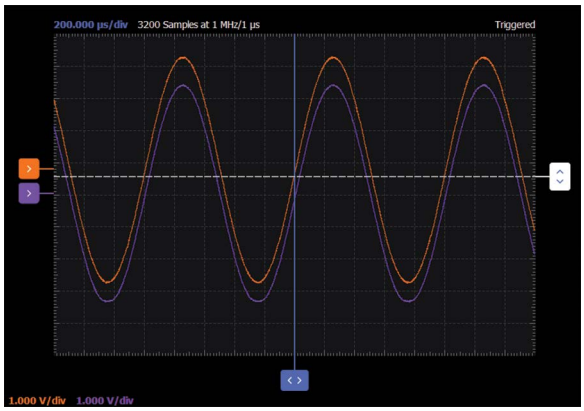

Figure 7. The push-pull output stage with zero-crossing distortion elimination waveforms.

Another Configuration

Remembering the loop formed by the base emitter voltages of Q1, Q2, Q3, and Q4, we also know that the order of the voltage drops around the loop can be interchanged. So, if we interchange the V_{BE} values of NPN Q1 and PNP Q3, we get the configuration shown in Figure 8. Some of you may recognize the combination of Q3 and Q2 as the low offset follower we discussed in the April article, "ADALM2000 Activity: The Emitter Follower (BJT)." The circuit uses the V_{BE} shift-up of a PNP emitter follower to partially cancel the VBE shift-down of an NPN emitter follower. Transistors Q1 and Q4 are simply the complement of Q3 and Q2.

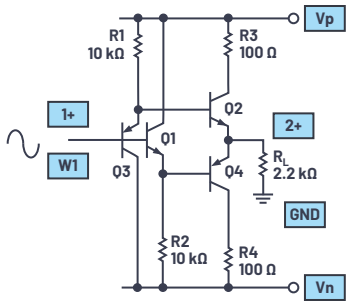

Figure 8. Emitter follower zero-crossing distortion elimination.

Hardware Setup

Channel 1 of the oscilloscope should be connected to display the output of the first generator, and both oscilloscope channels (1 and 2) should be set to display 1 V per division. The breadboard connections are shown in Figure 9.

Procedure

The waveform generator, W1, should be configured for a 1 kHz sine wave with approximately 6 V amplitude peak-to-peak and 0 offset. Use Oscilloscope Channel 1 to observe the input at W1 and Oscilloscope Channel 2 to observe the output of the amplifier at R_L.

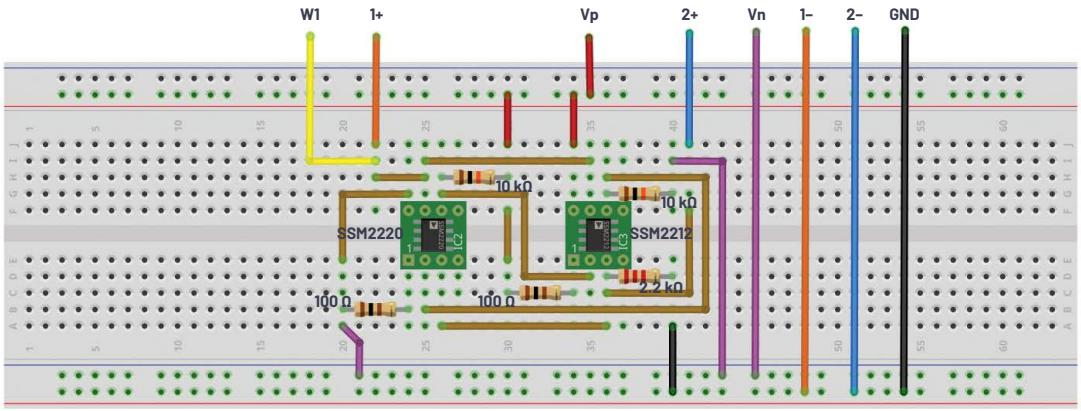

Figure 9. Emitter follower zero-crossing distortion elimination breadboard circuit.

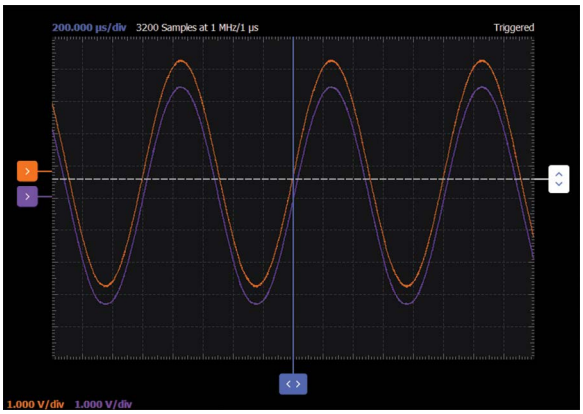

Figure 10. Emitter follower zero-crossing distortion elimination waveforms.

Question:

- For the circuits in Figure 5 (push-pull output stage with zero-crossing distortion elimination) and Figure 8 (emitter follower zero-crossing distortion elimination), simulate and plot the input/output transfer curve. How do they compare to the circuit in Figure 1?

About the Author

Doug Mercer received his B.S.E.E. degree from Rensselaer Polytechnic Institute (RPI) in 1977. Since joining Analog Devices in 1977, he has contributed directly or indirectly to more than 30 data converter products and he holds 13 patents. He was appointed to the position of ADI Fellow in 1995. In 2009, he transitioned from full-time work and has continued consulting at ADI as a Fellow Emeritus contributing to the Active Learning Program. In 2016 he was named Engineer in Residence within the ECSE department at RPI. He can be reached at doug.mercer@analog.com.

About the Author

Antoniu Miclaus is a system applications engineer at Analog Devices, where he works on ADI academic programs, as well as embedded software for Circuits from the Lab®, QA automation, and process management. He started working at Analog Devices in February 2017 in Cluj-Napoca, Romania. He is currently an M.Sc. student in the software engineering master's program at Babes-Bolyai University and he has a B.Eng. in electronics and telecommunications from Technical University of Cluj-Napoca. He can be reached at antoniu.miclaus@analog.com.