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Put an End to High Speed Converter Bandwidth Terms

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There are many confusing specifications that are centered around a converter's bandwidth. What bandwidth term(s) should I use in order to choose an appropriate converter for my next design?

When starting a new design, the parameter that needs to be decided on first and foremost is bandwidth. Bandwidth will provide direction in the design and will allow the designer to start carving the path to success. Essentially there are three types of front ends to choose from: baseband, band-pass or super-Nyquist (also sometimes referred to as narrow-band and/or subsampling—basically you are not using the 1st Nyquist zone), and wideband, as shown in Figure 1. The application determines which front end should be applied.

Baseband designs require a bandwidth from dc (or the low kHz or MHz region) to the Nyquist of the converter. In terms of relative bandwidth, this implies about 100 MHz or less, assuming a sample rate of 200 MSPS. Designs like these can employ an amplifier or transformer/balun.

A band-pass design means a small piece of the converter's bandwidth (that is, <Nyquist) is going to be used at high IFs. For example, the requirement might only be 20 MHz to 60 MHz and centered at 170 MHz—again, assuming 200 MSPS. However, trends show the market is targeting for even higher IFs, with the release of newer GSPS converter type offerings. So the example in the previous statement might be padded with an extra 0. In essence, the designer only needs a small piece of converter bandwidth to do the job. Typically, a transformer or balun is used here. However, an amplifier can be used if the dynamic performance is adequate at these higher frequencies and gain is required.

A wideband design usually refers to those designs that need it all. As much bandwidth as the converter will supply, the user will take—like drinking from a firehose! These can be the most challenging front-end designs since they have the widest bandwidth of the three. Even more challenging is if the design calls for 0.1 dB flatness across the pass band. These applications require dc or low kHz/MHz regions to the +GHz region. These types of designs often employ a wideband balun to couple to the converter.
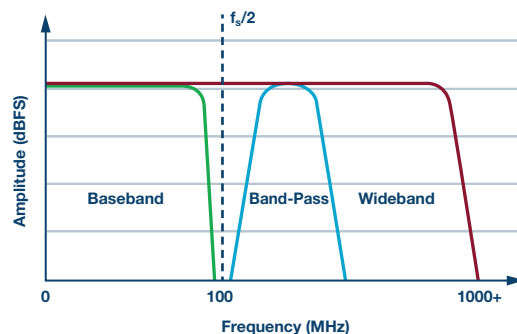

Figure 1. Baseband vs. band-pass vs. wideband, F_{SAMPLE} = 200 MSPS.

Notes on Bandwidth

The term bandwidth is tossed around loosely in engineering and, depending on the application, it can mean something completely different from one designer's perspective to another's. In this article, the converter's full power bandwidth is different from a converter's usable or sample bandwidth. Full power bandwidth is the bandwidth that the converter needs to acquire signals accurately and for the internal front end to settle properly. In most cases, the converter's sample bandwidth target is dialed in at roughly two Nyquist zones. The converter is often characterized this way over its ac frequency specifications as well.

A designer selecting an IF outside the converter's specified region is not a good idea, as ac performance results will widely vary in the system, despite the rated resolution and performance stated in a converter's data sheet, or shown full-power bandwidth, being much bigger (possibly 2×) than the sample bandwidth of the converter itself. Sample bandwidth is what the design is centered around. All designs should avoid using some or all of the highest frequency portions of the rated full power bandwidth—by doing so, expect a derating in dynamic performance (SNR/SFDR). To determine the sample bandwidth of a high speed analog-to-digital converter, consult the data sheet or application support, as sometimes the

sample bandwidth isn't specially given. Typically, the data sheet has specified or even listed production tested frequencies that guarantee delivered performance within the converter's sample bandwidth. However, better explanations about these bandwidth terms in the industry need to be specified and defined.

Understanding Converter Bandwidth and Accuracy

All ADCs have a settling-time inaccuracy. Keep in mind that a converter's internal front end must have enough bandwidth (BW) to accurately sample the signal. Otherwise, the accumulation of errors will be greater than what was described above.

In general, an ADC's internal front end must settle within half a period of the sample clock cycle ($0.5/f_s$, where f_s = sample frequency) to provide an in-bounds accurate representation of the analog signal to be acquired. Therefore, for a 12-bit ADC sampling at 2.5 GSPS and a full-scale input range (V_{FS}) of 1.3 V p-p, the full-power bandwidth (FPBW) required can be derived by starting with the transient equation:

$$1 \text{ LSB} = V_{FS} \times e^{(-t/\tau)}$$

Solving for t:

$$t = -\tau \times \ln\left(\frac{1 \text{ LSB}}{V_{FS}}\right)$$

Substituting in $\tau = 1/(2 \times \pi \times \text{FPBW})$ for one time constant, and solving for FPBW:

$$\text{FPBW} = -\left(\frac{1}{2 \times \pi t}\right) \times \ln\left(\frac{1 \text{ LSB}}{V_{FS}}\right)$$

let $t = 0.5/f_s$. That is the time needed for a sample to settle, where the sampling period is $1/f_s$:

$$\text{FPBW} = -\left(\frac{f_s}{\pi} \times \ln\left(\frac{1 \text{ LSB}}{V_{FS}}\right)\right) = -\left(\frac{2.5 \text{ G}}{\pi}\right) \times$$
$$\ln\left(\frac{317 \text{ } \mu\text{V p-p}}{1.3}\right)\right) = 6.62 \text{ GHz}$$

This will yield the minimum required bandwidth for the ADC's internal front-end FPBW. The converter's internal front end needs this amount of bandwidth to settle within 1 LSB and sample the analog signal appropriately. It will require the passage of several time constants to meet an accuracy of 1 LSB for this type of ADC, where one time constant is equal to 24 ps, or:

$$\tau = \frac{1}{(2 \times \pi \times \text{FPBW})}$$

To understand the number of time constants required for the full-scale

range of the ADC in LSB size, %Full-scale error, or V_{FSE}, needs to be found. Or, $1 \text{ LSB} = V_{FS}/(2^N)$, where N = number of bits; or

$$\text{LSB} = \frac{1.3 \times \text{V p-p}}{(2^{12})} = 317 \text{ } \mu\text{V p-p, and } V_{FSE} =$$
$$\left(\frac{\text{LSB}}{V_{FS}}\right) \times 100 = 0.0244$$

See Table 1, which shows a breakdown of different resolution converters vs. the number of bits, LSB size, and the V_{FSE} for each.

Table 1. Converter Resolution Breakdown

Converter Resolution	Number of Bits	LSB Size	V_{FSE}
6	64	0.01875	1.5625
8	256	0.0046875	0.390625
10	1024	0.001171875	0.09765625
12	4096	0.000292969	0.024414063
14	16384	0.0000732422	0.006103516
16	65536	0.0000183105	0.001525879

By plotting Euler's number, or e^τ, a graph can be developed that makes it easy to show the relative error with the passing of each time constant. In Figure 2, it can be found that it takes 8.4 time constants for the 12-bit ADC example to settle appropriately within 1 LSB.

This analysis allows designers to estimate the maximum analog input frequency, or sample bandwidth, that the converter can handle and still settle within 1 LSB of error. Beyond that, the ADC cannot accurately represent the signal. Thus:

$$F_{max} = \frac{1}{(\tau \times \text{number of time constants})} \text{ or}$$
$$\frac{1}{(24 \text{ ps} \times 8.4)} = 4.96 \text{ GHz}$$

Keep in mind that this represents a best-case scenario, and the assumption is for a single-pole model ADC front end. Not all practical converters behave this way, but this is good starting point.

For example, the model described is valid up to 12 bits. However, for 14 or 16 bits and beyond, a second-order model should be used, because of subtle effects that can make settling time stretch out beyond the predicted first-order models.
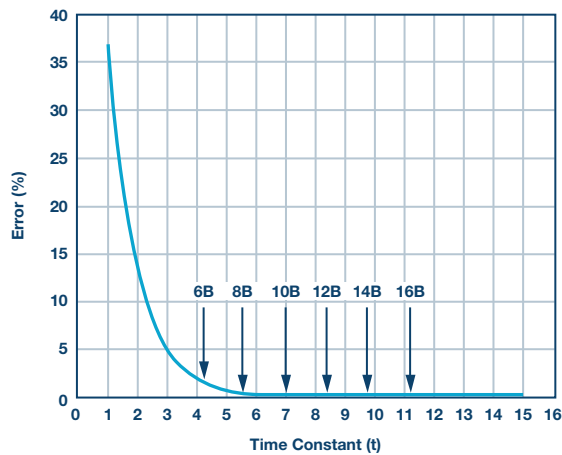
Figure 2. Converter sampling accuracy vs. number of time constants: number of time constants an ADC needs in order to settle accurately within ½ LSB.

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Rob Reeder [rob.reeder@analog.com] is a senior system application engineer with Analog Devices in the High Speed Converter and RF Applications Group in Greensboro, North Carolina. He has published numerous articles on converter interfaces, converter testing, and analog signal chain design for a variety of applications. Formerly, Rob was an application engineer for the Aerospace and Defense Group for five years, where he focused on a variety of radar, EW, and instrumentation applications. Previously he was part of the high speed converter product line for nine years. His prior experience also includes test development and analog design engineering for the Multichip Products Group at ADI, where he designed analog signal chain modules for space, military, and high reliability applications for five years. Rob received his M.S.E.E. and B.S.E.E. from Northern Illinois University in DeKalb, Illinois, in 1998 and 1996, respectively. When Rob isn't writing papers late at night or in the lab hacking up circuits, he enjoys hanging around at the gym, listening to techno music, building furniture out of old pallets, and, most importantly, chilling out with his two boys.