

# Rarely Asked Questions

Strange stories from the call logs of Analog Devices

## Considerations on High-Speed Converter PCB Design, Part 2: Using Power and Ground Planes to Your Advantage

**Q.** What are some important PCB layout rules when using a high-speed converter?

**A.** Part 1 of this RAQ discussed why splitting AGND and DGND is not necessary unless circumstances within the design force you to make that choice. Part 2 discusses the design of a power delivery system (PDS) for the printed circuit board (PCB). Often overlooked, this task is critical for analog and digital designers working at the system level.

The PDS design goal is to minimize the voltage ripple that occurs in response to supply current demand. All circuits require current, some more than others and some at faster rates than others. A low-impedance power or ground plane with adequate decoupling and a good PCB stack will minimize the voltage ripple that occurs as a result of the circuit's current demands. For example, if a design has 1-A switching currents and the PDS has 10-m $\Omega$  impedance, the maximum voltage ripple will be 10 mV.

First, design a PCB stack that supports a large plane capacitance. For example, a six-layer stack may comprise top signal, ground1, power1, power2, ground2, and bottom signal. Specify ground1 and power1 to be close in the stack—separating them by 2 mils to 3 mils forms an inherent plane capacitor. The best part about this capacitor is that it is free; just specify it in the PCB fabrication notes. If the power planes must be divided, with multiple VDD rails on the same plane,



use as much of the plane as possible. Don't leave voids, but be mindful of sensitive circuitry as well. This will maximize the capacitance for that VDD plane. If the design allows extra layers—from six to eight in our example—put two extra ground planes between power1 and power2, doubling the inherent capacitance in the stack given the same 2-mil to 3 mil core spacing.

With the perfect PCB stack, use decoupling at both the entry point where the power plane originates and around the DUT. This will ensure a low PDS impedance across the entire frequency range. Use a handful of capacitor values from 0.001  $\mu$ F to 100  $\mu$ F to help cover this range. It isn't necessary to sprinkle capacitors everywhere, and butting them right up against the DUT breaks all kinds of manufacturing rules. If these kinds of drastic measures are required, then something else is going on in the circuit.

**To Learn More About  
High-Speed Layout**

<http://dn.hotims.com/34921-101>



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