RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Considerations on High-Speed Converter PCB Design, Part 1: Power and Ground Planes.

Q. What are some important PCB layout rules when using a high-speed converter?

A. To ensure that the design meets datasheet specifications, you should follow a few guidelines. First, an age old question: "Should the AGND and DGND ground planes be split?" The short answer is: it depends.

The long answer is: not usually. Why? In most situations a split ground plane can cause more harm than good, as splitting the ground plane only serves to increase the inductance for the return current. Remember the equation V = L(di/dt)? As the inductance increases, so does the voltage noise. As the switching current increases—and it will as converter sampling rates increase—the voltage noise will also increase. Therefore, keep the grounds connected unless you have a reason to split them.

One example is when a form factor restriction prohibits good layout partitioning. This could be because the dirty bus supplies or digital circuits must be located in certain areas to conform with legacy designs. In that case, splitting the ground plane may make the difference in achieving good performance. However, to make the overall design work, a bridge or tie point is required to connect the grounds together somewhere on the board. With that being the case, spread the tie points evenly across the ground plane split. One tie point on the PCB often ends up being the optimum place for the return current to pass without reducing performance. This tie point is usually near or under the converter.



When designing the power planes, use all of the copper available for these designated layers. If possible, don't share traces on the same layers, as additional traces and vias can quickly compromise the power plane by breaking it into smaller pieces. The resultant sparse plane can squeeze current paths down where they are needed most: at the converter's supply pins. Squeezing currents between vias and traces increases resistance and can cause slight drops in voltage at the converter's supply pins.

Finally, placement of power planes is critical—don't overlay the noisy digital plane over the analog plane, as they can still couple even if they are on different layers. To reduce the risk of degrading system performance, keep these types of planes separated and non-overlapping throughout each layer in the design if possible.

Stay tuned for Part 2, where power delivery and decoupling high-speed converters will be discussed.

To Learn More About High-Speed Layout http://dn.hotims.com/27761-101



Contributing Writer Rob Reeder is a senior converter applications engineer working in **Analog Devices high**speed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

Have a question involving a perplexing or unusual analog problem? Submit your question to: www.analog.com/ askrob

For Analog Devices' Technical Support, Call 800-AnalogD

SPONSORED BY

