RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Keeping Your A/D Converter Clocks Jitter Free

Q. How do I make improvements to my system clock or clock circuit so as to reduce jitter?

A. Jitter or noise on a clock signal can only corrupt an ADC's timing when present around the threshold region of the ADC's clock input. Increasing the slew rate of the clock signal decreases its transition time, thus reducing the amount of time that noise is present during the threshold period. This effectively reduces the amount of rms (root-mean-square) jitter introduced to the system. As an example, a 12-bit ADC requiring 100-fs minimum rms jitter for a 70-MHz analog input must have 1-V/ns slew rate.

So, minimizing jitter means improving the slew rate of the clock edge. One way to do this is to improve the clock source itself. A custom high-performance clock oscillator is typically used to characterize the baseline performance achieved by Analog Devices ADCs. Not all users of these high-speed converters can afford the cost or space required by a highperformance, oven-controlled, low-jitter oscillator, but available cost effective oscillators can achieve reasonable performance, even at high input frequencies. Care should be taken when selecting an "off-the-shelf" oscillator, though, as oscillator vendors do not always specify or measure jitter in the same way. A pragmatic way to determine which oscillator is best for the particular application is to collect a handful and test them in the system directly. By making this choice the only variable, performance can be predicted (assuming that the oscillator vendor maintains reasonable standards of quality control). Better yet is to contact the oscillator manufacturer to obtain



jitter- or phase noise data and get suggestions as to how to best terminate the device. Improper oscillator termination can seriously degrade the converter's spurious-free dynamic range (SFDR).

It is critical to understand the entire clock system in order to achieve the best possible performance from the converter. Decreasing the jitter of the system clock circuit can be achieved in many ways, including improving the clock source, as discussed, as well as filtering, frequency division, and proper choice of clock circuit hardware. Remember to pay attention to the slew rate of the clock, as this will determine the amount of noise that can corrupt the converter during the transition time. Minimizing this transition time can improve the converter's performance. Use only necessary circuitry to drive and distribute the clock because each component in the signal chain will increase the overall jitter. Finally, don't use "cheap" hardware; its performance is likely to be disappointing. One can't expect championship performance from a \$70,000 car outfitted with \$20 tires.

> To Learn More About Jitter Free Clocks

http://designnews.hotims.com/27744-100



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Have a question involving a perplexing or unusual analog problem? Submit your question to: raq@reedbusiness.com

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