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RAQ Issue 222: Analysis of Switch-Mode Power Supply and Rectification: Transistor Timing & Boost Capacitor Issues

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Question

Why am I having trouble getting a regulated output voltage when my input and output are close in value?

Answer

Having very large or very small duty cycles, especially at high switching frequencies, can cause timing violations, leading to degraded system performance.

Abstract

This article is the third article in a series where common switch-mode power supply (SMPS) design errors will be discussed as well as their appropriate rectification. This article aims to address complications that arise with the power stage design of DC-to-DC switching regulators, focusing on the power transistors and the boost capacitor. Power transistors have a minimum and maximum duty cycle that, when violated, will lead to worsened performance of the SMPS. Furthermore, when the boost capacitor is neglected, the transistors will not operate as intended.

Introduction

In this article, buck converters are used to demonstrate the effects of disregarding the timing specification of the power transistors, as well as what happens when the boost capacitor is removed. A detailed introduction to the operation of buck converters can be found in the first article of this series, "Analysis of Switch-Mode Power Supply and Rectification: Inductor Violations." The power transistors have a minimum on- and off-time to ensure proper charge and discharge of the FET's gate capacitor, ensuring that they fully turn on and off. When ignored (for faster switching speed, for example), issues begin to manifest themselves as unstable outputs and corrupted switching frequencies. Additionally, the boost capacitor is essential in maintaining the operation of these transistors. The absence of the boost capacitor will mean that the transistors will not have enough drive strength and will fail to fully turn on.

What Is a Boost Capacitor?

The boost capacitor is responsible for maintaining the proper functionality of the top N-channel MOSFET. This can be seen in Figure 1, highlighted in orange.

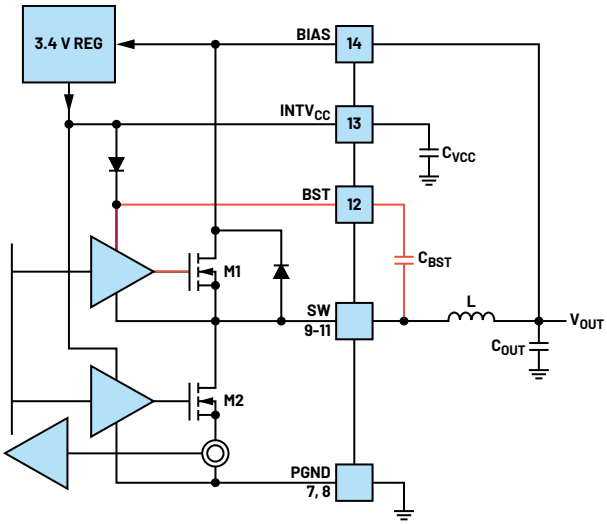

Figure 1. A block diagram from the LT8610 data sheet demonstrating the function of a boost capacitor.

When the top N-channel MOSFET is closed, the switch node is approximately at the same potential as the input source. This means that the source voltage of the top MOSFET is higher than the gate voltage (coming out of the gate driver). Without a positive gate to source voltage higher than the threshold voltage of the NMOS, the MOSFET cannot turn on. The boost capacitor is therefore used to always keep the gate voltage higher than the source voltage.

Neglecting the Boost Cap

Designers do not have a perceived advantage to leaving out the boost capacitor, but may do so to reduce BOM size and cost, or may simply forget to include these components, without realizing the downsides to this decision—the boost capacitor is necessary to help the chip provide enough voltage to the gate of the top FET to fully turn on, as seen in Figure 2.

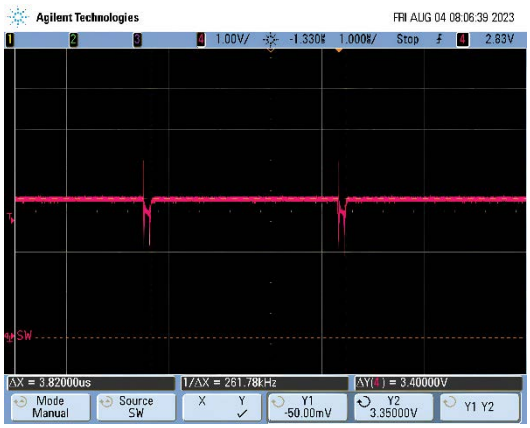

Figure 2. Switch node without boost capacitor.

If the top FET does not fully turn on, the device will not be able to regulate the output voltage. The FET will operate in its linear region, dissipating a large amount of power and heating up the chip.

To fix this, designers must add the boost capacitor. If designers are unsure about what value to add, they should choose a value in the data sheet example closest to their application. If a device needs a boost capacitor, forgetting to add it will lead to failure of the SMPS. Adding the boost capacitor will allow the top gate driver to have enough drive strength to operate the FET in its saturation region, allowing it to act as a switch, and provide the full input voltage to the SW node. This can be seen in Figure 3.

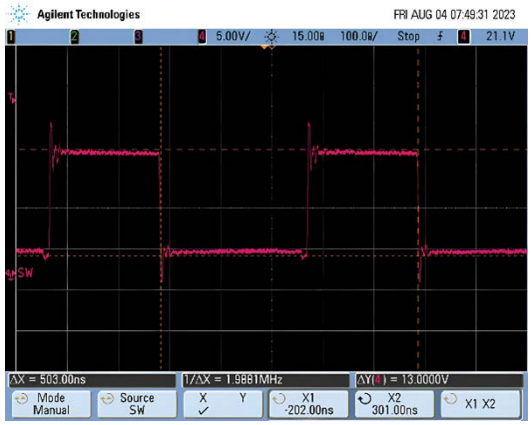

Figure 3. Switch node with boost capacitor.

Violating the Minimum On-Time Spec

Designers often opt for higher switching frequencies to achieve smaller board footprints at the expense of lower power efficiency due to the increased switching losses. However, when a device has a high frequency and a high step-down ratio, the duty cycle is forced to become small and could drop below the minimum duty cycle value. The minimum duty cycle shown in Equation 1.

$$D_{min} = t_{min-on} \times f_{switching} \quad (1)$$

Where t_{min-on} is defined as the minimum amount of time that the inductor is being charged by the input. Switching converters come with a specified minimum on-time value that the designers must adhere to for proper functionality of the FETs (as they cannot switch instantaneously). Designers are free to choose a switching frequency. However, when too high of a switching frequency and too large of a step-down ratio are specified, the on-time is forced below the minimum value.

When the on-time is forced below its minimum value, the inductor current will discharge faster than it charges in one period. As a new period begins, the starting point is lower than the previous cycles' starting point, which is known as current drooping. Eventually, both the current and output voltage droop so low that the device internally generates a bigger duty cycle (with a higher on-time) to regulate the output voltage, as demonstrated in Figure 4.

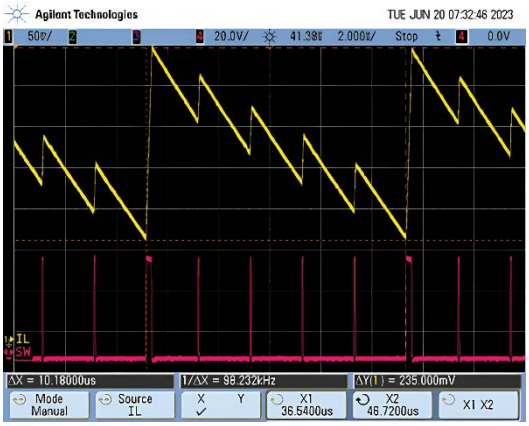

Figure 4. Violated minimum on-time current waveform.

This droop of the inductor current ripple manifests itself in the converter's output voltage as well. The output voltage ripple becomes noisier, which could affect sensitive loads and worsen EMI performance. This effect can be seen in Figure 5.

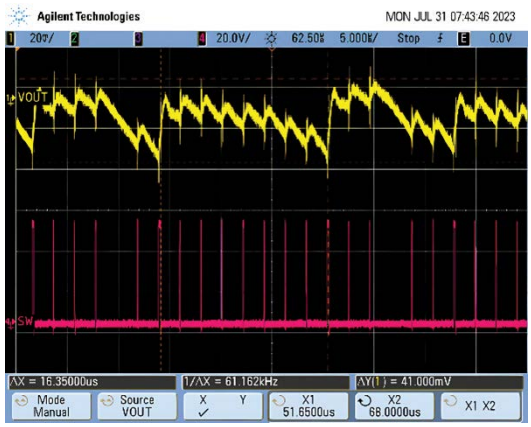

Figure 5. Violated minimum on-time output waveform.

This issue has an easy solution. Since the on-time is influenced primarily by the switching frequency, designers can rectify the issue by decreasing the frequency. This comes at the expense of needing larger power stage components, primarily a larger inductor. The improved functionality of the buck converter can be seen in the consistent on-time between periods, as well as the stable current ripple in Figure 6 and the stable output ripple in Figure 7.

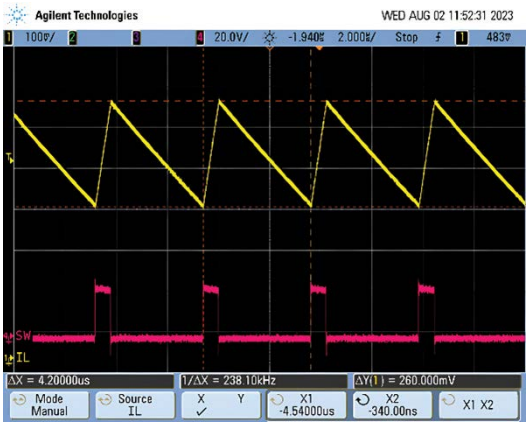

Figure 6. Stable current ripple.

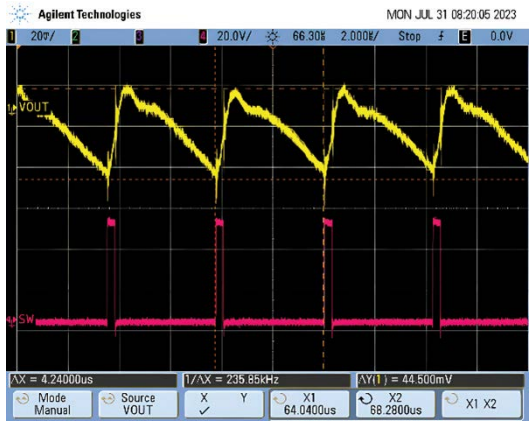

Figure 7. Stable output ripple.

Violating the Minimum Off-Time Spec

Some applications may require small step-down rations, which risks violating a converter's minimum off-time specification. $t_{min-off}$ is the complement of t_{min-on}, and it is the minimum time the inductor is not being charged by the input. Like the on-time requirement, the SMPS must be turned off for a set period to ensure proper functionality of the FETS (allowing proper discharge). The minimum off-time spec is violated when the demanded duty cycle is larger than the maximum duty cycle allowed, given by Equation 2.

$$D_{max} = 1 - (t_{min-off} \times f_{switching}) \quad (2)$$

If the duty cycle exceeds the maximum value, the SMPS will fold back the frequency that it was configured for to avoid violating the minimum off-time spec. This can be seen in Figure 8. The device was initially configured for 2 MHz.

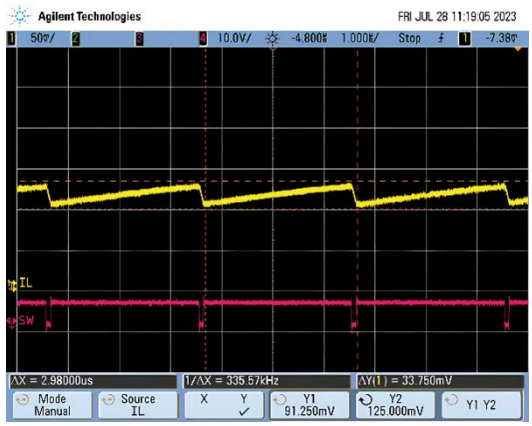

Figure 8. Violated minimum off-time current waveform. Frequency folds back to 335 kHz.

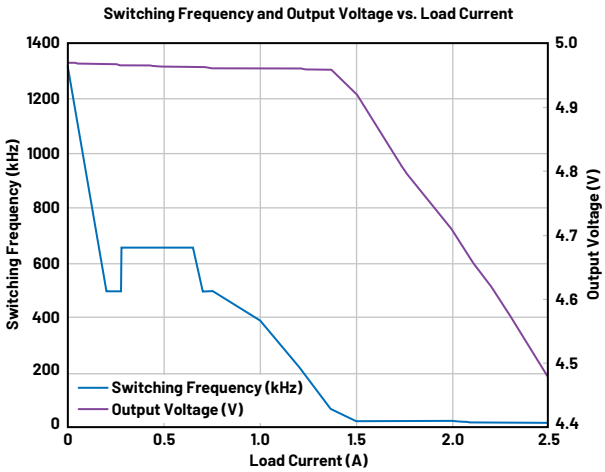

Figure 9. Load regulation and foldback frequency. As the load increases, the frequency folds back to maintain a regulated output voltage.

In Figure 9, the device is shown to fold back the frequency to maintain a constant output voltage as the load increases. The device operated in DCM up until about 0.28 A, which is why the frequency drops to about 495 kHz before rising back up to 657 kHz. The device can maintain proper operation running at 657 kHz until drawing a load of 0.7 A. The frequency decreases to maintain the proper output voltage until the load draws around 1.4 A. When this happens, the device cannot decrease the frequency below 100 kHz (the minimum specified feedback frequency for the part) while maintaining the output voltage, so the output voltage begins to droop.

The solution for this issue is not as simple as the minimum on-time violation. Since designers often have a set input voltage and set output voltage, the duty cycle cannot be changed to allow for a longer off-time. If they can provide a larger input voltage, the part will operate at the set frequency since the smaller duty cycle will prevent the part from violating the minimum off-time. This can be seen in Figure 10, where the part operates at its set 2 MHz.

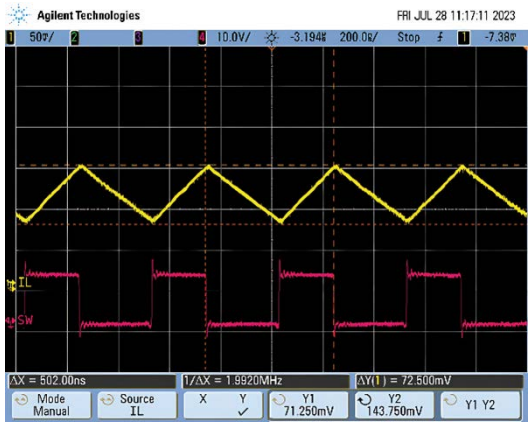

Figure 10. Unviolated minimum off-time current waveform. Set frequency is 2 MHz.

In contrast to the minimum on-time, lowering the frequency will only work up to a certain load. If the designer cannot sufficiently lower the switching frequency to prevent violating the minimum off-time spec, the best course of action is to choose a different part that can handle higher duty cycles and shorter on-times.

Conclusion

This article, which concludes a series on common SMPS design errors, is focused on maintaining the proper function of the power transistor. Demanding too high or too low of a duty cycle will destabilize the switching converter, leading to undesirable consequences such as a lower switching frequency, unregulated output voltage, and undesirable performance of the inductor with regard to the current. Furthermore, neglecting the boost capacitor can not only impede the transistor's normal operation, but can also lead to fatal outcomes for the load, transistor, or chip itself.

About the Author

Abe Ibraheim is a central applications intern who joined Analog Devices in the summer of 2023. Abe is a rising third-year student at Worcester Polytechnic Institute, pursuing a bachelor's and a master's degree in electrical and computer engineering. His concentration is in microelectronics and power systems.

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Kenneth Armijo joined Analog Devices in 2022 as an associate engineer in central applications. He holds two bachelor's degrees from Worcester Polytechnic Institute in electrical engineering and robotics engineering, as well as a master's degree in electrical engineering. He specializes in the design and implementation of power management circuits, mainly switching regulators.

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