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AnalogDialogue

RAQ Issue 209: How to Combine a Low-Pass Filter and an ADC Driver for a 20 V p-p Signal

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Question:

Why combine a low-pass filter (LPF) and an analog-to-digital converter (ADC) driver?

Answer:

To reduce the size and cost of an analog signal chain and provide ADC antialiasing protection (ADC input signals in a frequency band around the ADC's sampling frequency are not protected by a digital filter and must be attenuated by an analog low-pass filter, LPF). A typical application for a 20 V p-p LPF driver is in industrial, scientific, and medical (ISM) equipment that must digitize a legacy 20 V p-p signal range using a high speed ADC with a lower full-scale input.

Introduction

Driving an ADC for an optimum mixed-signal performance is a design challenge. Figure 1 shows a standard driver-ADC circuit. During ADC acquisition time, the sampling capacitor kicks back an exponentially decaying voltage and current into the RC filter. A mixed-signal ADC driver circuit optimum performance depends on multiple variables. The driver's settling time, the RC filter's time constant, driving impedance, and the ADC sampling capacitor's kickback current interact during acquisition time and contribute sampling errors. Sampling errors increase directly with the number of ADC bits, input frequency, and sampling frequency.

The standard ADC driver has a large sample of experimental data to use for a reliable design procedure. There is a lack of lab data to guide the design of a low-pass filter that drives an ADC. This article features an LPF driver circuit that combines analog low-pass filtering, signal compression, and an ADC driver (see Figure 2).

Table 1 lists the performance variables of the circuit shown in Figure 2. The following laboratory data and analysis are a guide to the time and frequency response limits of the circuit shown in Figure 2.

Table 1. The Performance Variables of the Circuit Shown in Figure 2

LPF Driver	RC Filter	ADC
–3 dB bandwidth, stop-band attenuation, settling time, noise, THD	Resistor value, RC time constant	Sampling frequency, number of bits, acquisition time, SNR, THD

Laboratory Data and Analysis

Two of the significant parameters to measure the dynamic performance of a system are the signal-to-noise ratio (SNR) and total harmonic distortion (THD). Optimum performance is the result of a combination of an ADC and the signal conditioning stage, which for this article, includes the third-order low-pass filter and the single-ended to differential converter. The –3 dB bandwidth and settling time of the LPF driver circuit shown in Figure 2 were varied and the SNR and THD measurements are listed in tables 2 to 5. The variables tested and the implication to the system's performance will be discussed in this article.

Low-Pass Filter –3 dB Bandwidth

A 1 MHz signal BW is compared to the performance at twice and half of the 1 MHz BW. The –3 dB points are 558 kHz, 1 MHz, and 2.3 MHz, and the performance is shown in Table 2. Lowering the cutoff frequency to 558 kHz lowers the LPF noise bandwidth and increases the SNR. Increasing the cutoff frequency to 1 MHz or 2.3 MHz decreases the LPF driver settling time and lowers the THD.

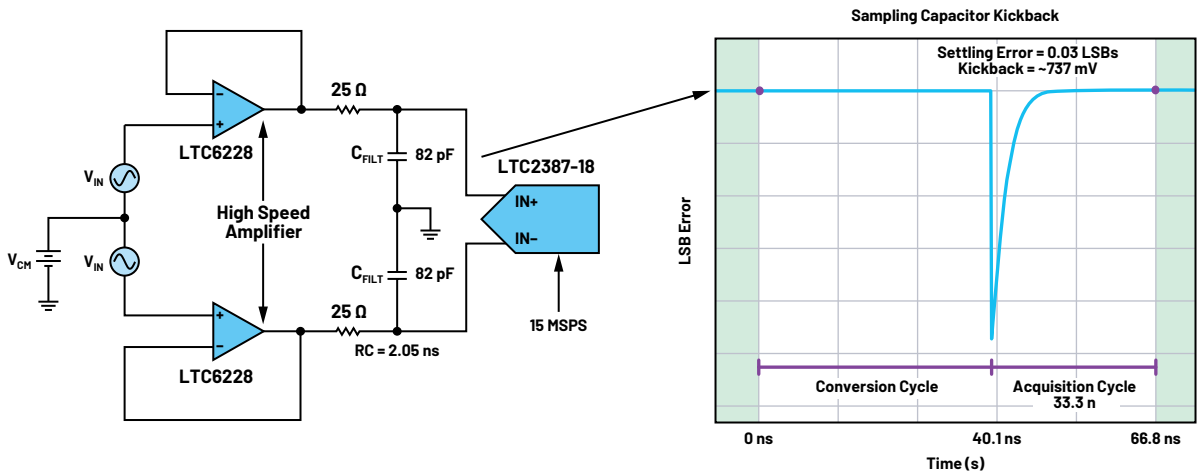

Figure 1. A standard ADC driver and RC filter.

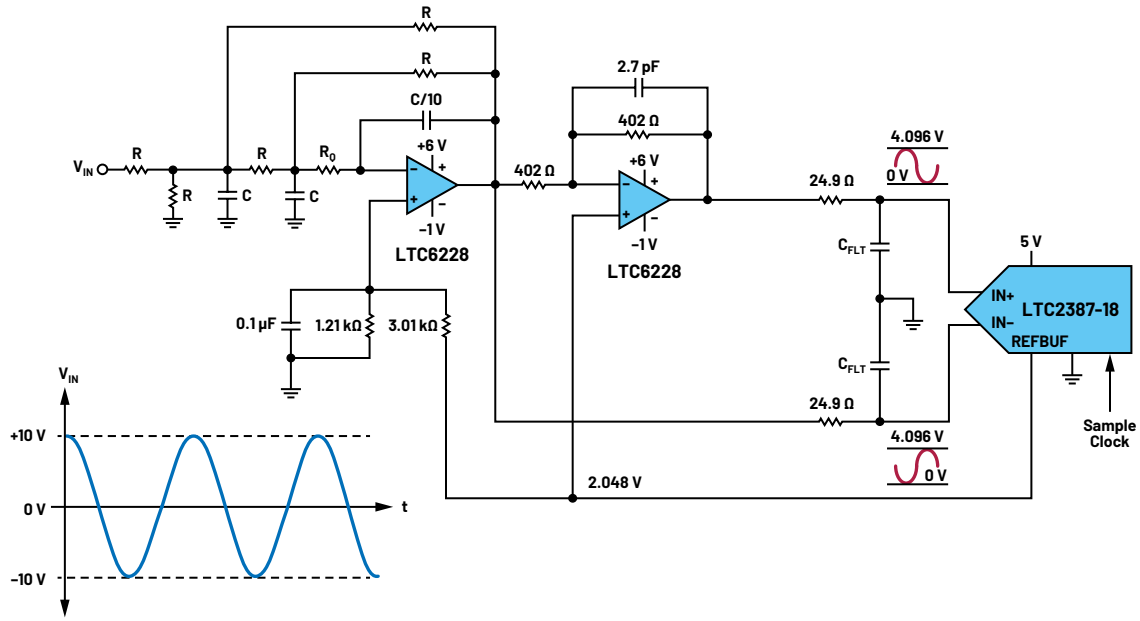

Figure 2. An LPF driver and ADC circuit.

Table 2. LPF Driver Performance for Three Cutoff Frequencies, R = 750 Ω

V_{IN} (V p-p)	F_{IN} (kHz)	–3 dB Frequency	RQ	LPF Driver C	LPF Driver R	SNR	THD
20	2	558 kHz	150 Ω	2700 pF	750 Ω	90 dB	–98 dB
		1 MHz		1500 pF		90 dB	–103 dB
		2.21 MHz		680 pF		88 dB	–106 dB

Table 3. LPF Driver Performance for Three Cutoff Frequencies, R = 412 Ω

V_{IN} (V p-p)	F_{IN} (kHz)	–3 dB Frequency	RQ	LPF Driver C	LPF Driver R	SNR	THD
20	2	580 kHz	150 Ω	4700 pF	412 Ω	91 dB	–98 dB
		1 MHz		2700 pF		90 dB	–97 dB
		2.25 MHz		1200 pF		89 dB	–99 dB

The cutoff frequency can be varied by changing either R or C in Figure 2. The LPF driver THD is lower when the C capacitor is used to set the cutoff frequency and the SNR is slightly improved if the R resistor is lowered. This is shown in Table 3.

Setting The RQ Resistor (Figure 2)

The RQ resistor of the LPF sets the time response. A higher RQ has higher overshoot and longer settling time. A lower RQ has lower overshoot and shorter settling time. Figure 3 shows the LPF transient response for a 150 Ω and 75 Ω RQ resistor. The LPF driver has been tested with different RQ and the result is shown in Table 4.

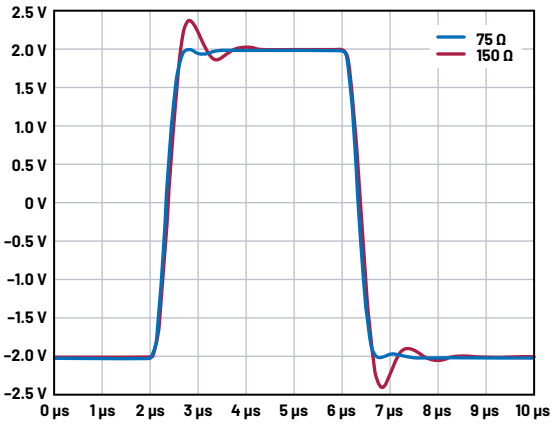

Figure 3. Overshoot and settling time for different RQ values.

Table 4. LPF Driver Performance for Different RQ Values

V_{IN} (V p-p)	Sampling Rate (MSPS)	–3 dB Frequency	RQ	LPF Driver C	LPF Driver R	SNR	THD
20	10	558 kHz	150 Ω	2700 pF	750 Ω	90 dB	–98 dB
			75 Ω			90 dB	–97 dB
		1 MHz	150 Ω	1500 pF		89 dB	–102 dB
			75 Ω			89 dB	–100 dB
		2.3 MHz	150 Ω	680 pF		88 dB	–106 dB
			75 Ω			88 dB	–106 dB

Based on the actual measured data, using RQ of 75 Ω and 150 Ω has no significant impact on the SNR and THD performance and is only a factor for overshoot and settling time.

ADC Sampling Rate

The data in Table 5 shows that the THD performance of the system is lower using LTC2387-18 at 10 MSPS than 15 MSPS (the RC drive capacitors C3 and C4 of Figure 2 are 180 pF for 10 MSPS).

Note: The acquisition time of an LTC2387-18 and LTC2386-18 at 10 MSPS is 61 ns and 50 ns respectively.

Table 5. LPF Driver Performance for 10 MSPS and 15 MSPS Sampling Rate

V_{IN} (V p-p)	Sampling Rate (MSPS)	–3 dB Frequency	RQ	LPF Driver C	LPF Driver R	SNR	THD
20	15	1 MHz	150 Ω	1500 pF	750 Ω	88 dB	–96 dB
	10					89 dB	–101 dB
	15	2.3 MHz	75 Ω	680 pF		88 dB	–93 dB
	10					88 dB	–106 dB

RC Filter

The RC filter between the driver and the ADC is used for bandwidth limiting to ensure low noise over wide bandwidth and to get better SNR. The RC value determines the –3 dB cutoff frequency. Lowering R can sometimes result to ringing and instability. Increasing the R increases the sampling error. Using lower values for C will result in higher charge kickback but will allow faster charging time. A higher C value will give lower charge kickback but will also result in slower charging time. In addition, setting the values of RC is critical to ensuring that the sample is settled within the given acquisition time. Using the data sheet's recommended value and the suggested value from the Precision ADC Driver Tool will be a great starting point.

The Precision ADC Driver Tool is a comprehensive tool that can help to predict system performance when using different RC values between the driver and ADC. Some of the parameters that can be checked using this tool are the charge kickback when sampling error and the acquisition time.

To achieve a lower –3 dB cutoff frequency by using 25 Ω and 180 pF RC, the settling of the input signal and the charge kickback are affected. To have a lower –3 dB cutoff frequency and to ensure the input signal is properly settled within the acquisition period, using a lower sampling rate can be an option. From the LTC2387-18 data sheet, the acquisition time is typically cycle time minus 39 ns. Optimizing the

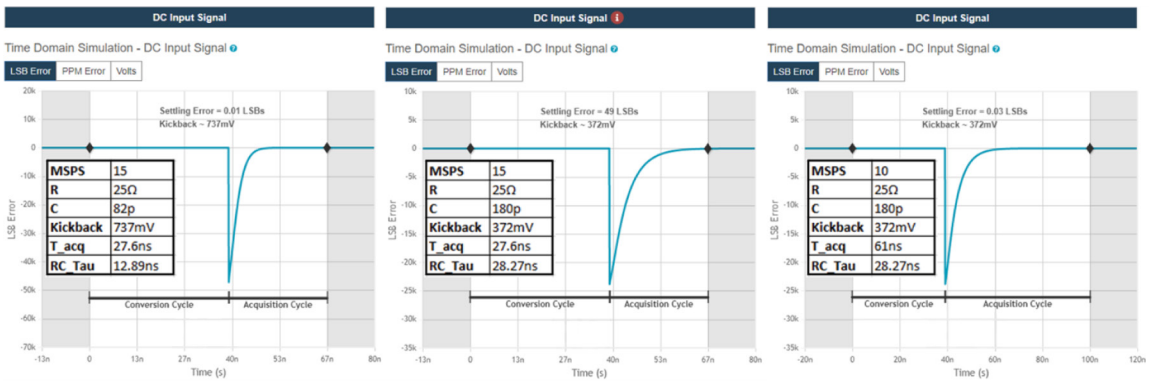

Figure 4. Charge kickback, RC_Tau, acquisition time for different sampling rates: (a) 15 MSPS sampling rate and using recommended RC values for LTC2387-18 (25 Ω and 82 pF), (b) 15 MSPS sampling rate and using recommended RC values for LTC2386-18 (25 Ω and 180 pF), and (c) 10 MSPS sampling rate using recommended RC values for LTC2386-18 (25 Ω and 180 pF).

LTC2387-18 at 15 MSPS results in a 27.67 ns acquisition time, while using this part at 10 MSPS results in a 61 ns acquisition time.

With the aid of the Precision ADC Driver Tool, Figure 4a to 4c summarize the kickback differences and RC time constant (Tau) when using different RC values and the acquisition time for a 10 MSPS and a 15 MSPS sampling rate. Figure 4a shows the settling response using recommended RC values of 25 Ω and 82 pF at a 15 MSPS sampling rate for LTC2387-18. Figure 4b shows a higher RC time constant when using C of 180 pF and that prevents the input from settling within the acquisition time of 27.6 ns for a 15 MSPS sampling rate. Figure 4c uses the same RC from Figure 4b (25 Ω and 180 pF) but the signal is able to settle after acquisition time increases to 61 ns when using a 10 MSPS sampling rate.

LPF Driver Resistor Selection

The –3 dB cutoff frequency of the LPF driver can be achieved by changing either R or C. One of the contributors to the total system noise is the noise from the resistors. From the formula for noise computation, the resistor noise can theoretically be reduced by lowering the resistance value. For this activity, two resistor values have been tried as LPF Driver R, 750 Ω, and 412 Ω. It is theoretically expected that SNR will be better when R is lower but from the gathered data, as seen in Table 2 and Table 3, the SNR doesn't indeed improve much but instead, there is a more noticeable effect on THD performance.

The lower the LPF resistance (R in Figure 1), the higher the current requirement needed from the amplifier. Using lower value resistors, the op amp output current is higher than a maximum linear current driving capability.

Amplifier Driver Selection

Best specifications for optimum performance of the parts are critical in the selection of ADC driver to be used. Two ADC drivers have been used on data gathering, the ADA4899-1 and LTC6228. These ADC drivers are good options for driving the LTC2387-18, which has been used for lab measurements. Some of the specifications that have been considered in the selection of ADC driver are the BW, voltage noise, harmonic distortion, and the current drive capability. Based on the tests done, in terms of THD and SNR, the ADA4899-1 and LTC6228 have a negligible difference in performance.

LPF Design and Application Guide

Figure 5 shows the LPF circuit. Five equal resistors (R1 to R5), one resistor (RQ) for adjusting LPF time response, two equal capacitors to ground (C1 and C2), and a feedback capacitor (C3) that is one-tenth the value of a grounded capacitor complete the set of the LPF passive components (±1% resistors and ±5% capacitors).

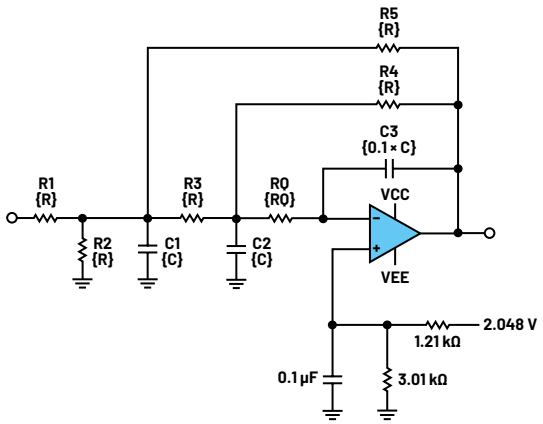

Figure 5. The LPF circuit.

A Simple LPF Design Procedure (Note 1)

R1 to R5 = R, C1 and C2 = C.

For minimum distortion, resistors R1 to R5 must be in the range 600 Ω to 750 Ω.

- Set R = 750 Ω
- C = 1.5E9/$f_{3\,dB}$ nearest standard 5% capacitor in pF, $f_{3\,dB}$ is the LPF –3 dB frequency (Note 2).
- For example: If $f_{3\,dB}$ is 1 MHz, then C = (1.5E9)/(1E6) = 1500 pF.
- C3 = C/10
- RQ = R/5 or R/10 (notes 3 and 4)

Note 1. A simple filter design requires only a calculator and dispenses with nonlinear s-domain equations.

Note 2. If R = 619 Ω, then C = 1.8E9/$f_{3\,dB}$, $f_{3\,dB}$ is the LPF –3 dB frequency.

Note 3. RQ = R/5 for maximum stop-band attenuation or R/10 for low overshoot and fast settling.

For RQ/5 and RQ/10, the stop-band attenuation is –70 dB and –62 dB, respectively, at 10× $f_{-3\,dB}$.

Note 4. If RQ = R/10, then the –3 dB frequency is 7% lower than for RQ = R/5 so, R1 to R5 is 0.93× the R for RQ/5.

Note 5. The PCB trace distance from the LPF driver differential output to the ADC input must be 1" or less.

Note 6. The LPF op amp's V_{CC} and V_{EE} are 6 V and –1 V, respectively, for an output linear voltage swing 0 V to 4.098 V.

Conclusion

The SNR and THD data of tables 2 to 5 provide insight into the performance of the circuit shown in Figure 2. Lowering the LPF bandwidth by increasing capacitors increases the SNR (lower LPF noise BW). A lower LPF bandwidth increases distortion (because the LPF settling time is longer than required for minimum sampling errors). In addition, if the LPF resistors values are too low, then the THD decreases because the LPF op amp drives the feedback resistors and the inverting op amp input resistor (at a higher op amp output current, distortion increases).

Using a 10 MSPS sampling frequency for the LTC2387-18 ADC, the LPF pass band must be 1 MHz or higher to minimize THD. Setting the LPF at 1 MHz is an arbitrary compromise for SNR, THD, and adequate ADC aliasing protection.

Design References: ADI's Precision ADC Driver Tool

Featured Devices

Op Amps

Part Number	V_{OS} (V) Max	I_{BIAS} (A) Max	GBP (Hz) typ	V_{NOISE} (V/√Hz) typ	THD 2 V p-p, RL = 1k	V_S Span min/max (V)
ADA4899-1	35 µV	–12 µA	600 MHz	1 nV/√Hz	–117 dBc at 1 MHz	±5 V
LTC6228/ LTC6229	20 µV	–16 µA	890 MHz	0.88 nV/√Hz	–120 dBc at 1 MHz	±5 V

Analog-to-Digital Converter

Part Number	Resolution (Bits)	Max F_S	Input Type (SE, Diff.)	V_{IN} Span (V_{MIN}/V_{MAX})	SNR (dB)	INL (LSB)	Data Out Interface
LTC2387	18	15 MSPS	Single-ended, differential	$-V_{REFBUF}$ to $+V_{REFBUF}$	95.7	±0.6	Serial LVDS interface

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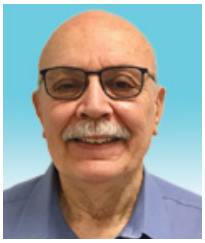

About the Author

Philip Karantzalis has worked in testing and designing analog signal circuits and systems since 1973. In 1986, he joined the Analog Devices, Inc. Signal Conditioning Group providing baseband signal designs for data acquisition, RF modulators, demodulators and mixers, ADCs, and high accuracy test systems. Philip is currently a senior applications engineer with the Precision Systems Group of Analog Devices. He is a graduate of RCA Institutes of Electronics in New York City and has studied advanced mathematics at San Francisco State University.

About the Author

Frances de la Rama joined Analog Devices as a technician in 2007. He pursued his degree in electronics engineering from 2014 to 2019 through ADI's Continuing Educational Program (CEP). He graduated from Technological University of the Philippines—Taguig. In 2019, he became part of the Philippine Development Center (PDC, formerly known as Design, Layout, and Applications) under the Product Applications Team at ADI. On his early engagements, his tasks and role were mainly aligned to linear products and solutions, focusing on amplifiers. Now, he focuses on battery formation and test (BFT) with ADBT100x as the core product.