Vol 56, No 1—March 2022

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

AnalogDialogue

RAQ Issue 199: Three Compact Solutions for High Step-Down Voltage Ratios

Olivier Guillemant, Central Applications Engineer

Question:

What are some methods for achieving a compact design under high step-down voltage ratios?

Answer:

This article will address why the nonisolated DC-to-DC buck converter (referred to simply as buck converter in this article) is facing serious challenges to downconverting high DC input voltages to very low output voltages at high output current. Three different approaches will be presented for downconverting steep voltage ratios while keeping a small form factor.

Introduction

System designers can be faced with the challenge of downconverting high DC input voltages to very low output voltages at high output current (such as 60 V down to 3.3 V at 3.5 A), while maintaining high efficiency, small form factor, and simple design.

Combining high input-to-output voltage difference with high current automatically excludes the linear regulator due to the excessive power dissipation. Consequently, the designer must opt for a switching topology under these conditions. However, even with such topologies, it is still challenging to implement a design that is sufficiently compact for space-restricted applications.

Challenges Faced by DC-to-DC Buck Converters

One candidate for high step-down ratios is the buck converter because it is the topology of choice when having to step down an input voltage to a lower output voltage (such as V_{IN} = 12 V down to V_{OUT} = 3.3 V) in an efficient way, with a significant amount of current while also using a small footprint. However, there are conditions under which the buck converter faces serious challenges to keep its output voltage regulated. To understand these challenges, we must remember that the simplified duty cycle (D) of a buck converter operating in continuous conduction mode (CCM) is:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

Now, the duty cycle also relates to the switching frequency (f_{SW}) in the following way, where the on-time (t_{ON}) is the duration over which the control FET stays on during each switching period (T):

$$D = \frac{t_{ON}}{T} = t_{ON} \times f_{SW} \quad (2)$$

Combining Equation 1 and Equation 2 shows how t_{ON} is influenced by the step-down voltage ratio and f_{SW}:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (3)$$

Equation 3 tells us that the on-time decreases when the input-to-output voltage ratio (V_{IN}/V_{OUT}) and/or f_{SW} increase. This means that the buck converter must be able to operate with very low on-time to regulate the output voltage in CCM under high V_{IN}/V_{OUT} ratio, and it becomes even more challenging with a high f_{SW}.

Let's consider an application with $V_{IN(MAX)}$ = 60 V, V_{OUT} = 3.3 V at $I_{OUT(MAX)}$ = 3.5 A. When required, we shall use values from the LT8641 data sheet because a solution with the LT8641 will be provided in a later section. The required minimum on-time ($t_{ON(MIN)}$) corresponds to the highest input voltage ($V_{IN(MAX)}$). In order to assess this $t_{ON(MIN)}$, it is advised to make Equation 3 more accurate. By including $V_{SW(BOT)}$ and $V_{SW(TOP)}$, the voltage drops for the two power MOSFETs of the buck converter, and replacing V_{IN} with $V_{IN(MAX)}$ we obtain:

$$t_{ON(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{V_{IN(MAX)} - V_{SW(TOP)} + V_{SW(BOT)}} \times \frac{1}{f_{SW}} \quad (4)$$

Using Equation 4 with $V_{IN(MAX)}$, f_{SW} = 1 MHz, we obtain a $t_{ON(MIN)}$ of 61 ns. For $V_{SW(BOT)}$ and $V_{SW(TOP)}$, we made use of the values provided for $R_{DS(ON)(BOT)}$ and $R_{DS(ON)(TOP)}$ in the LT8641 data sheet, knowing as well that $V_{SW(BOT)} = R_{DS(ON)(BOT)} \times I_{OUT(MAX)}$ and $V_{SW(TOP)} = R_{DS(ON)(TOP)} \times I_{OUT(MAX)}$.

Buck converters can rarely guarantee a $t_{ON(MIN)}$ with the short value of 61 ns obtained above; therefore, the system designer is forced to search for alternative topologies. There are three possible solutions for high step-down voltage ratios.

Three Compact Solutions for $V_{IN(MAX)}$ = 60 V, V_{OUT} = 3.3 V at $I_{OUT(MAX)}$ = 3.5 A

Solution 1: Using the LT3748 Non-opto Flyback

The first option consists of using an isolated topology, where the transformer performs most of the downconversion thanks to its N:1 turn ratio. For that matter, Analog Devices offers flyback controllers such as the LT3748 that do not require a third transformer winding or opto-isolator, making the design simpler and compact. The LT3748 solution for our conditions is presented in Figure 1.

Even though the LT3748 solution simplifies the design and saves space compared with a standard flyback design, a transformer is still required. For applications where isolation between input and output sides is not required, it is preferred to avoid this component, which adds complexity and increases the form factor vs. a nonisolated solution.

Solution 2: Using the LTM8073 and LTM4624 µModule Devices

As an alternative, the designer can downconvert in two steps. To achieve a reduced component count of only 10, two µModule® devices and eight external components can be used, as demonstrated in Figure 2. Moreover, the two µModule devices already integrate their respective power inductor, sparing the system engineer a design task that is rarely straightforward. The LTM8073 and LTM4624 both come in BGA packages, with respective dimensions of 9 mm × 6.25 mm × 3.32 mm and 6.25 mm × 6.25 mm × 5.01 mm (L × W × H), providing a solution with a small form factor.

Since the LTM4624 exhibits an efficiency of 89% under these conditions, the LTM8073 supplies at most 1.1 A to the input of the LTM4624. Given that the LTM8073 can provide up to 3 A of output current, it can be used to supply other circuit rails. It is with this purpose in mind that we selected 12 V as the intermediary voltage (V_{INT}) in Figure 2.

Despite avoiding the usage of a transformer, some designers might be reluctant to implement a solution that requires two separate buck converters, especially if no intermediary voltage is required to supply other rails.

Solution 3: Using the LT8641 Buck Converter

Consequently, in many cases, using a single buck converter would be preferred because it provides the optimal solution to combine system efficiency, a small footprint, and design simplicity. But did we not just demonstrate that buck converters cannot cope with high V_{IN}/V_{OUT} combined with high f_{SW}?

This statement might apply to most buck converters, but not to all of them. The ADI portfolio includes buck converters such as the LT8641, which is specified with a very short minimum on-time of 35 ns typical (50 ns max) over the full operating temperature range. Those specifications are safely below the required minimum on-time of 61 ns previously calculated, providing us with a third possible compact solution. Figure 3 shows how simple the LT8641 circuit can be.

It is also worth noting that the LT8641 solution can be the most efficient of the three. Indeed, if efficiency must be further optimized compared with Figure 3, we can decrease f_{SW} and select a bigger inductor size.

Although f_{SW} can also be decreased with Solution 2, the integration of the power inductors does not offer the flexibility to increase the efficiency beyond a certain point. Moreover, the use of two consecutive downconversion stages has a small negative impact on the efficiency.

In the case of Solution 1, the efficiency will be very high for a flyback design, thanks to the operation in boundary mode and to all components removed with the no-optical feedback design. However, the efficiency cannot be fully optimized because there is a limited number of transformers to select from, as opposed to the broad portfolio of inductors available for Solution 3.

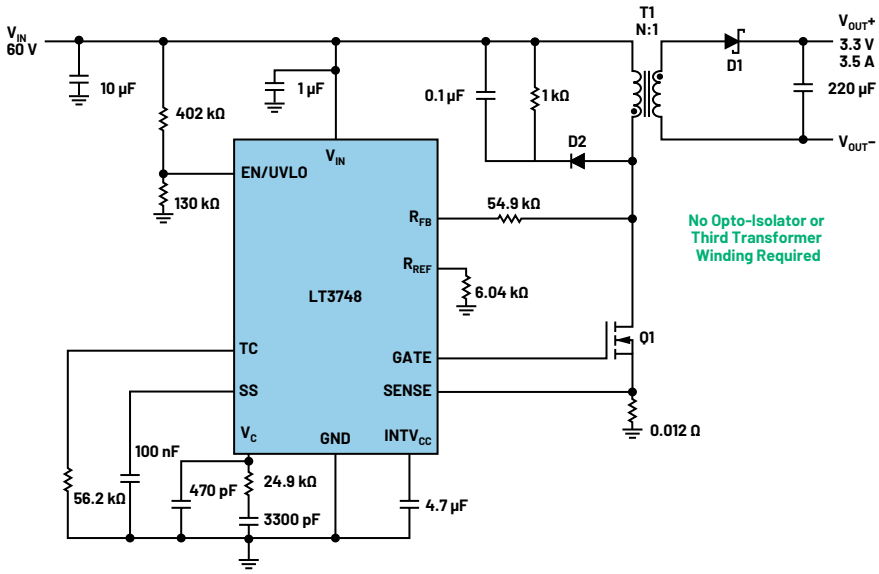

Figure 1. A circuit solution with the LT3748 downconverting 60 V input to 3.3 V output.

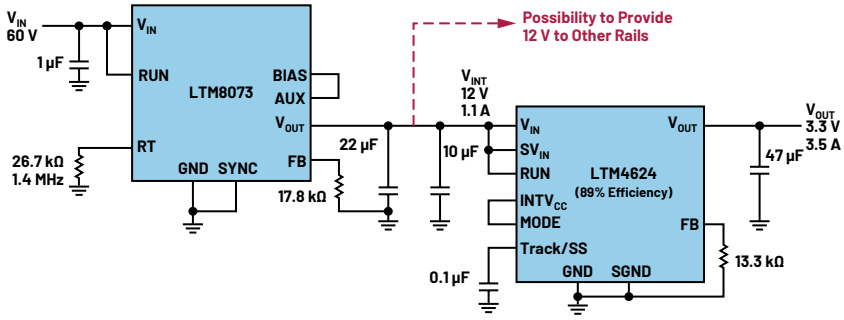

Figure 2. A circuit solution with the LTM8073 and LTM4624, downconverting 60 V input to 3.3 V output.

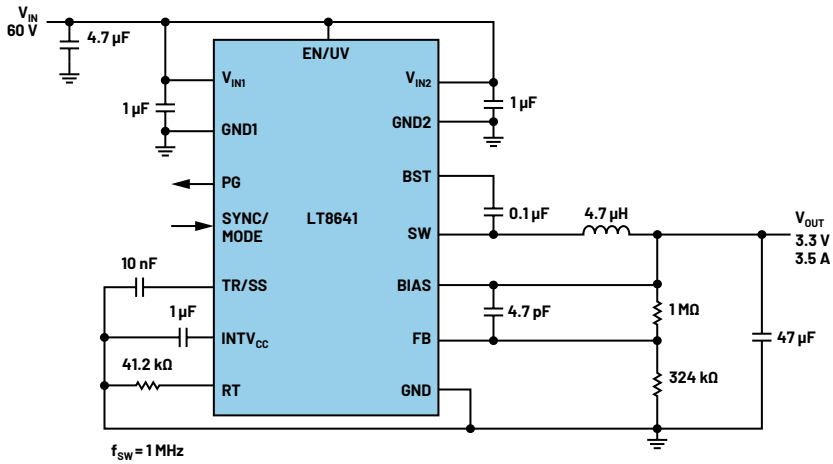

Figure 3. A circuit solution with the LT8641 downconverting 60 V input to 3.3 V output.

An Alternative Way to Check Whether LT8641 Fulfills Requirements

In most applications, the only adjustable parameter in Equation 4 is the switching frequency. Consequently, we reformulate Equation 4 to assess the maximum permitted f_{SW} for the LT8641 under given conditions. By doing this, we obtain Equation 5, which is also provided on page 16 of the LT8641 data sheet.

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)} \times (V_{IN(MAX)} - V_{SW(TOP)} + V_{SW(BOT)})} \quad (5)$$

Let's use this equation with the following example: V_{IN} = 48 V, V_{OUT} = 3.3 V, $I_{OUT(MAX)}$ = 1.5 A, f_{SW} = 2 MHz. An input voltage of 48 V is commonly found in automotive and industrial applications. By inserting those conditions in Equation 5, we obtain:

$$f_{SW(MAX)} = \frac{5\ \text{V} + 0.0825\ \text{V}}{50\ \text{ns} \times (48\ \text{V} - 0.1575\ \text{V} + 0.0825\ \text{V})} = 2.12\ \text{MHz} \quad (6)$$

Therefore, under the provided application conditions, the LT8641 would operate safely with f_{SW} set as high as 2.12 MHz, confirming that the LT8641 is a good choice for this application.

Conclusion

Three different methods were presented to achieve a compact design under high step-down voltage ratios. The LT3748 flyback solution does not require a bulky opto-isolator and is recommended for designs where isolation is necessary between input and output sides. The second method, which involves implementing the LTM8073 and LTM4624 µModule devices, is of particular interest when the designer is hesitant to select the optimal inductor for the application and/or when an additional intermediary rail must be supplied. The third method, a design based on the LT8641 buck converter, offers the most compact and simplest solution when the sole requirement is the steep voltage downconversion.

About the Author

Olivier Guillemant is a central applications engineer at Analog Devices in Munich, Germany. He provides design support for the Power by Linear portfolio for European broad market customers. He has held various power application positions since 2000 and joined ADI in 2021. He received his M.Sc. in electronics and telecommunications from University of Lille, France. He can be reached at olivier.guillemant@analog.com.