

AnalogDialogue

RAQ Issue 189: Isolation for SAR ADCs

Wilfried Platzer, Applications Engineer

Question:

How do I add isolation to my ADC without harming its performance?



Answer:

For isolated high performance ADCs, keep one eye on isolated clocks and a second on isolated power.

SAR ADCs have traditionally been used for lower sample rates and lower resolution. Nowadays, fast, high precision, 20-bit SAR ADCs sampling at 1 MSPS like the LTC2378-20 and oversampled SAR ADCs with 32-bit resolution like the LTC2500-32 are available. When designing for high performance to utilize the ADC performance, very low noise is required across the complete signal chain. When additional isolation is required for a signal chain, performance will be impacted.

There are three isolation topics to consider:

- Isolated power to ensure the hot side is powered
- Data isolation to ensure the datapath is isolated
- Clock isolation for the ADC (sample clock or conversion signal), in case the clock is not generated at the hot side

Isolated Power (Comparison Between Flyback and Push-Pull Topology)

For sensor applications, isolated power is usually in a less than 10 W range.

Flyback converters are widely chosen to isolate power. Figure 1 shows the simplicity of a flyback converter. The topology's advantage is that only a few external components are required. Flyback converters have only one integrated switch. This switch can be the main noise source impacting signal chain performance. For high performance analog design, the flyback converter comes with many high discontinuities in the form of electromagnetic radiation called EMI, which can limit the performance of your circuit.



Figure 1. A typical flyback converter topology.

Figure 2 shows the current in transformers L1 and L2. The currents jump from high values to zero in a short period of time in the primary (L1) and secondary (L2) windings. The current spikes can be seen in the I(L1)/I(L2) traces in Figure 3. Current and energy are built up in the primary inductance and they are transferred while the switch is off to the secondary inductance, which creates transients. Those transients of the switching noise effects need to be reduced, and, consequently, snubbers and filters must be inserted in the design. Aside from the additional filters, an additional disadvantage of the flyback topology is that the utilization of the magnetic material is low, leading to larger transformers due to the required high inductances. Furthermore, the hot loops of the flyback converter are large and not easy to manage. For background information on hot loops, please read Application Note AN139.



Another challenge of the flyback converter involves the switching frequency change. Figure 3 shows a frequency change due to load change. As seen in Figure 3a, t1 < t2. This means that f_{SWITCH} is when the load current decreases from the higher load current I1 to the lower load current I2. The variations in frequency create internal noise at unpredictable times. In addition, the frequencies also will differ from part to part, which will make it more difficult to filter them as adjusted filtering would be required for each individual PCB. Taking a 20-bit SAR ADC, with a 5 V input span, one LSB corresponds to \sim 5 μ V. The errors introduced through EMI noise should be below 5 μ V, which means that a flyback topology should not be selected when isolating power for a precision system.

There are other isolated power architectures with lower radiating emissions. Push-pull converters are much better suited in respect to radiation compared to flyback converters. A push-pull regulator like the LT3999 offers the possibility of clock synchronization to the ADC and helps to achieve high performance. Figure 4 shows the LT3999 in an isolated power circuit with synchronization to an ADC sampling clock. Remember that the primary to secondary capacitor provide switching noise a return path to avoid common-mode noise effects. This capacitor may be realized in a PCB design with overlapping primary and secondary planes and/or with a real capacitor.



Never Forget the Primary to Secondary Capacitor to Give the Transformer Parasitic Capacitive Coupled Energy a Return Path

C5

10 nF

Figure 4. An LT3999 with an ultralow noise postregulator.

PULSE(0 5 1u 10n 10n

Œ

490n 1u)



Figure 6. LT3999 and the switching relation to the sync pin.

Figure 5 shows the current waveforms at the transformer (both the primary side and secondary side current), which gives a better utilization of the transformer and provides better EMI behavior.

Figure 6 shows synchronization to an external clock signal. The end of the acquisition phase aligns to the positive edge of the sync pin. As a result, there will be a long quiet time of ~4 μ s. This enables the converter to sample an input signal during that timeframe and eliminate the transient effects in the isolated power to a minimum. The LTC2378-20 has an acquisition time of 312 ns, which is ideal for the <1 μ s quiet window.

Data Isolation

Data isolation can be done with digital isolators, such as those in the ADuMx family. Those digital isolators are available for many standard interfaces like SPI, I²C, CAN, etc.—for example, the ADuM140 can be used for SPI isolation. To achieve data isolation, the SPI signal SPI clock, SD0, SCK, and Busy just need to be connected to the data isolator. In data isolation, electrical energy is transferred from the primary side to the secondary side through the inductive isolation barrier. A current return path needs to be added, which is done by a capacitor. This capacitor can be built at the PCB with overlapping planes.

Clock Isolation

Clock isolation is another important task. In case you want to have a high performance ADC with 20 bits at a 1 MHz sample rate, such as the LTC2378-20, a signal-to-noise ratio (SNR) of 104 dB SNR is possible. To achieve high performance,

a jitter free clock is required. Why shouldn't you use a standard isolator like the ADuM14x series? The standard isolator will limit the performance of the ADC as it adds jitter to the clock. More details can be found in Design Note DN1013.

Figure 7 displays the theoretical limit of the SNR over frequency for various types of clock jitter. High performance ADCs like the LTC2378 have an aperture clock jitter of 4 ps, which gives a theoretical 106 dB limit at 200 kHz input.



Figure 7. Clock jitter vs. ADC performance.



Figure 8. Clock isolation using a standard isolator.

The standard clock isolator concepts depicted in Figure 8 include:

- A good standard digital isolator like the ADuM250N has a jitter of 70 ps rms. For a 100 dB SNR goal, the signal sample rates are limited to 20 kHz due to the clock jitter.
- An optimized clock isolator like LTM2893 provides a reduced jitter of 30 ps rms. For a 100 dB SNR goal, the signal sample rate is now 50 kHz, which gives you more bandwidth at full SNR performance.



Figure 9. Clock isolation using an LVDS clock isolator.

Figure 9: For higher input frequencies, LVDS isolators should be used. ADN4654 provides a 2.6 ps jitter, which brings you close to the best performance for an ADC. The SNR limit through clock jitter at 100 kHz input would be 110 dB.



Figure 10. Clock isolation using an additional PLL for clock jitter cleaning.

► Figure 10: This shows the use of a PLL for clock cleaning. An ADF4360-9 can help to reduce the clock jitter.

A more detailed block diagram for a clock cleaning with a PLL is shown in Figure 11. You can use the ADF4360-9 as a clock cleaner and add a divider by 2 to the output. The AD7760 is characterized to 1.1 MHz.



Figure 11. An ADF4360-9 used as a clock cleaner.

So a 1 MSPS SAR ADC like the LTC2378 will not directly be supported. A low jitter flip-flop helps in this case. It divides the clock by 2.



Figure 12. A flip-flop used to get the clock down for the LTC2378.



Figure 13. Clock generation at the isolated (hot) side.

Figure 13: Local clock generation is another option to get a clock with the required jitter performance. Local clock generation makes the clocking architecture more complicated as it introduces asynchronous clock domains to the system. For example, if you want to use two separate isolated ADCs, the clocks will differ in absolute frequency and a sample rate conversion must be added to match the clocks again. Some details on sample rate conversion can be found in the Engineer-to-Engineer Note, EE-268.

Clocking for High Performance Sigma-Delta ADCs

Similar problems with the clocks apply also for high performance sigma-delta ADCs like the AD7760. Here the important clock signal is the jitter free oversampling clock at, for example, 40 MHz. In this case, no additional dividers are required.

Conclusion

Isolated high performance ADCs require a careful isolated design and a selection of various isolation techniques to achieve a high performance SNR above 100 dB. Specific care should be taken on the isolated clock, as the influence of the clock jitter could destroy the performance. Secondly, care should be given to isolated power. Simple isolation topologies like a flyback introduce high EMI transients.

For better performance, a push-pull converter should be used. Data isolation is another, albeit less important, concern as standard available devices offer good performance and have less impact to the overall system performance. Addressing these three isolation topics enables the designer to come up with a high performance isolated system solution.



About the Author

Wilfried Platzer studied information technology with an emphasis on RF in Karlsruhe, Germany. He started at ITT in 1997 and later worked at TDK-Micronas. Wilfried has held several positions starting as a field applications engineer and then focusing on IC concept and IC system architecture engineering for mixed-signal ICs. After 11 years, he moved to an electronic predevelopment position at Auma and in 2015, he joined Linear Technology (now part of Analog Devices). Currently, Wilfried is a senior field applications engineer at Analog Devices, providing regional support for Switzerland. He can be reached at wilfried.platzer@analog.com.



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