Rarely Asked Questions—Issue 153 High Speed ADC Power Supply Domains

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Question:

Why are there all these power domains for high speed ADCs?

Answer:

Today's radio frequency analog-to-digital converters (RF ADCs) have come a long way in terms of sample rates, as well as serviceable bandwidths. They also pack in a lot more digital processing and have increased in complexities when it comes to power supplies. With that said, why are there so many different power rails and domains in today's RF ADCs?

To understand the proliferation of power domains and supplies, we need to take a trip along ADC history lane. Back in the days when the ADC was just that, an ADC, the sample speeds were slower—in the 10s of MHz—and the amount of digital content was small to nonexistent. The digital portion of the circuit primarily dealt with figuring out how to transmit the bits out to the digital receive logic—either an application-specific integrated circuit (ASIC) or field programmable gate array (FPGA). The process node used to fabricate these circuits was a higher geometry, around 180 nm or more. You could extract adequate performance from a single voltage rail (1.8 V) and just two different domains (AVDD and DVDD for analog and digital domains, respectively).

As silicon processing technologies improved, transistor geometries reduced, meaning one could pack more transistors (in other words, features) per mm^2. However, the ADCs were still expected to achieve the same (or better) performance as their earlier generation counterparts. Now, the design of the ADC had taken a multifaceted approach where:

- The sample speeds and analog bandwidths had to be improved
- The performance had to be the same as or better than previous generation
- There is more on-chip digital processing to aid the digital receive logic

Let us further discuss each of these features and how they pose challenges to the silicon design.

The Need for Speed

In CMOS technology the most popular way to go faster (bandwidths) is to go smaller (transistor geometries). Using finer geometry CMOS transistors results in reduced parasitics, which aid in the transistor's speed. Faster transistors mean wider bandwidths. The power in digital circuits has a direct relationship to the switching speed, but a square relationship to the supply voltage. This is shown by the equation below:

$$P = C_{LD} \times V^2 \times f_{SW}$$

where:

P is power dissipated

C_{LD} is load capacitance

V is supply voltage

f_{SW} is switching frequency

Going to finer geometries allows circuit designers to implement faster circuits while maintaining the same power per transistor per MHz as the previous generation. As an example, take AD9680 and AD9695, which were designed using the 65 nm and 28 nm CMOS technology, respectively. At 1.25 GSPS and 1.3 GSPS, the AD9680 and AD9695 burn 3.7 W and 1.6 W, respectively. This shows that for the same architecture, give or take, the same circuit can burn about half the power on a 28 nm process as it did on a 65 nm process. The corollary to that is you can run the same circuit at twice the speed on 28 nm process, as you did at 65 nm while burning the same amount of power. The AD9208 illustrates this to a good extent.

Headroom Is Everything

While the need for sampling wider bandwidths has necessitated the move to finer geometries, the expectations on data converter performance—like noise and linearity—still stand. This poses a unique challenge to analog design. An unintended side effect of going to smaller geometries is the reduction in supply voltages. This greatly lowers the headroom required to develop the analog circuits needed to operate at the high sample rates and maintain the same noise/linearity performance. To circumvent this limitation, the circuit is designed with different voltage rails to provide the required noise and linearity performance. In the AD9208, for example, the 0.975 V supply provides the power to the circuits needing the fast switching. This includes the comparators and other associated circuitry, as well as the digital and the driver outputs. The 1.9 V supply provides power to the reference and other bias circuits. The 2.5 V supply provides power to the input buffer, which requires the high headroom to function at the high analog frequencies. It is not necessary to have the 2.5 V supply for the buffer; it can operate at 1.9 V as well. This lowering of the voltage rail will result in degraded linearity performance. With digital circuits, there is no need for headroom as the most important parameter is speed. So, digital circuits usually run at the lowest supply voltage to take advantage of the CMOS switching speed and the power dissipation. This is evident in the newer generation ADCs where the lowest voltage rail is as low as 0.975 V. Table 1 below shows some common ADCs across generations.

Table 1: Product Comparisons

Product	Sample Rate (MSPS)	Process Node (nm)	Voltage Rails (V)	Domains
AD9467	250	180	1.8, 3.3	AVDD1, AVDD2, AVDD3, DRVDD
AD9625	2500	65	1.3, 2.5	AVDD1, AVDD2, DRVDD1, DRVDD2, DVDD1, DVDD2, DVDDIO, SPI_VDDIO
AD9208	3000	28	0.975, 1.9, 2.5	AVDD1, AVDD2, AVDD3, AVDD1_SR, DVDD, DRVDD1, DRVDD2, SPIVDD

Isolation Is Key

With the move to deep submicron technology and high speed switching circuits, the level of integration of features has gone up as well. As an example, take the AD9467 and the AD9208. The AD9467 utilizes the 180 nm BiCMOS process, whereas the AD9208 utilizes the 28 nm CMOS process. Granted, the AD9467 has a noise density of about –157 dBFS/Hz, while the AD9208 has a noise density of about –152 dBFS/Hz. However, if one were to do a simple data sheet exercise, take the total power (per channel), and divide it by the resolution and sample rate, then you can see that the AD9467 consumes about 330 µW/bit/MSPS, whereas the AD9208 only consumes 40 µW/bit/MSPS. Compared to the AD9467, the AD9208 has much higher sample rate (3 GSPS vs. 250 MSPS), much higher input bandwidth (9 GHz vs. 0.9 GHz), and way more digital features packed into it. The AD9208 does all this and consumes about 1/8th the power per bit, per MSPS. The power per bit, per MSPS is not an industry standard metric and is being used in this case to point out the benefits of utilizing a smaller geometry process in ADC design. When you have ultrafast circuits running in very close proximity, there is always the risk of coupling or chatter between the various blocks. To improve the isolation, the designer must consider the various coupling mechanisms. The most obvious mechanism would be through a shared power supply domain. If the domains are separated as far away from the circuits as possible, the likelihood of the digital circuits chattering with their analog counterparts sharing the same voltage rail (0.975 V in the AD9208's case) can be minimized. In silicon, the supplies are already separated, as are the grounds. The package is designed to continue this isolated supply domain treatment all the way through. This results in a package that shows a proliferation of supply domains and rails, as shown in the Table 2, with the AD9208 as an example.

Table 2: AD9208 Power and Ground Domains

Voltage Domain	Voltage Rail (V)	Description
AVDD1	0.975	Analog power supply
AVDD1_SR	0.975	Analog power supply for SYSREF
AVDD2	1.9	Analog power supply
AVDD3	2.5	Analog power supply
DVDD	0.975	Digital power supply
DRVDD1	0.975	Digital driver power supply
DRVDD2	1.9	Digital driver power supply
SPIVDD	1.9	Digital power supply for SPI
AGND	—	Analog ground return for AVDD1, AVDD1_SR, AVDD2, and AVDD3
AGND[1]	—	Ground reference for the clock domain
AGND[2]	—	Ground reference for SYSREF±
AGND[3]	—	Isolation ground; barrier between analog and digital domains on chip
DGND	—	Digital ground return for DVDD and SPIVDD
DRGND	—	Digital driver ground return for DRVDD1 and DRVDD2

A pinout diagram showing the various domains of the AD9208 is shown in Figure 1.

This could be a source of considerable consternation to a systems designer. At first glance, the data sheet gives the impression that these domains need to be treated separately to optimize performance in the system.

AD9208

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AVDD2	AVDD2	AVDD1	AVDD1[1]	AVDD1[1]	AGND[1]	CLK+	CLK–	AGND[1]	AVDD1[1]	AVDD1[1]	AVDD1	AVDD2	AVDD2
B	AVDD2	AVDD2	AVDD1	AVDD1[1]	AGND	AGND[1]	AGND[1]	AGND[1]	AGND[1]	AGND	AVDD1[1]	AVDD1	AVDD2	AVDD2
C	AVDD2	AVDD2	AVDD1	AGND	AGND	AGND[1]	AGND[1]	AGND[1]	AGND[1]	AGND	AGND	AVDD1	AVDD2	AVDD2
D	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND[1]	AGND[1]	AGND	AGND	AGND	AGND	AGND	AVDD3
E	VIN–B	AGND	AGND	AGND	AGND	AGND[2]	AVDD1_SR	AGND[2]	AGND	AGND	AGND	AGND	AGND	VIN–A
F	VIN+B	AGND	AGND	AGND	AGND	AGND	SYSREF+	SYSREF–	AGND	AGND	AGND	AGND	AGND	VIN+A
G	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD3
H	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	VREF	AGND	AGND	AGND	AGND
J	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
K	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]	AGND[2]
L	DGND	GPIO_B1	SPIVDD	FD_B/ GPIO_B0	CSB	SCLK	SDIO	PDWN/ STBY	FD_A/ GPIO_A0	SPIVDD	GPIO_A1	DGND	DGND	DGND
M	DGND	DGND	DRGND	DRGND	DRVDD1	DRVDD1	DRVDD1	DRVDD1	DRGND	DRGND	DRVDD1	DRGND	DRVDD2	DVDD
N	DVDD	DVDD	DRGND	SERDOUT7+	SERDOUT6+	SERDOUT5+	SERDOUT4+	SERDOUT3+	SERDOUT2+	SERDOUT1+	SERDOUT0+	DRGND	SYNCINB+	DVDD
P	DVDD	DVDD	DRGND	SERDOUT7–	SERDOUT6–	SERDOUT5–	SERDOUT4–	SERDOUT3–	SERDOUT2–	SERDOUT1–	SERDOUT0–	DRGND	SYNCINB–	DVDD

[1]Denotes Clock Domain.
[2]Denotes SYSREF± Domain.
[3]Denotes Isolation Domain.

Figure 1. AD9208 pin configuration (top view).

Is There No End in Sight?

The situation is not as dire as it seems. The aim of the data sheet was to merely call attention to the various sensitive domains so the system designer can pay attention to the PDN (power delivery network) design and partition them appropriately. Most of the supply and ground domains that share the same rail can be combined and, thus, the PDN can be simplified. This results in a simplified BOM (bill of material) and layout. Depending on the design constraints, two such approaches to designing the PDN for the AD9208 are shown in Figure 2 and Figure 3.

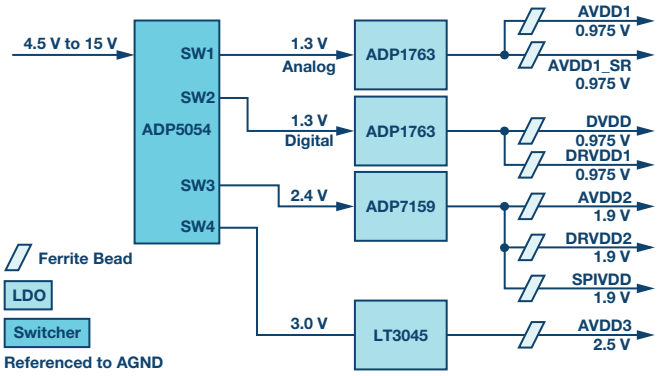

Figure 2. AD9208 pin configuration (top view).

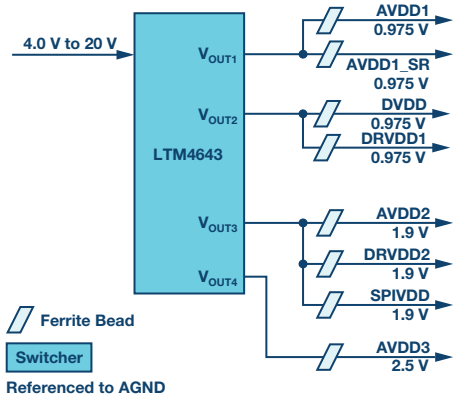

Figure 3. AD9208 PDN showing dc-to-dc converter powering all domains.

With adequate filtering and layout separation, the various domains can be laid out in such a way that the performance of the ADC is maximized while the BOM and PDN complexity are lowered. A Kelvin connection approach to the various ground domains also will result in improved isolation. From a netlist standpoint, there will still only be one GND net. The board can be partitioned to various ground domains to provide the adequate isolation. In the AD9208-3000EBZ, which is the evaluation board for the AD9208, the various grounds are partitioned to make a Kelvin connection on Layer 9. The cross section of the AD9208-3000EBZ, which is a 10-layer PCB (printed circuit board) showing the various GND connections, is shown in Figure 4.

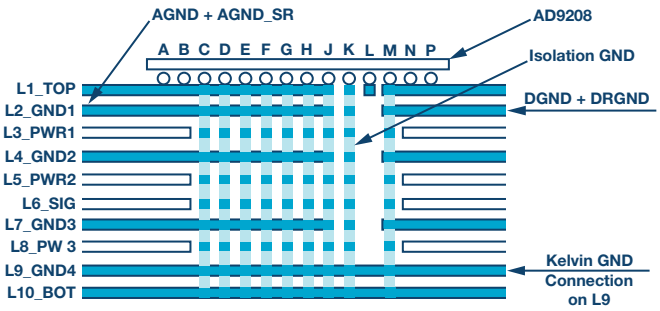

Figure 4. AD9208—3000 EBZ PCB cross section under the AD9208.

So, It's Not the End of the World, Is It?

Absolutely not. Just because the data sheet for the AD9208 shows all these domains does not mean that they must all be separated on the system board. Knowing the system performance goals and ADC target performance will go a long way in optimizing the PDN for the ADC. Using smart partitioning on the board with an eye to reducing unnecessary ground loops is key in keeping the cross-talk between various domains to a minimum. Sharing supply domains where applicable but keeping in mind the isolation requirements will result in a simplified PDN and BOM.

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