Rarely Asked Questions—140 Presto! Multiply Your ADC's Virtual Channel Count with DDC Magic

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Question:

I bought a dual-channel ADC and configured the digital downconverters. Now I am being told I have four converters! Is there a 2-for-1 data converter sale I wasn't aware of?

Answer:

Ever since the advent of the very first monolithic, silicon-based analog-todigital converters (ADCs), the ADC has been keeping pace with the rapid advancements in silicon processing technology. Over the years, the silicon processing technology has advanced enough that it is now possible to economically design ADCs with a lot more powerful digital processing. Earlier generation ADC designs used very little digital circuitry outside of error correction and digital drivers. The new family of GSPS (gigasample per second) converters (also known as RF sampling ADCs) are enabled using sophisticated 65 nm CMOS technology and can pack a lot more digital processing power to enhance the ADC's performance.

With high sample rates (in the GSPS realm) also come a huge payload of data (bits per second). Take the AD9680, which is a dual 14-bit, 1.25 GSPS/1 GSPS/820 MSPS/500 MSPS, JESD204B analog-to-digital converter as an example. At the maximum sample rate of 1.25 GSPS, the ADC streams

14 bits \times 2 converter channels \times 1.25 Gbps = 35 Gbps

This amount of data will require an enormous number of LVDS routing lanes to extract the digital data. In order to facilitate the implementation of

this large throughput, the JESD204B standard was adopted. The JESD204B is a high speed, data transmission protocol that employs 8b/10b encoding and scrambling among other features aimed at providing adequate signal integrity. With the JESD204B standard, the total throughput now becomes

16 *bits* × 2 *converter channels* ×
$$\left(\frac{10}{8}\right)$$
 × 1.25 Gbps = 50 Gbps

Using the JESD204B standard, the data throughput can be split across four high speed serial lanes at 12.5 Gpbs on each lane. Compare this to an LVDS interface where, at a line rate cap of about 1 Gbps/lane, the chip would need more than 28 pairs!

A quick inspection of the AD9680 data sheet reveals that there is quite the alphabet soup as far as setting up the link goes. Whereas earlier generation LVDS ADCs were easier to implement, the newer generation JESD204B ADCs are a bit more complicated. They become even more complicated when you take into account the internal digital downconverter (DDC) setups. However, the ADC setup is primarily determined by three letters in that alphabet soup:

- L = number of lanes per JESD204B link
- M = number of converters per JESD204B link
- F = number of octets per frame of data in the JESD204B link

Take for example the AD9250, which is a dual 14-bit, 250 MSPS JESD204B analog-to-digital converter. Figure 1 shows the block diagram representation of the AD9250 in its default setup.







In this setup the JESD204B link (JESD204B transmitter) is pretty straightforward, as there are no additional digital processing done in the AD9250. To the JESD204B link, Channel A becomes Converter 0 (M_0), whereas Channel B becomes Converter 1 (M_1), which means the value of M becomes 2. The total line rate for this setup is

$$Line Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times F_{OUT}}{L} = \frac{2 \times 16 \times 1.25 \times 250 M}{2} = 5 \text{ Gbps/lane}$$

Compare this to the AD9680 sampling at 1 GSPS—but in this case, two digital downconverters are used in a complex (I/Q) setup. Figure 2 shows the AD9680 where the digital downconverters are used to decimate the data sampled at 1 GSPS by four. This results in an output sample rate (F_{OUT}) of 250 MSPS.



Figure 2. Setting up the AD9860-1000 with two DDCs set to decimate by 4.

It is clear from Figure 2 that the AD9680 can effectively reduce the sample rate using the internal on-chip digital downconverters. Since each of the DDCs outputs a 16-bit stream, the actual (physical) converter bit streams are now decoupled from the "M" parameter of the JESD204B alphabet soup. Per the standard, M is the number of converters per link.

In the modified scenario, M now becomes a parameter called a virtual converter. Even though the AD9680 physically only has two ADC channels (A and B), with the DDCs in complex output mode enabled, there are now four different (16-bit) data streams to the JESD204B interface. To the JESD204B interface, this looks like there are now four (virtual) converters sending bit streams. Hence, the M = 4 or converter multiplying act. The output line rate in this case becomes

$$Line Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times F_{OUT}}{L} = \frac{4 \times 16 \times 1.25 \times 250 M}{2} = 10 \text{ Gbps/lane}$$

The flexibility of the AD9680's JESD204B interface becomes apparent here, as there are now two options available depending on what the line rate acceptability of the receive logic (ASIC or FPGA). Table 1 shows the available options for the JESD204B interface in the AD9680 setup shown in Figure 2.

Table 1. Configuration Options for the AD9680 ADC's JESD204B Output Interface

# Virtual Converters M	# Lanes Per Link L	# Octets Per Frame F	Line Rate (Gbps/Lane)	
٨	4	2	5	
4	2	4	10	

For a dual-channel ADC like the AD9680 that has four DDCs, Table 2 shows the virtual converter mapping that is available for various configurations.

Table 2. Configuration Options for the AD9680 ADC's JESD204B Output Interface

Number of Virtual Converters Supported	Chip Operating Mode	Chip Q Ignore	Virtual Converter Mapping							
			0	1	2	3	4	5	6	7
1 to 2	Full Bandwidth Mode	Real or Complex	ADC A Samples	ADC B Samples	Unused	Unused	Unused	Unused	Unused	Unused
1	One DDC Mode	Real (I Only)	DDC 0 I Samples	Unused						
2	One DDC Mode	Complex (I/Q)	DDC 0 I Samples	DDC 0 Q Samples	Unused	Unused	Unused	Unused	Unused	Unused
2	Two DDC Mode	Real (I Only)	DDC 0 I Samples	DDC 1 I Samples	Unused	Unused	Unused	Unused	Unused	Unused
4	Two DDC Mode	Complex (I/Q)	DDC 0 I Samples	DDC 0 Q Samples	DDC 1 I Samples	DDC 1 Q Samples	Unused	Unused	Unused	Unused
4	Four DDC Mode	Real (I Only)	DDC 0 I Samples	DDC 1 I Samples	DDC 2 I Samples	DDC 3 I Samples	Unused	Unused	Unused	Unused
8	Four DDC Mode	Complex (I/Q)	DDC 0 I Samples	DDC 0 Q Samples	DDC 1 I Samples	DDC 1 Q Samples	DDC 2 I Samples	DDC 2 Q Samples	DDC 3 I Samples	DDC 3 Q Samples

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