

Rarely Asked Questions—Issue 118

Mystery Spur Explained: Don't Blame the DDC!

By David Buchanan

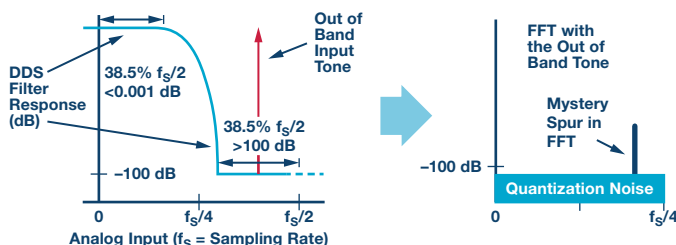


Question:

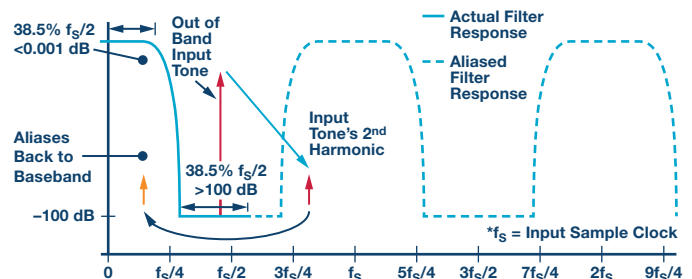
I recently witnessed some “strange” behavior while evaluating the output spectrum on one of your high speed ADCs that incorporates a digital downconverter (DDC) function. Can you explain the existence of a mystery spur?

Answer:

The DDCs include a decimation filter, which allows you to avoid traditional input antialiasing filtering requirements, yet digitally filter out the baseband signal of interest with a net lower payload of data to process. You revealed that you were testing a frequency plan and wanted to see that an input frequency that was outside the pass and transition band of the DDC was indeed attenuated by >100 dB (see diagram below). You ran an FFT of the ADC output data with the decimation filter enabled, and saw a spur in the resulting output spectrum that was only 90 dB down, not the >100 dB down that you expected to see. If you removed the input signal, the spur went away. Where's it coming from, you ask? How could a signal that is well into the stop band be causing a spur in the pass band?



Well, when you start thinking about the ADC's on-board DSP options, it can sometimes be easy to stop thinking about how an analog-to-digital converter behaves. So while the figure above is accurate in describing the decimation filter's response in the baseband Nyquist zone, it doesn't cover what happens in the other Nyquist zones in the converter. In this case, the filter's response will alias into all the higher order Nyquist zones. In the diagram below you can see the response over the first five Nyquist zones. Also noted is the mystery spur, which is the aliased second harmonic of the out of band input tone.



You indicated that in your test setup, there was no analog input antialiasing filter present. So there is the answer to the root cause of the mystery spur—the digital filter can't eliminate spectral content on the analog side. This is an interesting illustration of how higher sample rate converters can ease the analog input filtering requirements, but you still can't ignore the laws of aliasing in sampled systems. The high sample rate and the DDC allowed the blocker between $f_s/4$ and $f_s/2$ to be dealt with without an aggressive analog filter on the front end, and a much less aggressive filter will eliminate the spurious from $3f_s/4$ and beyond.

References

Technical article:

Beavers, Ian. “Understanding Spurious-Free Dynamic Range in Wideband GSPS ADCs.” Analog Devices, 2014.

Blog series on ADI's EngineerZone® community:

- Examining DDCs in Wideband GSPS ADCs—Part 1
- Examining DDCs in Wideband GSPS ADCs—Part 2
- Examining DDCs in Wideband GSPS ADCs—Part 3
- Examining DDCs in Wideband GSPS ADCs—Part 4
- Examining DDCs in Wideband GSPS ADCs—Part 5
- Examining DDCs in Wideband GSPS ADCs—Part 6
- Examining DDCs in Wideband GSPS ADCs—Part 7



David Buchanan [david.buchanan@analog.com] received a B.S.E.E. from the University of Virginia in 1987. Employed in marketing and applications engineering roles by Analog Devices, Adaptec, and STMicroelectronics, he has experience with a variety of high performance analog semiconductor products. He is currently a senior applications engineer with ADI's High Speed Converters product line in Greensboro, North Carolina.



David Buchanan

Also by this Author:

[Rarely Asked Questions—Issue 115, March 2015](#)

[Isn't That Gain Specification a Bit Lopsided?](#)