Product/Process Change Notice - PCN 22_0042 Rev. -

Analog Devices, Inc. One Analog Way, Wilmington, MA 01887

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: ADuCM410/420 Silicon Revision

Publication Date: 25-Mar-2022

Effectivity Date: 27-Jun-2022 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release

Description Of Change:

Silicon update on WLCSP packaged ADuCM410 and ADuCM420 devices.

Reason For Change:

Background: The default System clock for the ADuCM410/ADuCM420 is from an internal PLL. The PLL input is the internal 16MHz oscillator, its output by default is 160MHz and can be selected as the System clock for the memories, Cortex-M33 and other peripherals.
An interrupt is provided to detect PLL lock and unlock states. If a PLL unlock interrupt is asserted, the PLL output should not be selected as the system clock.
Issue: On previous silicon, When P3.6 was toggled as a GPIO pin or, when used as the MDIO data I/O function, the PLL lock detection circuit asserted many PLL unlock interrupts to the Cortex-M33 core when the PLL interrupt was enabled.
On the WLCSP parts, the P3.6 pin is directly underneath the 16MHz oscillator. If P3.6 toggled at frequencies >1kHz, the oscillator output frequency can vary beyond the frequency range allowed by the PLL lock detection circuit.
Fix: An additional metal layer was added at the chip to act as an insulator between the external balls of the WLCSP package the inner layers containing oscillator circuits.
This additional layer is connected to DGND of the chip.

Impact of the change (positive or negative) on fit, form, function & reliability:

No impact to fit, form or reliability.

Product Identification *(this section will describe how to identify the changed material)*

Revision branding changes from B90 to C91
(Die revision brand is changing B to C).
(Kernel revision brand is changing from 0 to 1).

Internal CHIPID register (ADDRESS: 0x40002024) changes from 0x571 to 0x572.
Internal Kernel Revision (ADDRESS: 0x101FE8) changes from 0x258d to 0x331e

Summary of Supporting Information:

ESD, Latch Up and SHR Qualification results available upon request.

Supporting Documents None

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.

Americas:	**Europe:**	**Japan:**	**Rest of Asia:**
PCN_Americas@analog.com	PCN_Europe@analog.com	PCN_Japan@analog.com	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (3)				
ADUCM410 / ADUCM410BCBZ-RL7	ADUCM420 / ADUCM420BCBZ-RL	ADUCM420 / ADUCM420BCBZ-RL7		

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	25-Mar-2022	27-Jun-2022	Initial Release