

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{PWR} = V_{IN\_SNS} = 12\text{V}$ ,  $V_{DD33}$ ,  $V_{DD25}$  and REF pins floating, unless otherwise indicated. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{UPDATE\_ADC}$	Update Time	Odd Numbered Channels in Current Sense Mode (Note 7)		160		ms
$C_{IN\_ADC}$	Input Sampling Capacitance			1		pF
$f_{IN\_ADC}$	Input Sampling Frequency			62.5		kHz
$I_{IN\_ADC}$	Input Leakage Current	$V_{IN\_ADC} = 0\text{V}$ , $0\text{V} \leq V_{COMMONMODE} \leq 6\text{V}$ , Current Sense Mode	●		$\pm 0.5$	$\mu\text{A}$
	Differential Input Current	$V_{IN\_ADC} = 0.17\text{V}$ , Current Sense Mode	●	80	250	nA
		$V_{IN\_ADC} = 6\text{V}$ , Voltage Sense Mode	●	10	15	$\mu\text{A}$

### DAC Output Characteristics

$N\_VDACP$	Resolution			10		Bits	
$V_{FS\_VDACP}$	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF	●	1.32	1.38	1.44	V
		DAC Polarity = 1	●	2.53	2.65	2.77	V
$INL\_VDACP$	Integral Nonlinearity	(Note 8)	●		$\pm 2$	LSB	
$DNL\_VDACP$	Differential Nonlinearity	(Note 8)	●		$\pm 2.4$	LSB	
$V_{OS\_VDACP}$	Offset Voltage	(Note 8)	●		$\pm 10$	mV	
$V_{DACP}$	Load Regulation ( $V_{DACPn} - V_{DACMn}$ )	$V_{DACPn} = 2.65\text{V}$ , $I_{VDACPn}$ Sourcing = 2mA		100		ppm/mA	
		$V_{DACPn} = 0.1\text{V}$ , $I_{VDACPn}$ Sinking = 2mA		100		ppm/mA	
	PSRR ( $V_{DACPn} - V_{DACMn}$ )	DC: $3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$ , $V_{PWR} = V_{DD33}$		60		dB	
		100mV Step in 20ns with 50pF Load		40		dB	
	DC CMRR ( $V_{DACPn} - V_{DACMn}$ )	$-0.1\text{V} \leq V_{DACMn} \leq 0.1\text{V}$		60		dB	
	Leakage Current	$V_{DACPn}$ Hi-Z, $0\text{V} \leq V_{DACPn} \leq 6\text{V}$	●		$\pm 100$	nA	
	Short-Circuit Current Low	$V_{DACPn}$ Shorted to GND	●	-10		-4	mA
Short-Circuit Current High	$V_{DACPn}$ Shorted to $V_{DD33}$	●	4		10	mA	
$C_{OUT}$	Output Capacitance	$V_{DACPn}$ Hi-Z		10		pF	
$t_{S\_VDACP}$	DAC Output Update Rate	Fast Servo Mode		500		$\mu\text{s}$	

### DAC Soft-Connect Comparator Characteristics

$V_{OS\_CMP}$	Offset Voltage	$V_{DACPn} = 0.2\text{V}$	●	$\pm 1$	$\pm 18$	mV
		$V_{DACPn} = 1.3\text{V}$	●	$\pm 2$	$\pm 26$	mV
		$V_{DACPn} = 2.65\text{V}$	●	$\pm 3$	$\pm 52$	mV

### Voltage Supervisor Characteristics

$V_{IN\_VS}$	Input Voltage Range (Programmable)	$V_{IN\_VS} = (V_{SENSEPn} - V_{SENSEMn})$	Low Resolution Mode	●	0	6	V
			High Resolution Mode	●	0	3.8	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	-0.1	0.1	V	
$N\_VS$	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode		4		mV/LSB	
		0V to 6V Range: Low Resolution Mode		8		mV/LSB	
$TUE\_VS$	Total Unadjusted Error	$2\text{V} \leq V_{IN\_VS} \leq 6\text{V}$ , Low Resolution Mode	●		$\pm 1.25$	% of Reading	
		$1.5\text{V} < V_{IN\_VS} \leq 3.8\text{V}$ , High Resolution Mode	●		$\pm 1.0$	% of Reading	
		$0.8\text{V} \leq V_{IN\_VS} \leq 1.5\text{V}$ , High Resolution Mode	●		$\pm 1.5$	% of Reading	
$t_{S\_VS}$	Update Period			12.21		$\mu\text{s}$	