OP4177 Die Revision & Wafer Fabrication Process Change

Qualification Results Summary of OP4177 Die Revision & Wafer Fabrication Process Change

QUALIFICATION PLAN / STATUS			
TEST	**SPECIFICATION**	**SAMPLE SIZE**	**RESULTS**
Early Life Failure Rate (ELFR)	*MIL-STD-883, M1015*	3 x 800	Pass
High Temperature Operating Life (HTOL)	JEDEC *JESD22-A108*	3 x 77	Pass
High Temperature Storage Life (HTSL)	JEDEC *JESD22-A103*	1 x 77	Pass
Solder Heat Resistance (SHR)*	JEDEC *J-STD-020*	3 x 11	Pass
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	3 x 77	Pass
Temperature, Humidity, Bias (THB)*	JEDEC *JESD22-A101*	3 x 77	Pass
Latch-Up	JEDEC *JESD78*	3/test	Pass ±200 mA, ±22.5 V
Electrostatic Discharge *Human Body Model*	JEDEC *JS-002*	3/voltage	Pass ±1000 V
Electrostatic Discharge *Field-Induced Charged Device Model*	JEDEC *JESD22-A114*	3/voltage	Pass ±1250 V

*Preconditioned per JEDEC J-STD-020 Level 1