

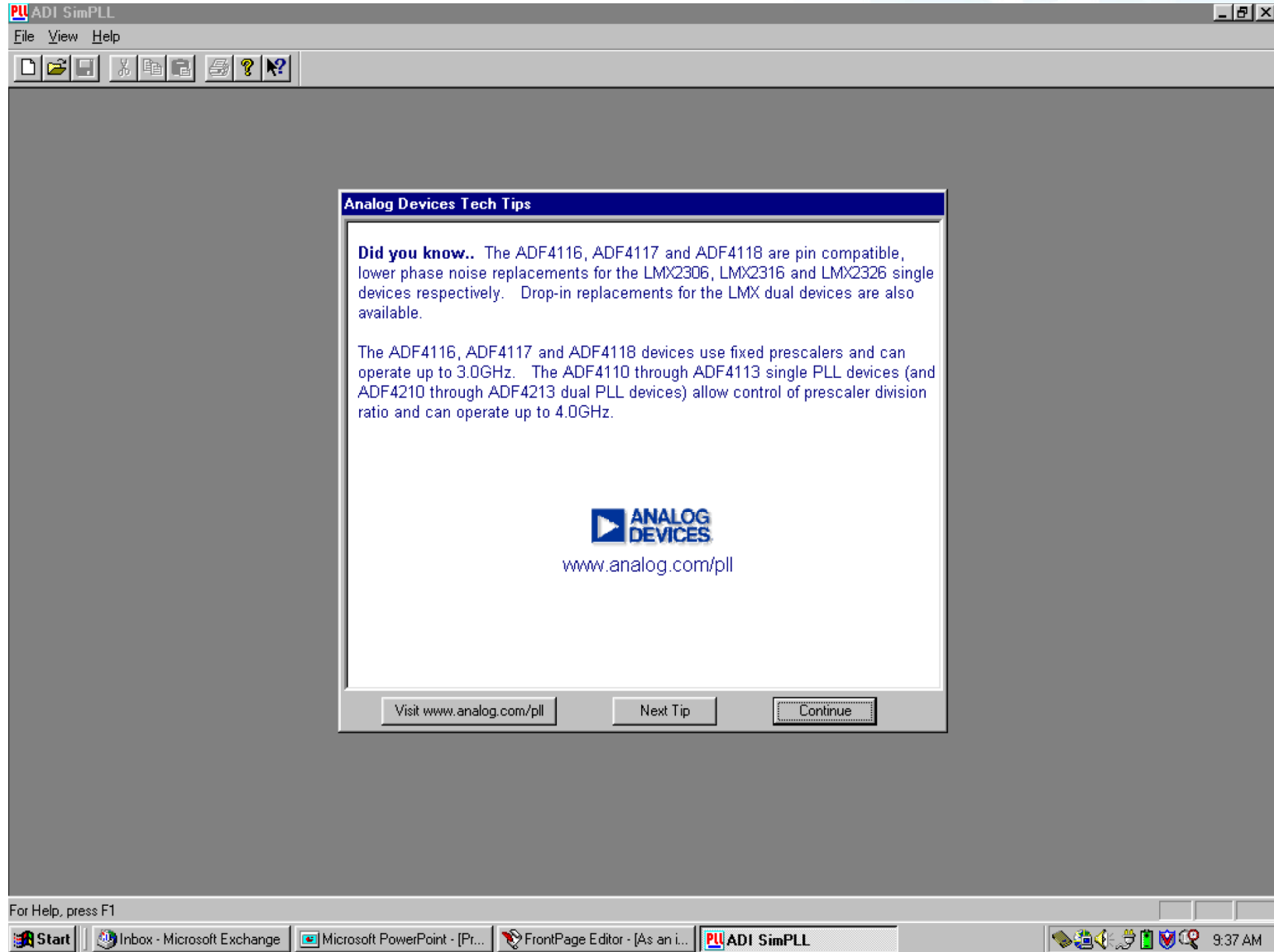
ADIsimPLL™

PLL电路设计和虚拟评估软件



PLL电路设计和虚拟评估软件

欢迎来到ADIsimPLL的虚拟设计和评估环境。以下演示文稿会自动引导您了解这款设计和评估软件工具的出色功能、无限的灵活性和用户友好的界面。本软件是由工程师针对工程师而开发的，其唯一目的是优化设计，使其更快速、更轻松地实现各项目标。从入门级工程师到经验丰富的资深人士，都能在ADIsimPLL中找到大量板载工具和选项，保证最大限度地提高电路设计效率。



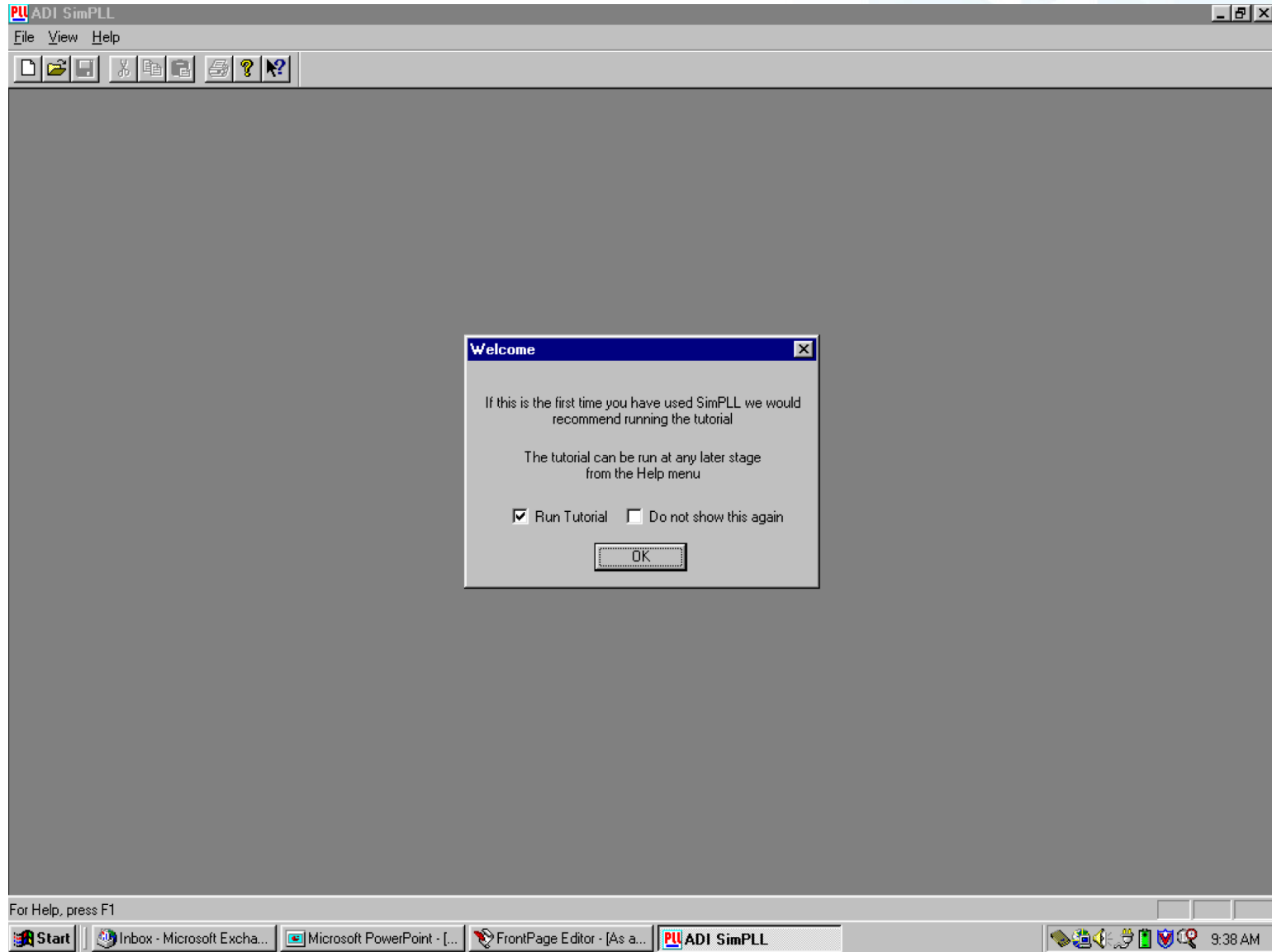
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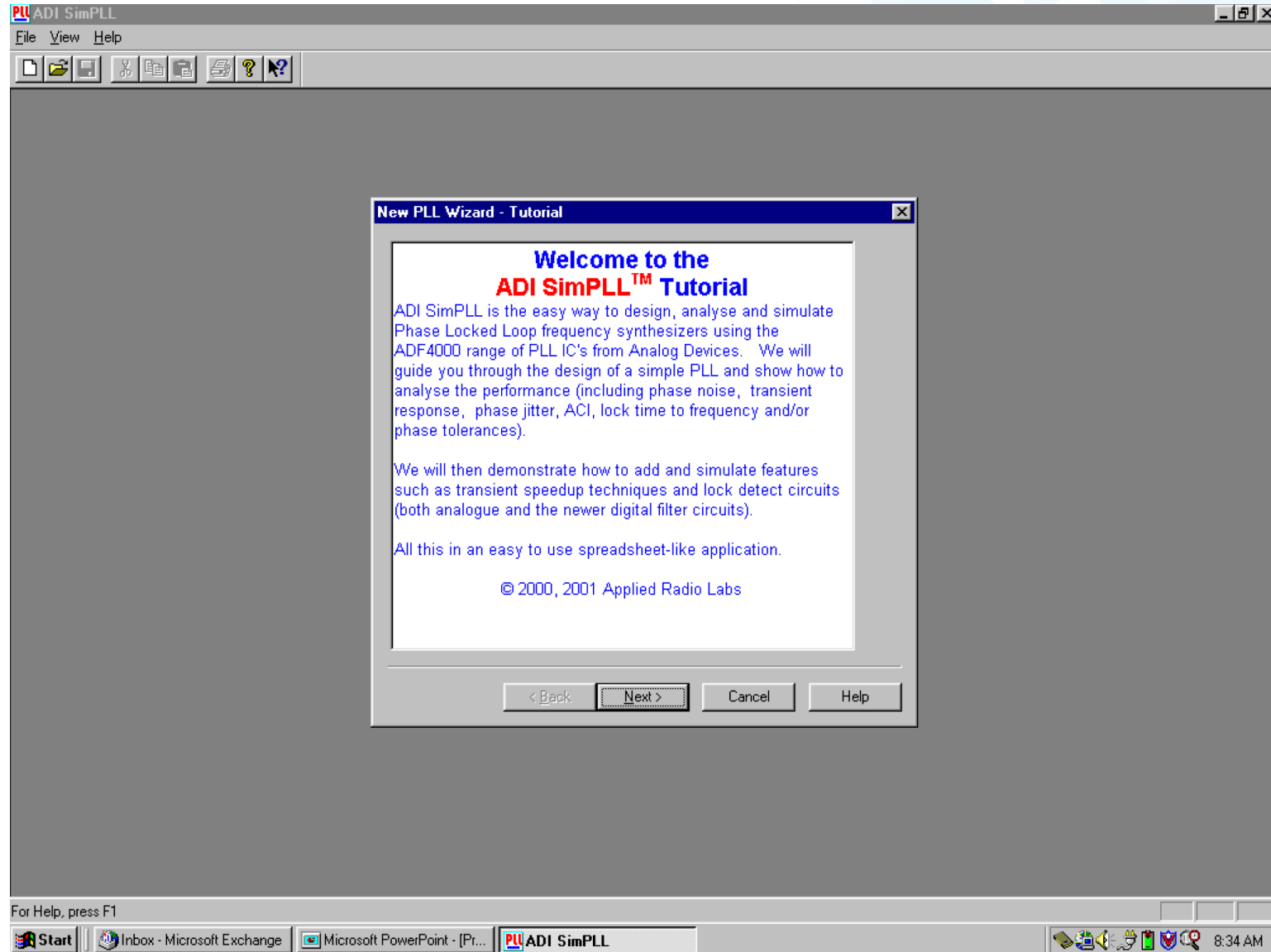


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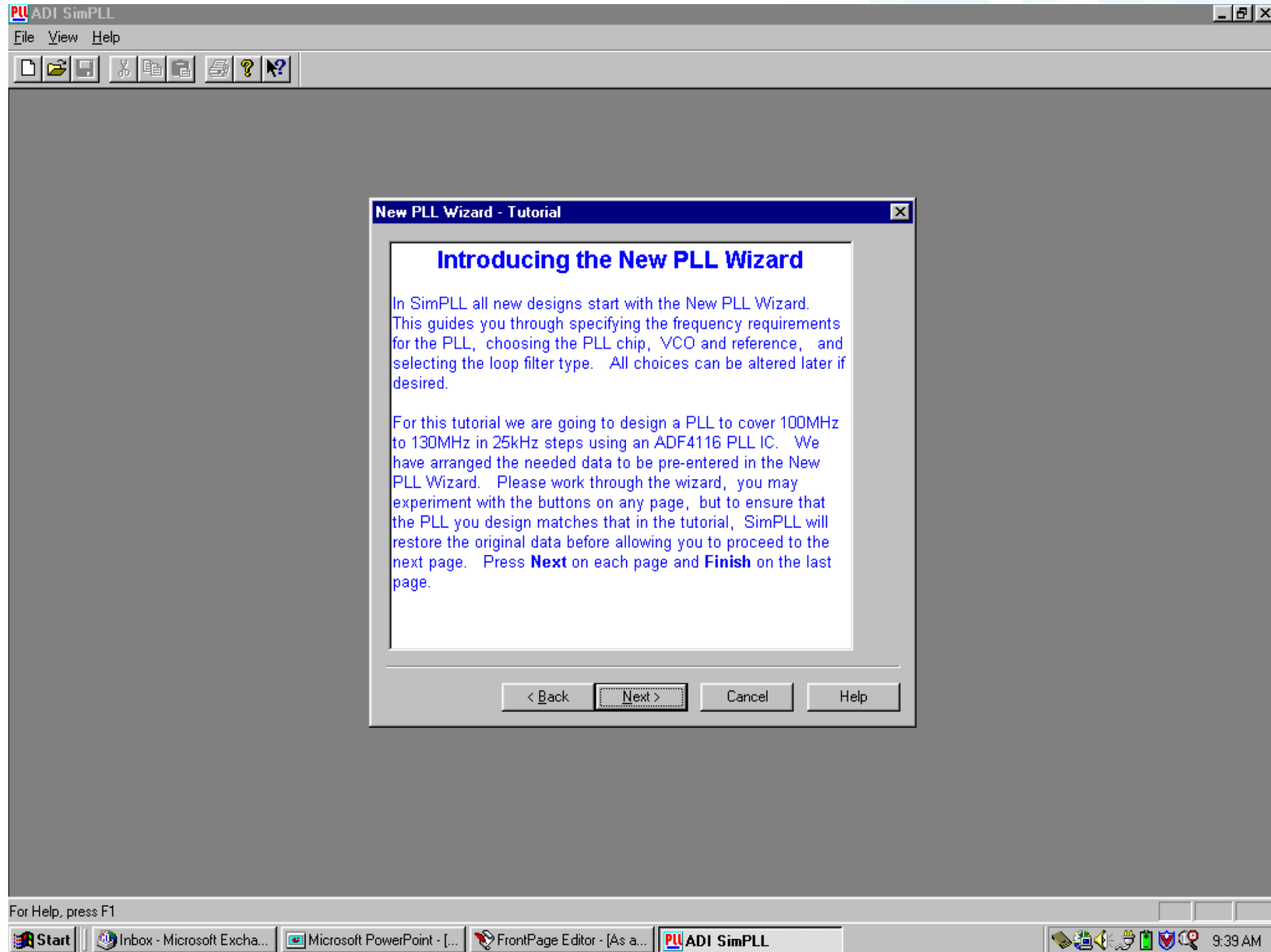
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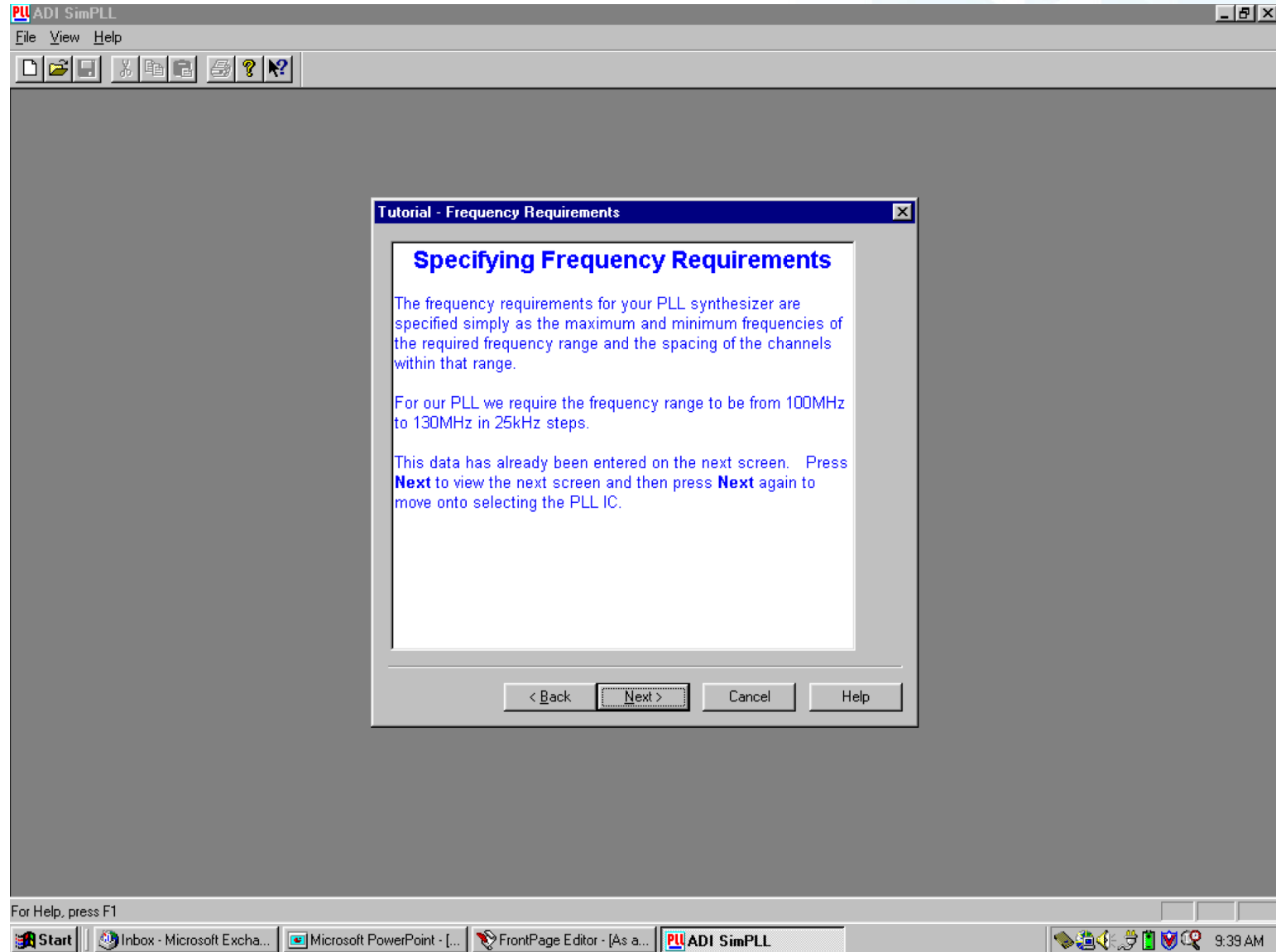
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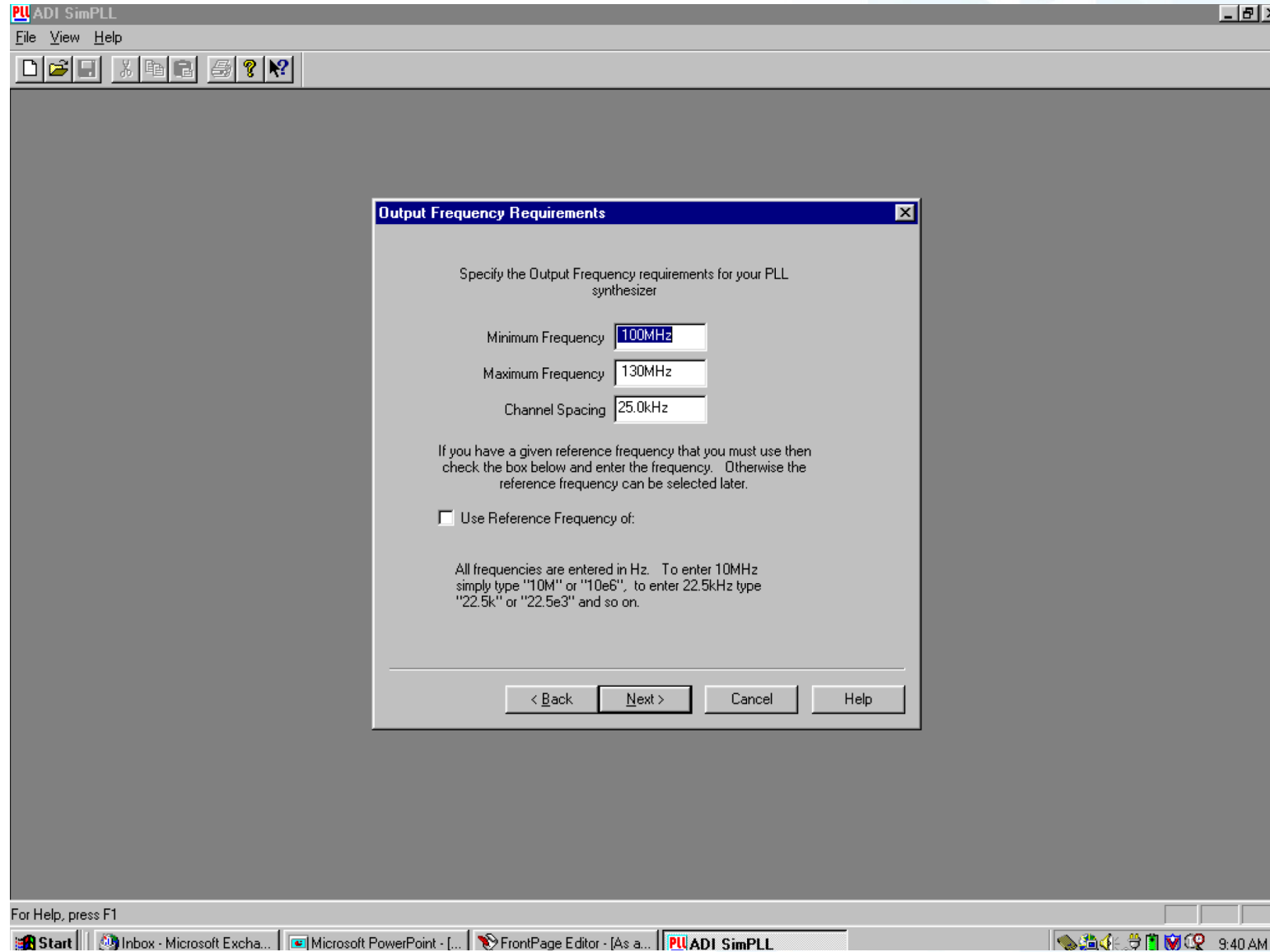
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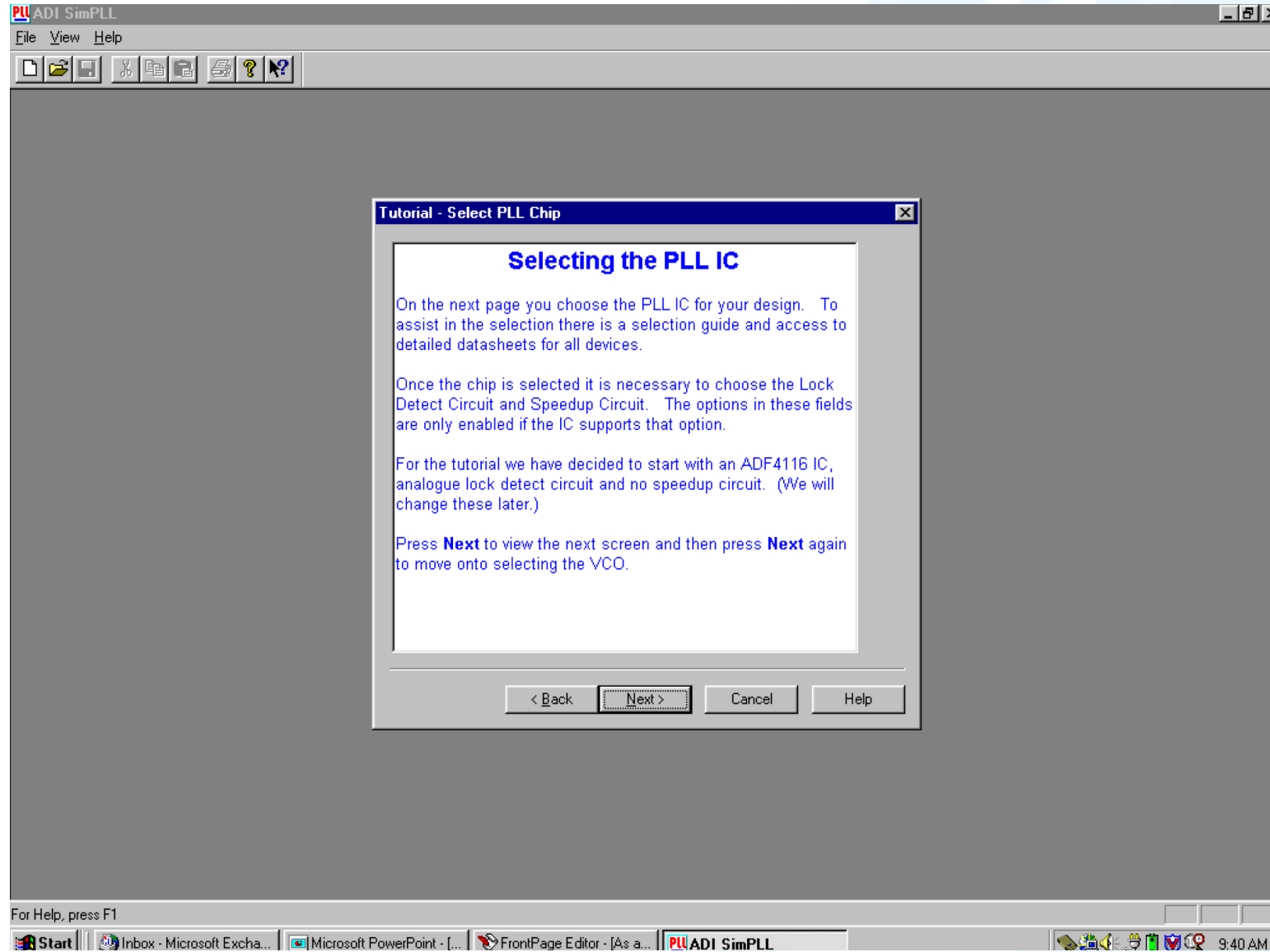
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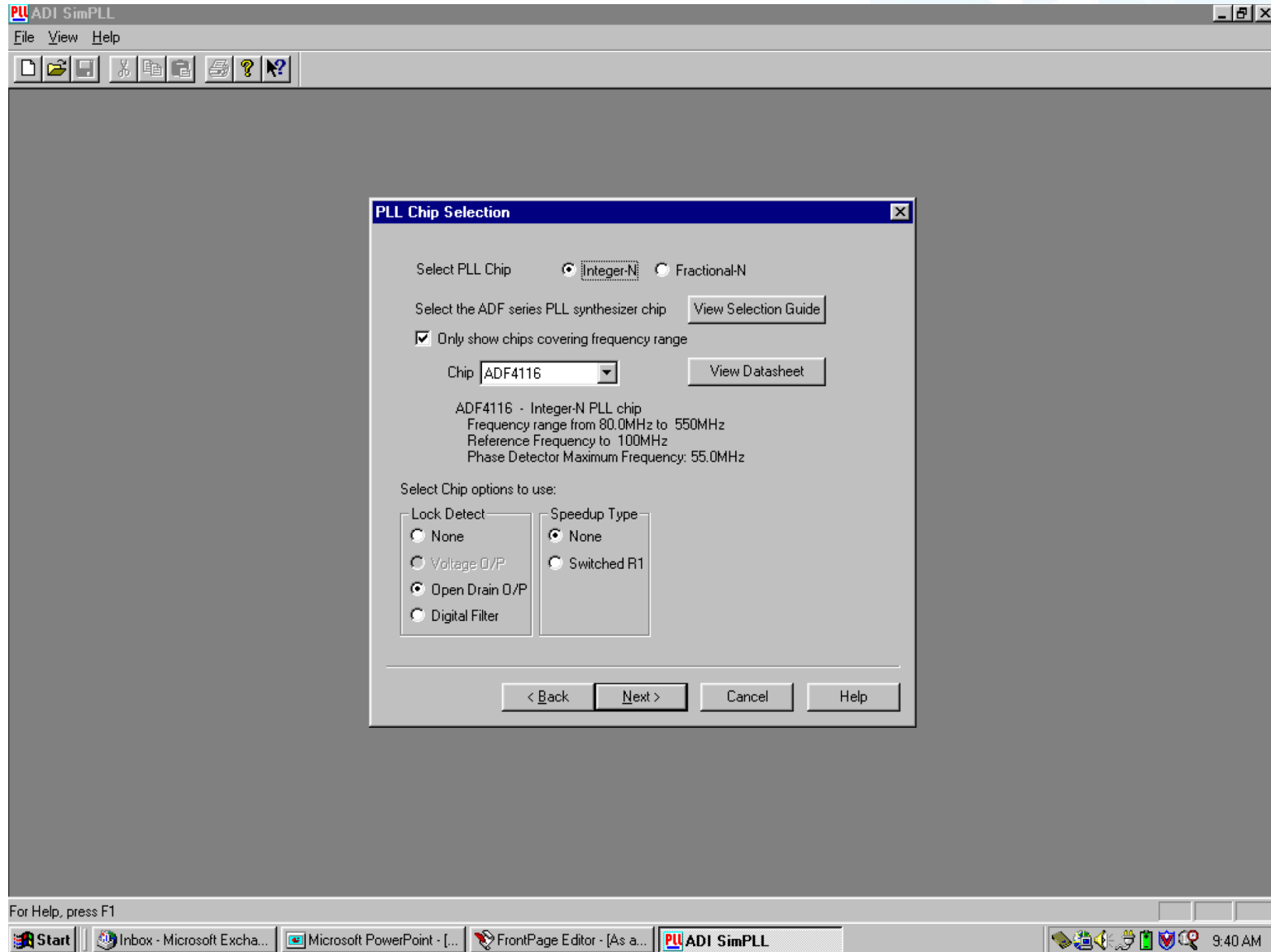


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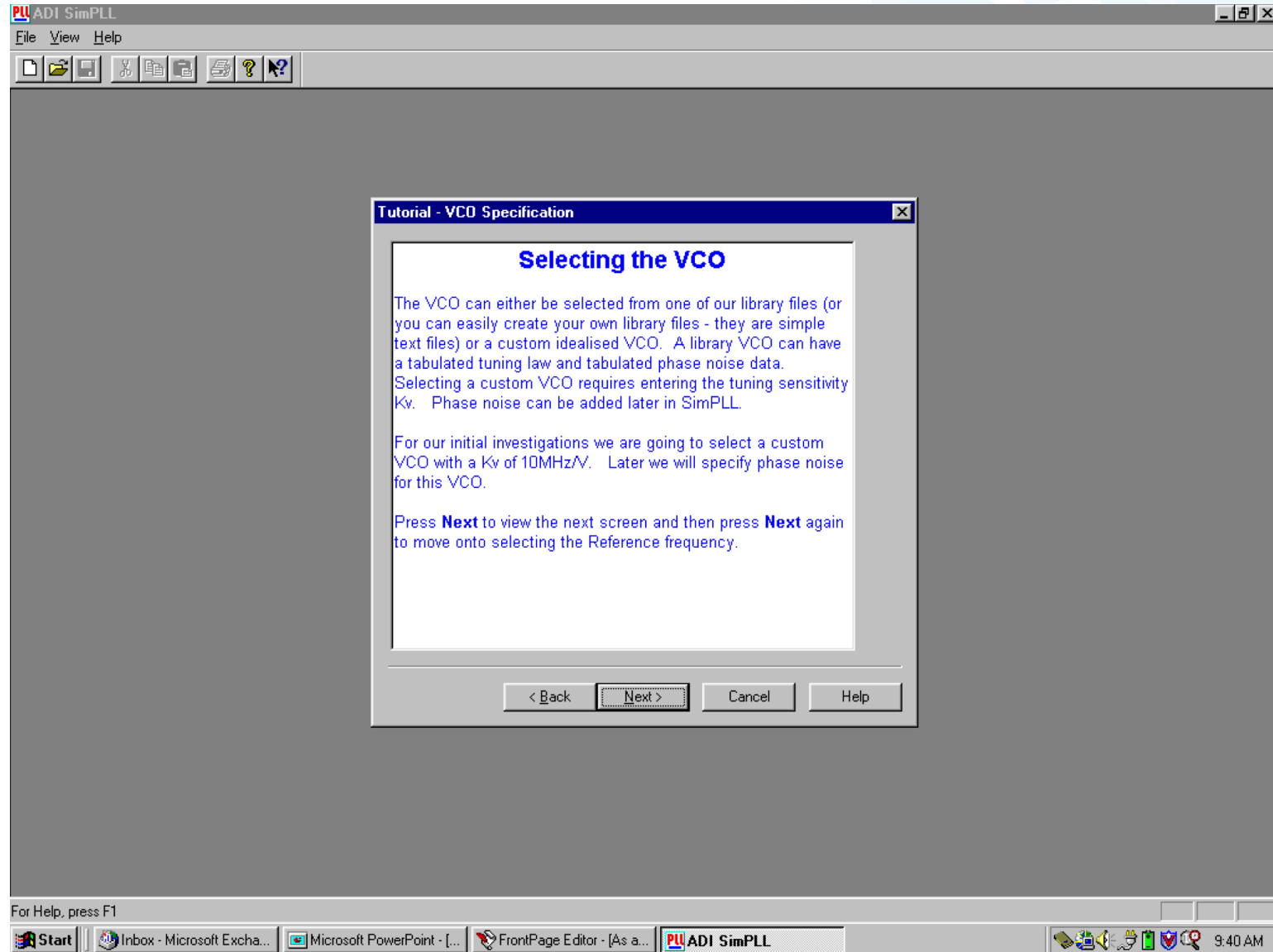


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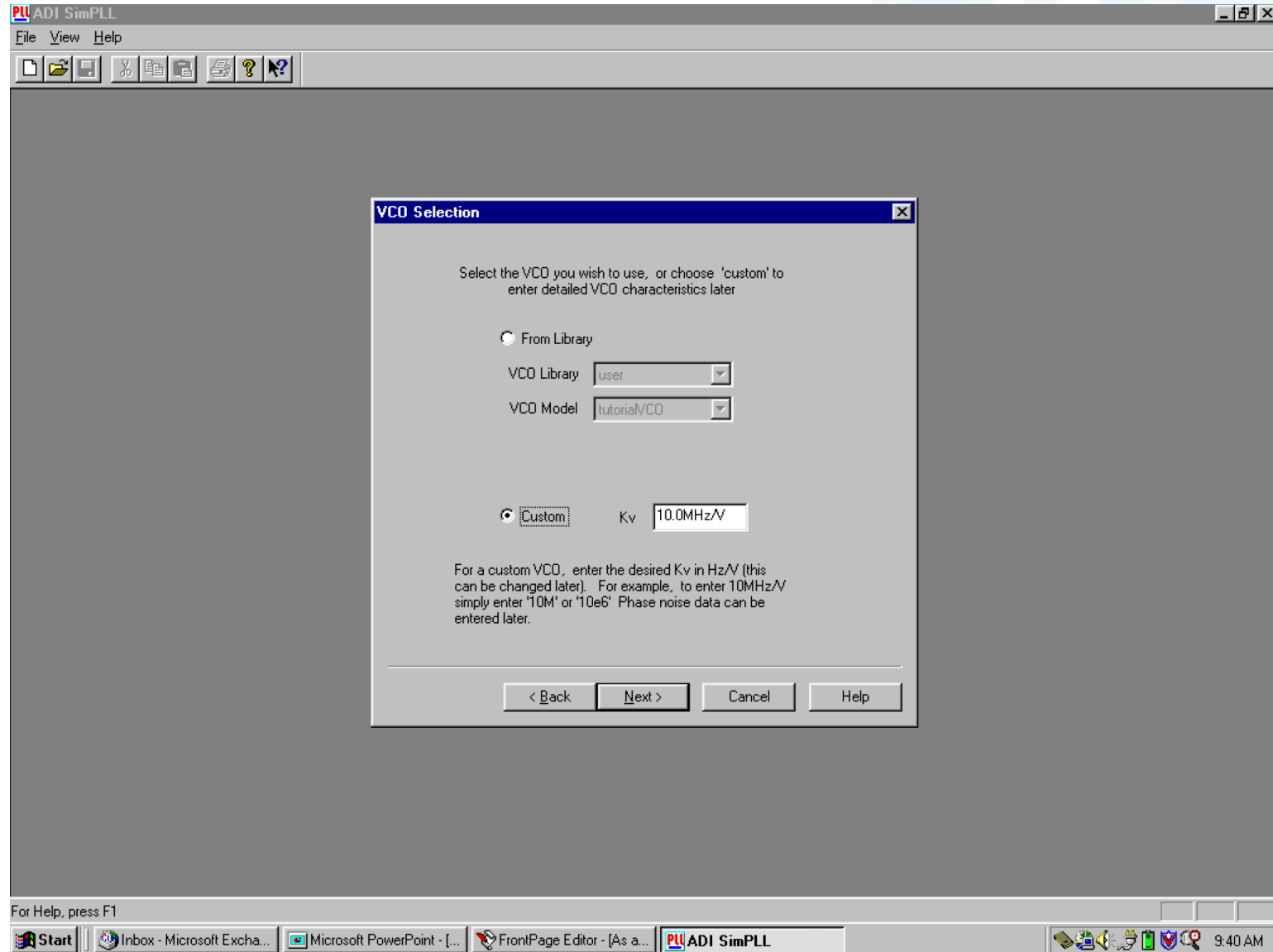


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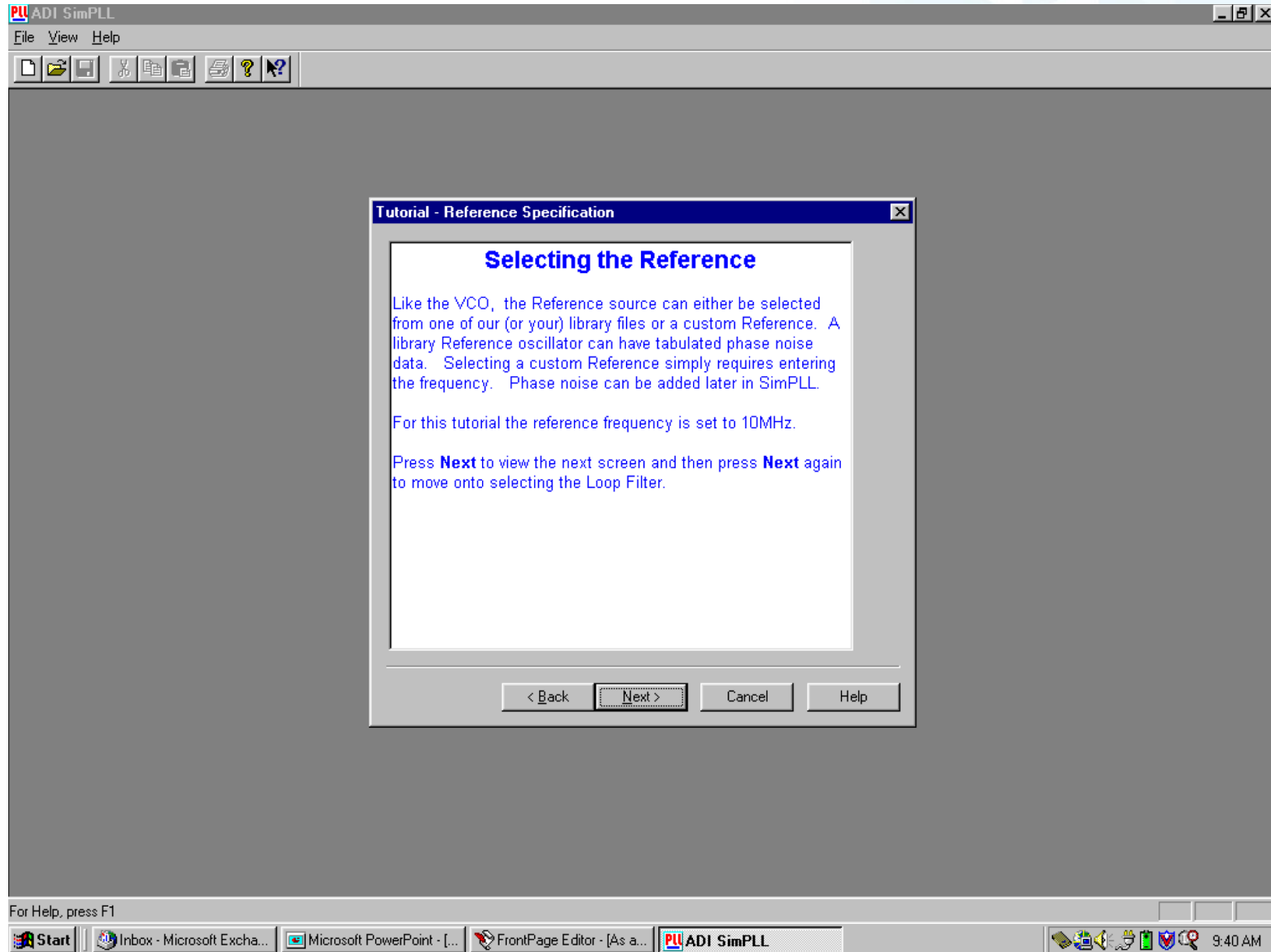
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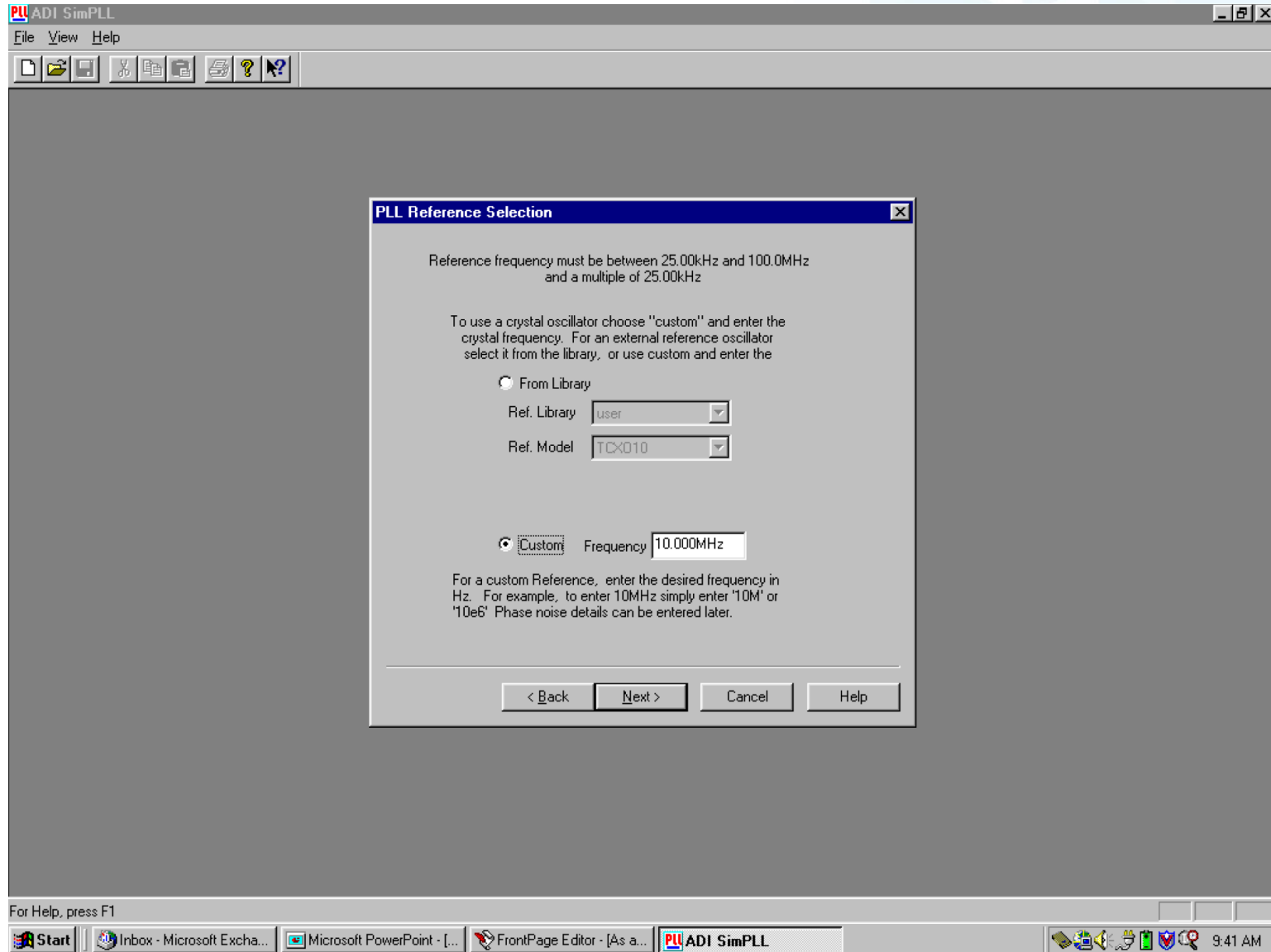


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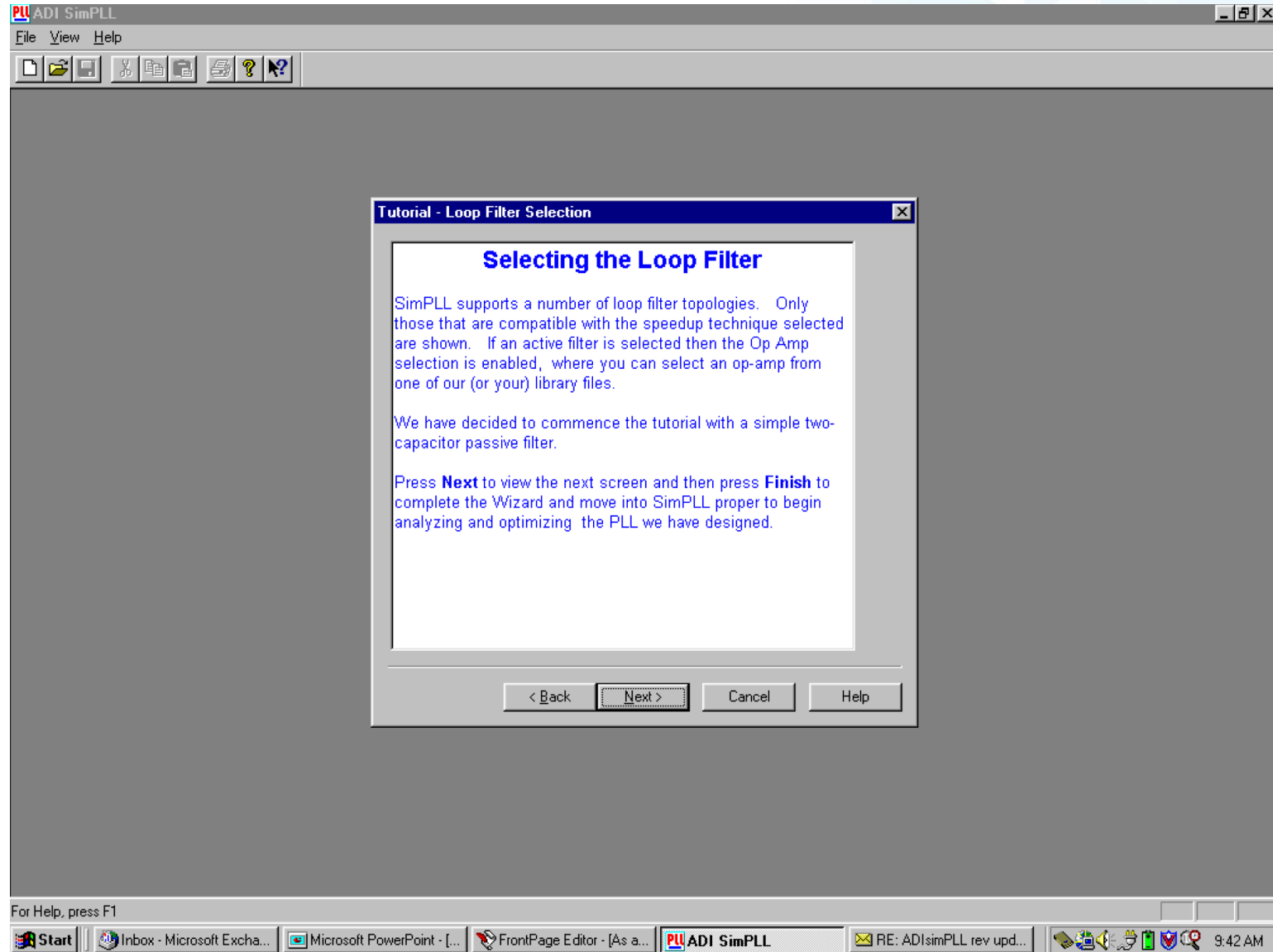
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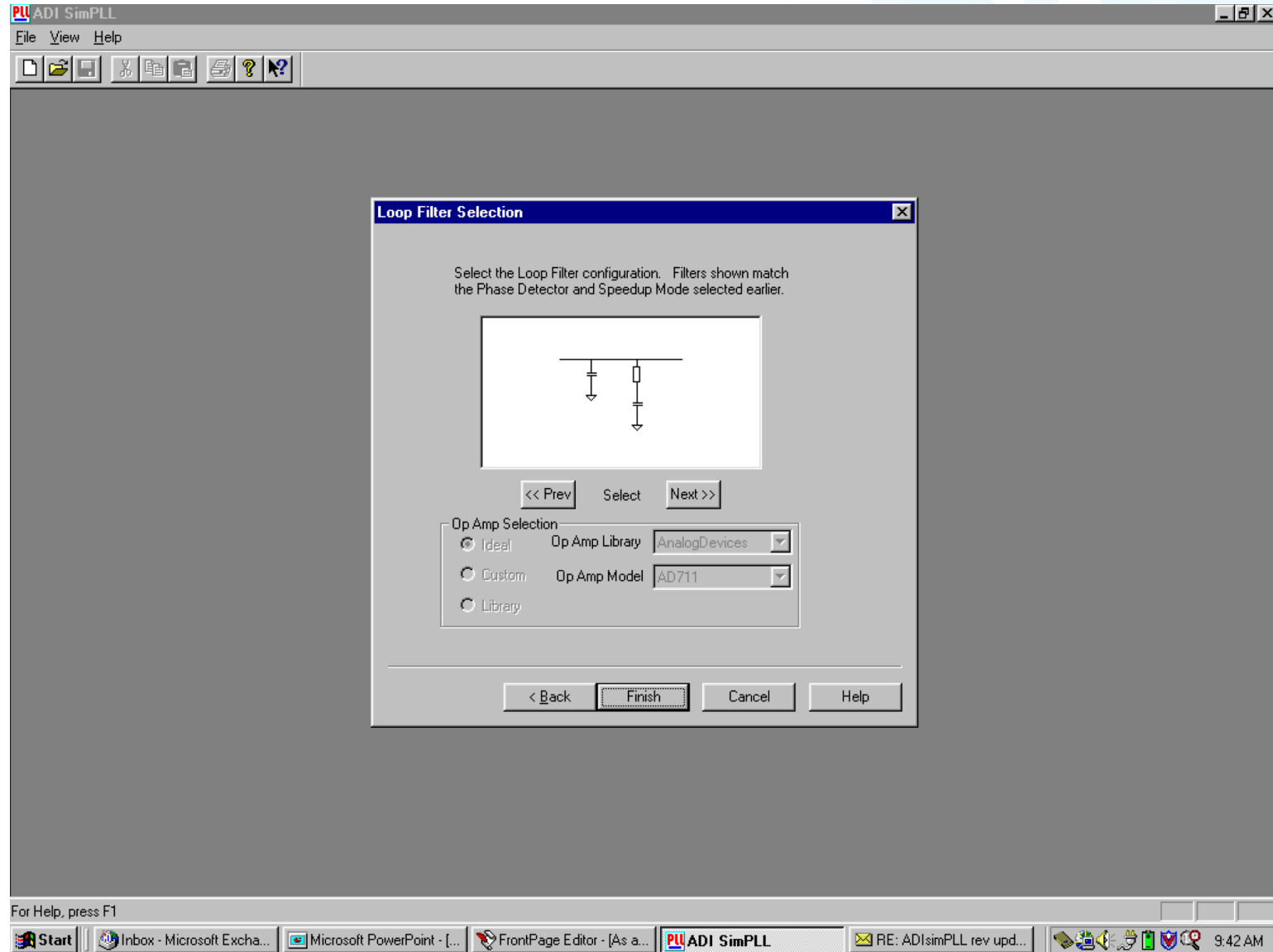


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ADI SimPLL - [Design1]

File Edit View Recalc Tools Window Help

System

- Reference custom
- VCO custom
- Chip ADF4116
- Loop Filter CPP_2C
- Lock Detect Analogue DD
- FreqDomain
- TimeDomain

Finding Your Way Around SimPLL

Let's have a quick look at the gadgets that will help you get around in SimPLL, and to get back to this tutorial.

Tutorial Navigation Buttons

<< >> These buttons are located in the lower right-hand corner of this document. They only appear when this tutorial is visible and are used to navigate between tutorial pages. Pressing >> advances to the next page, and << returns to the previous page.

To view the rest of this page you will need to use the scrollbar on the right.

Results Navigation Tabs

Tutorial VCO FreqDomain TimeDomain Schematic Report

The navigation tab bar appears below this tutorial text. It is used to move between pages of results, and this Tutorial when it is running. (Normally there is no Tutorial tab.) Click on the other tabs to see the other pages, make sure that you return to this tutorial page when you are ready to continue. If all the other tabs are not visible, use the mouse to drag the splitter bar at the left end of the scrollbar. Alternatively, if you are short of screenspace, the arrows at the left end of the tabs can be used to bring the obscured tabs into view.

Main Screen

OK, so you are already finding your way around the SimPLL screen. We just need to name a few parts of the screen. In normal usage the main screen of SimPLL is divided into two parts as shown below:

The screenshot shows the main SimPLL interface. The left side is the 'Data Panel' containing a list of components and their settings. The right side is the 'Results Panel' displaying two graphs: 'Frequency' and 'Phase Noise'. The 'Frequency' graph shows a peak at the center frequency, and the 'Phase Noise' graph shows the noise floor across a range of offsets. Navigation buttons (<< >>) are visible in the bottom right corner of the window.

For Help, press F1

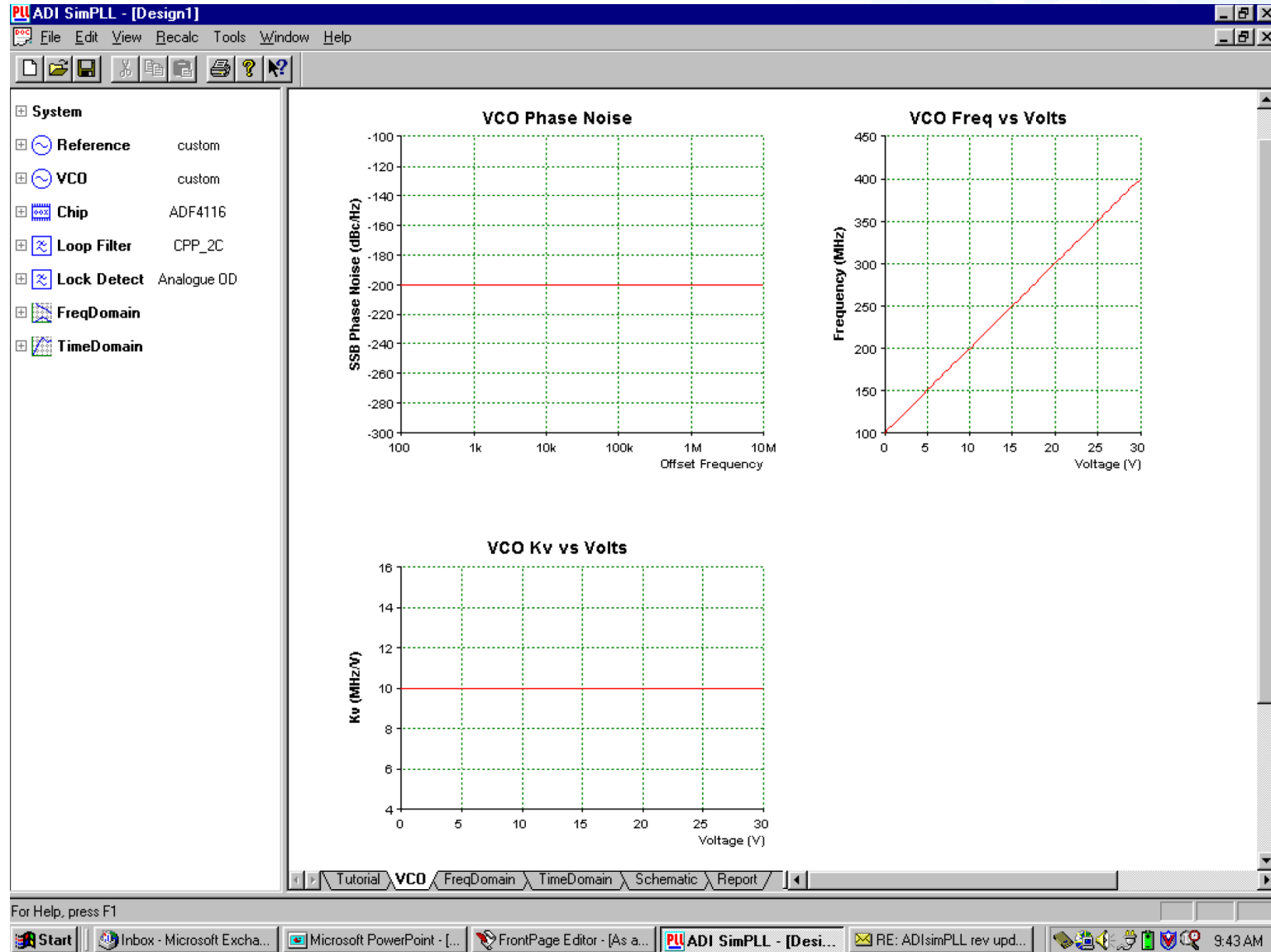
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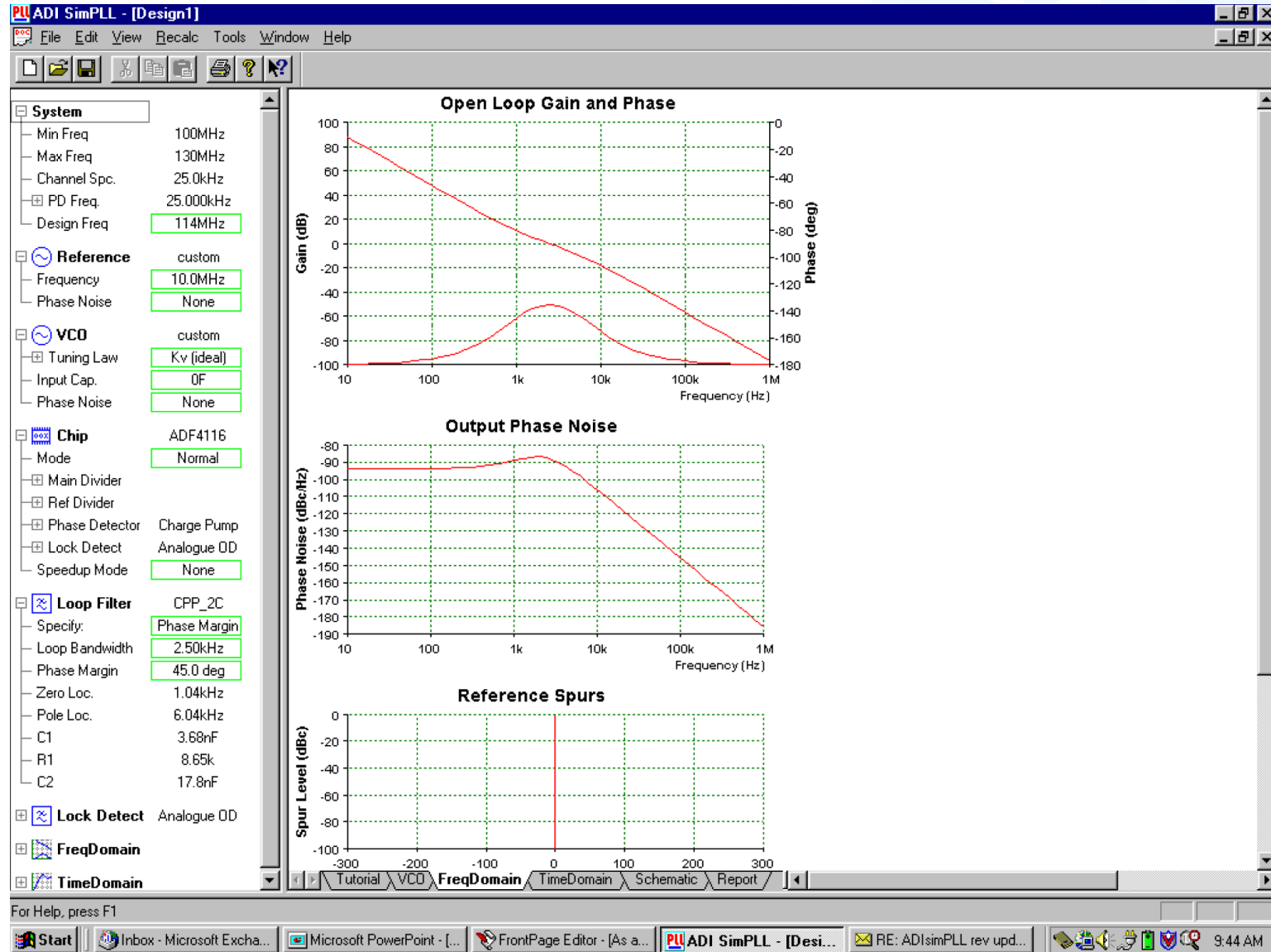


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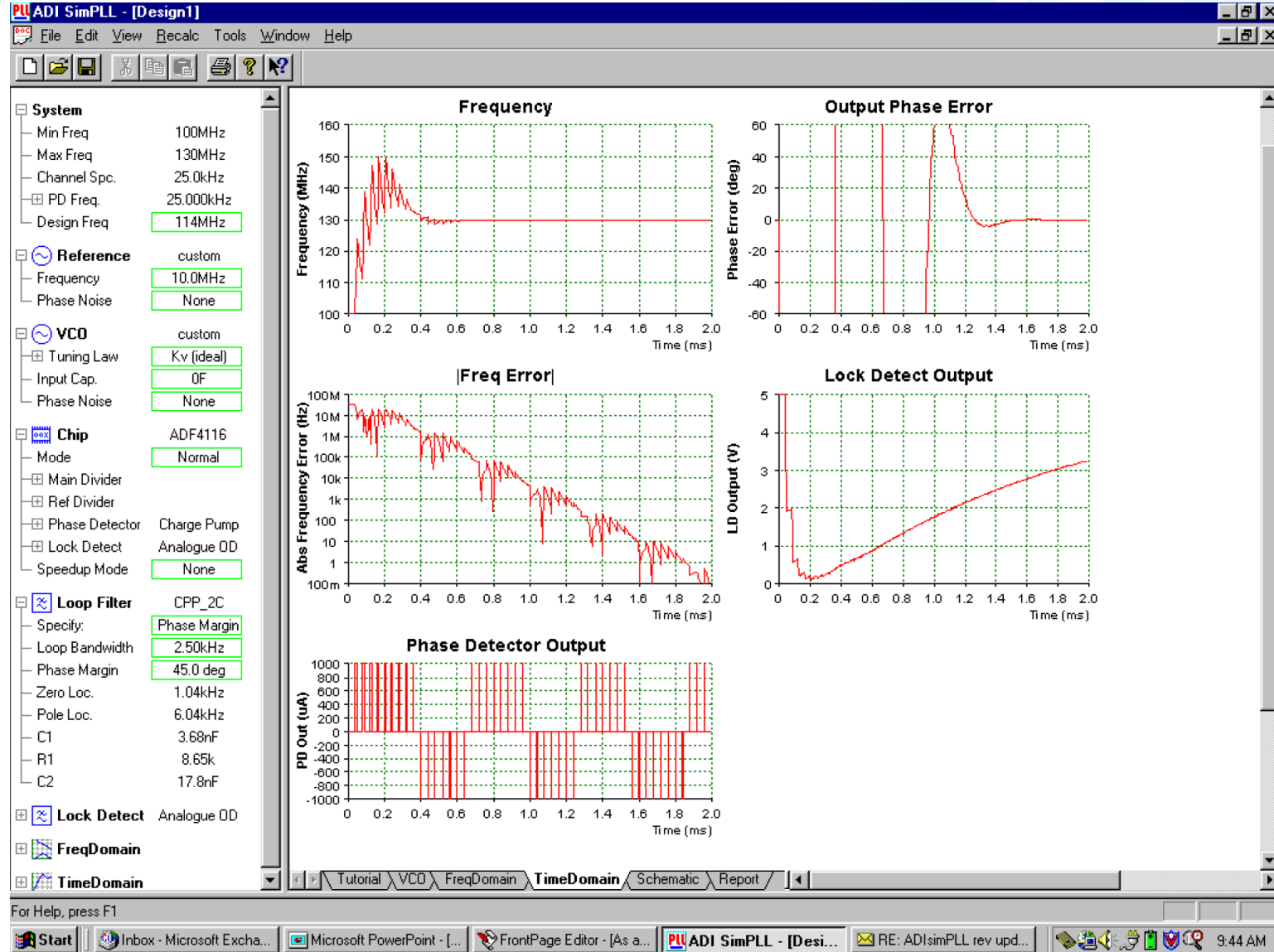


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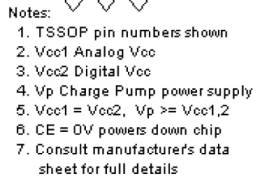
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ADI SimPLL - [Design1]

File Edit View Recalc Tools Window Help

Design1 analysed at 02/13/02 09:43:06

PLL Chip is ADF4116
VCO is custom
Reference is custom

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 114MHz

Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
100	-93.73	--	--	-93.81	-111.5
1.00k	-88.97	--	--	-91.73	-92.25
10.0k	-106.0	--	--	-110.5	-107.9
100k	-145.7	--	--	-150.3	-147.6
1.00M	-185.7	--	--	-190.3	-187.6

Phase jitter using brick wall filter
from 10.0kHz to 100kHz
Phase Jitter **0.02 degrees rms**

Carrier Recovery phase jitter
Carrier recovery bandwidth 6.40kHz damping factor 0.7071
Symbol Filter cutoff 32.0kHz Butterworth with 3 poles
Phase Jitter **0.09 degrees rms**

Residual FM
from 300 Hz to 5.00kHz is **8.52 Hz**

FM SNR
sinusoidal modulation with 10.0kHz peak deviation
Signal to Noise Ratio = **58.4 dB**

ACP - Channel 1
Channel 1 is centred 25.0kHz from carrier with bandwidth 15.0kHz
Power in channel = **-78.6dBc**

---- End of Frequency Domain Results ----

For Help, press F1

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