High Speed System Applications

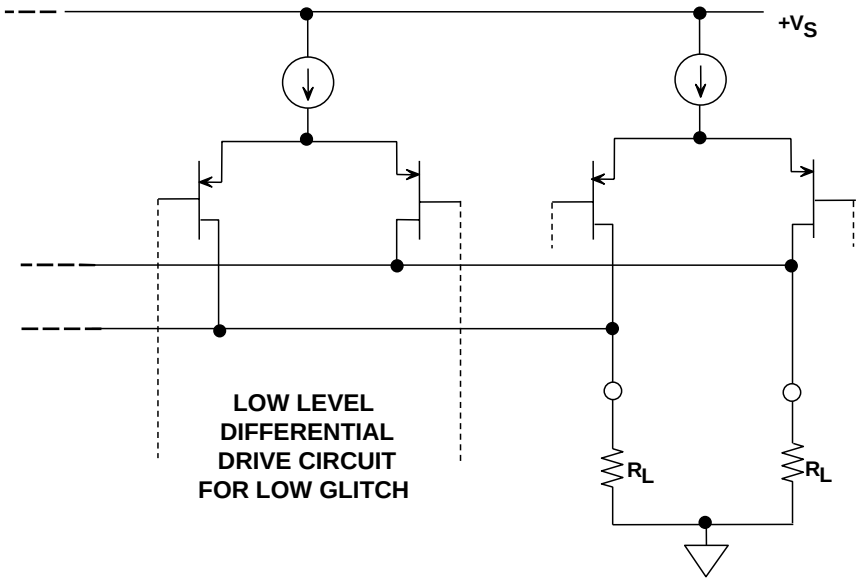
1. High Speed Data Conversion Overview
2. Optimizing Data Converter Interfaces
3. **DACs, DDSs, PLLs, and Clock Distribution**
4. PC Board Layout and Design Tools

SECTION 3
DACs, DDSs, PLLs, AND CLOCK DISTRIBUTION

High Speed CMOS DACs

www.analog.com/txdacs

PMOS Transistor Current Switches



This is a typical CMOS transistor current steering switch based on PMOS transistors. It is used in the TxDAC family.

The advantage of PMOS is that the output sources current and provides a signal which is above ground in a single-supply system. Both true and complementary current outputs are supplied in low distortion DACs allowing differential operation to minimize second-order distortion products.

An NMOS output stage would sink current, and provide a negative output voltage in a single-supply system. NPN or NMOS transistor-based DACs operate in this manner.

The outputs of the PMOS switches generally have 1V or 2V of compliance, and can usually go about 1V below ground. (Compliance is the allowable output voltage range over which the DAC meets its linearity specifications).

The basic PMOS current switch is driven from a low-level differential signal whose level and amplitude has been optimized to produce a minimum switching glitch at the DAC output. The following references describe the basic method used in optimizing the current switching action in the TxDAC family as well as other details of their design:

---

1. Doug Mercer, "Low Power Approaches to High Speed CMOS Current Steering DACs," *CCIC 2006 Conference Proceedings*.

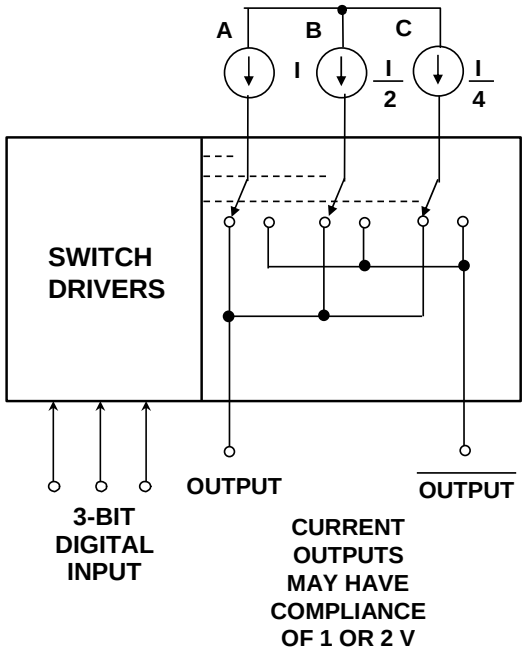
2. Doug Mercer, "A Low Power Current Steering Digital-to-Analog Converter in 0.28 micron CMOS," *ISLPED 2005 Digest of Technical Papers*.

3. Doug Mercer, "A Study of Error Sources in Current Steering Digital-to-Analog Converters," *CCIC 2004 Conference Proceedings*.

4. W. Schofield, Doug Mercer, and L. St. Onge, "A 16b 400MS/s DAC with <–80dBc IMD to 300MHz and <–160dBm/Hz Noise Power Spectral Density," *ISSCC 2003 Digest of Technical Papers*.

5. Doug Mercer, "A 16b D/A Converter with Increased Spurious Free Dynamic Range," *IEEE Journal of Solid State Circuits*, vol. 29, no. 10, pp. 1180-1185, October 1994.

High Speed 3-Bit Binary DAC with Complementary Current Outputs



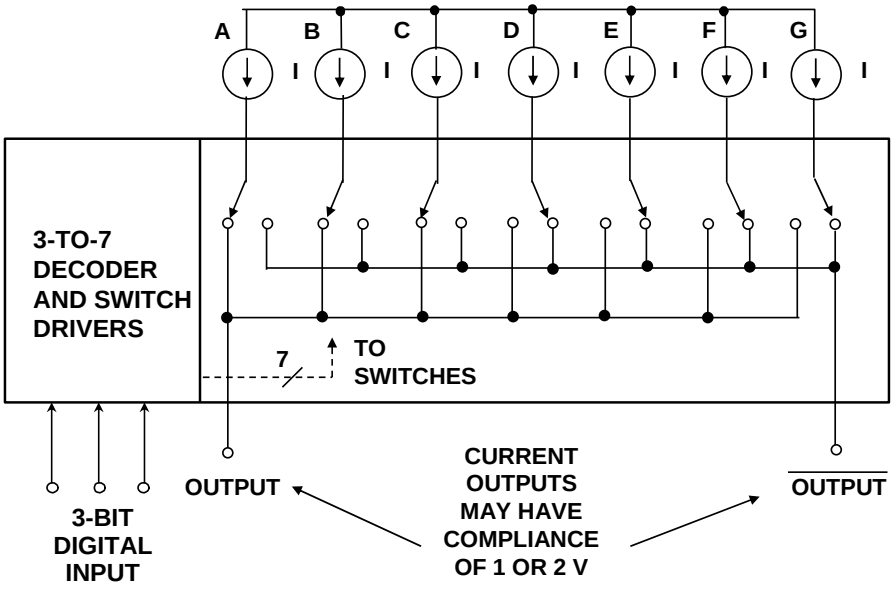
PMOS current switches available in digital CMOS processes can be used to construct simple binary-weighted DACs as shown here for a 3-bit DAC. There are two basic problems in using this architecture for high resolution fast DACs.

The first problem is maintaining the correct binary ratio between the currents for high resolutions. For resolutions greater than about eight bits, some type of trimming is required in order to maintain the required accuracy.

The second problem is the switching glitches of the binary DAC tend to be code dependent. That is, the switching transient generated at the bit-1 transition, 011 to 100, tends to be larger than the switching transient generated at the bit-2 transitions, 101 to 110, or 001 to 010.

The code-dependent glitches produce various unwanted harmonics of the fundamental output frequency. Basic sampling theory tells us that the higher order products which fall outside the Nyquist bandwidth (dc to $f_s/2$) will alias back into the Nyquist bandwidth where they may add distortion to the desired output frequency.

High Speed 3-Bit Thermometer (Fully Decoded) DAC with Complementary Current Outputs



While it is impossible to totally eliminate DAC switching glitches, it is possible to use architectures which produce glitches that are code-independent and occur at the DAC update rate.

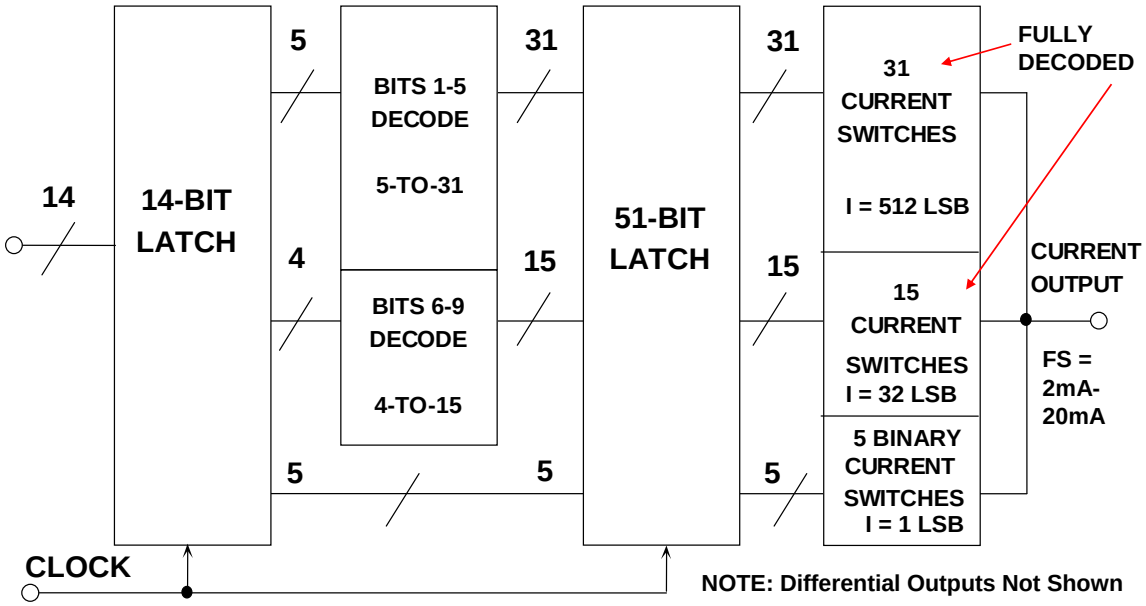
This figure shows a "thermometer" or "fully-decoded" DAC based on equal value current sources and switches. This architecture minimizes the code dependent glitches at the expense of an increase in the number of current sources and switches to obtain the same 3-bit resolution.

The thermometer DAC also makes it easier to match each stage, since the currents are equal.

The problem with this architecture is the physical size and power required to implement high resolutions. For instance, an 8-bit thermometer DAC requires 255 current sources and switches. (Note that the concept of a thermometer DAC is similar to that of a flash ADC).

The thermometer DAC and binary DAC architectures can be combined to produce a "segmented" architecture which makes an excellent compromise between performance and chip area.

Typical TxDAC® 14-Bit CMOS Segmented DAC Core



This figure shows a typical example of a 14-bit core of the TxDAC family. This is an excellent illustration of the "segmented" DAC architecture. The five MSBs are fully decoded into 31 equal current switches. The next four bits are fully decoded into 15 equal current switches. The five LSBs are binarily decoded.

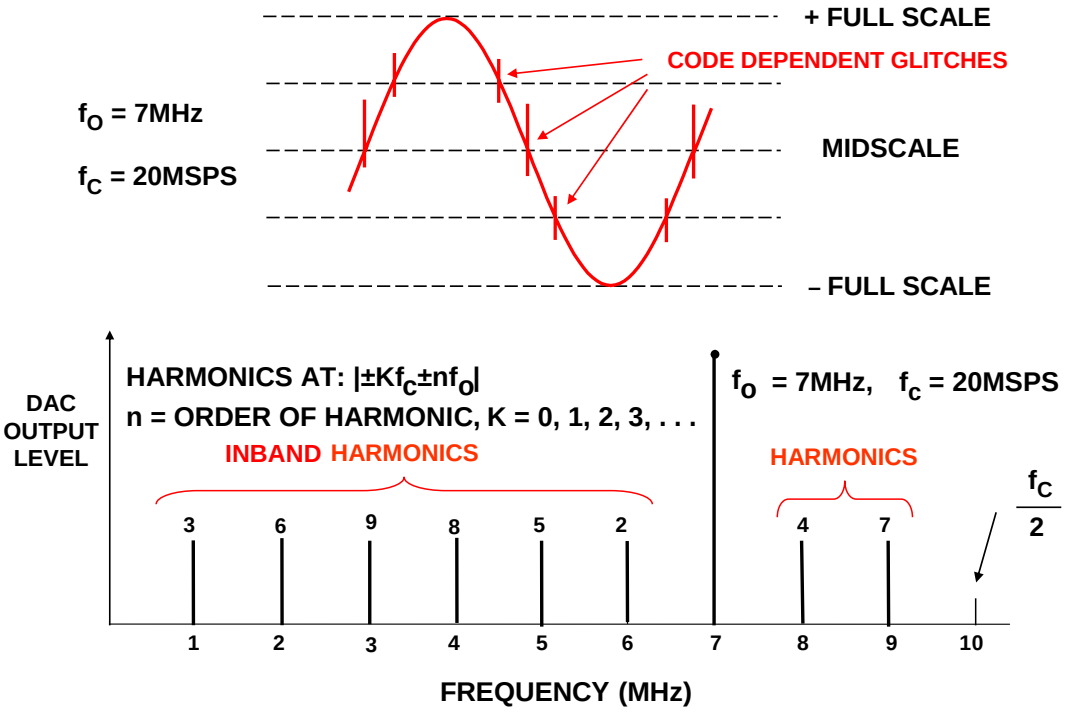
Note that a second latch (51 bits) is used to drive the output current switches. This eliminates the delay "skew" added by the decoding logic which follows the input 14-bit latch.

All the currents are combined to produce the final output current.

This architecture yields excellent low-distortion performance.

In practice, the DAC is fully differential for better linearity and to minimize second-order distortion.

Location of First Nine Harmonic Products: Output Signal = 7MHz, DAC Update Rate = 20MSPS



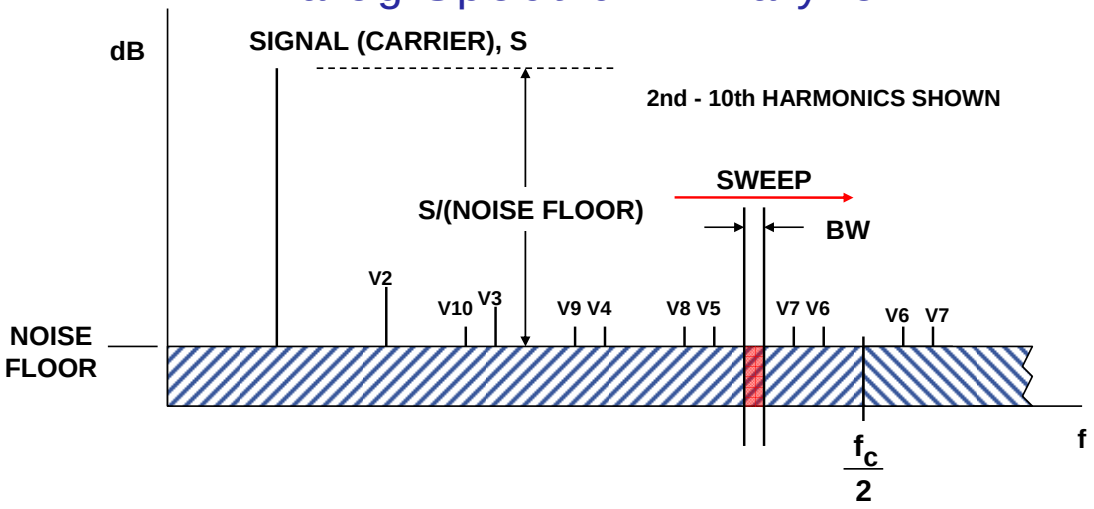
This figure shows how code dependent glitches produce harmonics which alias back into the Nyquist bandwidth.

In this case, the DAC is updated at a 20MSPS rate and produces a 7-MHz output signal. The figure shows the location of the first nine harmonics.

Aliased harmonics of f_O fall at frequencies equal to $|\pm Kf_C \pm nf_O|$, where n is the order of the harmonic, and K = 0, 1, 2, 3, ...

It is often desirable to carefully select the DAC update rate and the output frequency such that the worst harmonics do not interfere with the signal band of interest. Locating the position of the higher order harmonics is facilitated by an on-line design tool from Analog Devices, the "DAC Harmonic Image" tool. This tool is described in more detail later in this section.

Measuring DAC Distortion and SNR with an Analog Spectrum Analyzer

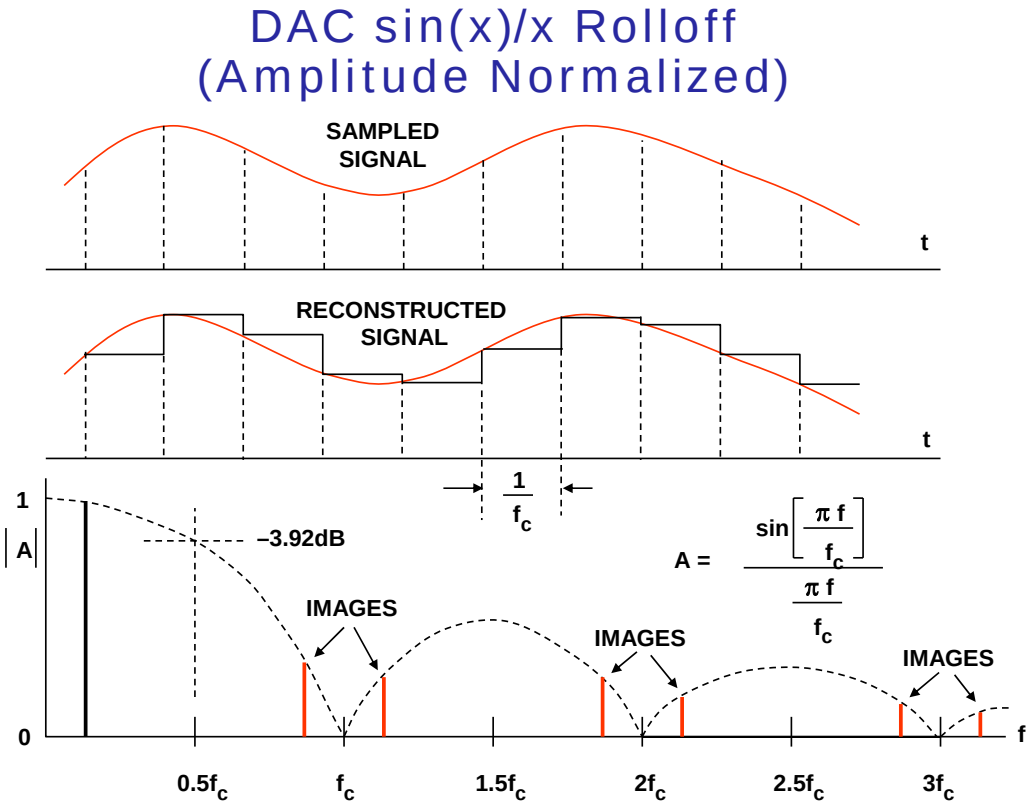


- BW = ANALYZER RESOLUTION BANDWIDTH
- $SNR = S/(NOISE\ FLOOR) - 10 \log_{10}\left[\frac{f_c/2}{BW}\right]$

Analog spectrum analyzers are used to measure the distortion and SFDR of high performance DACs. Care must be taken such that the front end of the analyzer is not overdriven by the fundamental signal. If overdrive is a problem, a bandstop (notch) filter can be used to filter out the fundamental signal such that the spurious components can be observed.

Spectrum analyzers can also be used to measure the SNR of a DAC provided attention is given to bandwidth considerations. SNR of an ADC is normally defined as the signal-to-noise ratio measured over the Nyquist bandwidth dc to $f_c/2$. However, spectrum analyzers have a resolution bandwidth which is less than $f_c/2$—this therefore lowers the analyzer noise floor by the *process gain* which is equal to $10 \cdot \log10[f_c/(2 \cdot BW)]$, where BW is the resolution noise bandwidth of the analyzer.

It is important that the noise bandwidth (not the 3-dB bandwidth) be used in the calculation, however the error is small assuming that the analyzer narrowband filter is at least two poles. The ratio of the noise bandwidth to the 3-dB bandwidth of a one-pole Butterworth filter is 1.57 (causing an error of 1.96 dB in the process gain calculation). For a two-pole Butterworth filter, the ratio is 1.11 (causing an error of only 0.45 dB in the process gain calculation). Using more than two poles makes essentially no difference in the effectiveness of the noise filter.



Here we see the effects of the sin(x)/x rolloff which occurs when the reconstructed signal is not composed of ideal impulses, but NRZ analog "boxcar" data as shown. This is often referred to as a "zero-order hold" output and affects all DACs.

The NRZ boxcar output is used because it is easier to generate with more energy and less distortion than data composed of narrow pulses.

At $f_C/2$, the output is attenuated by 3.92dB.

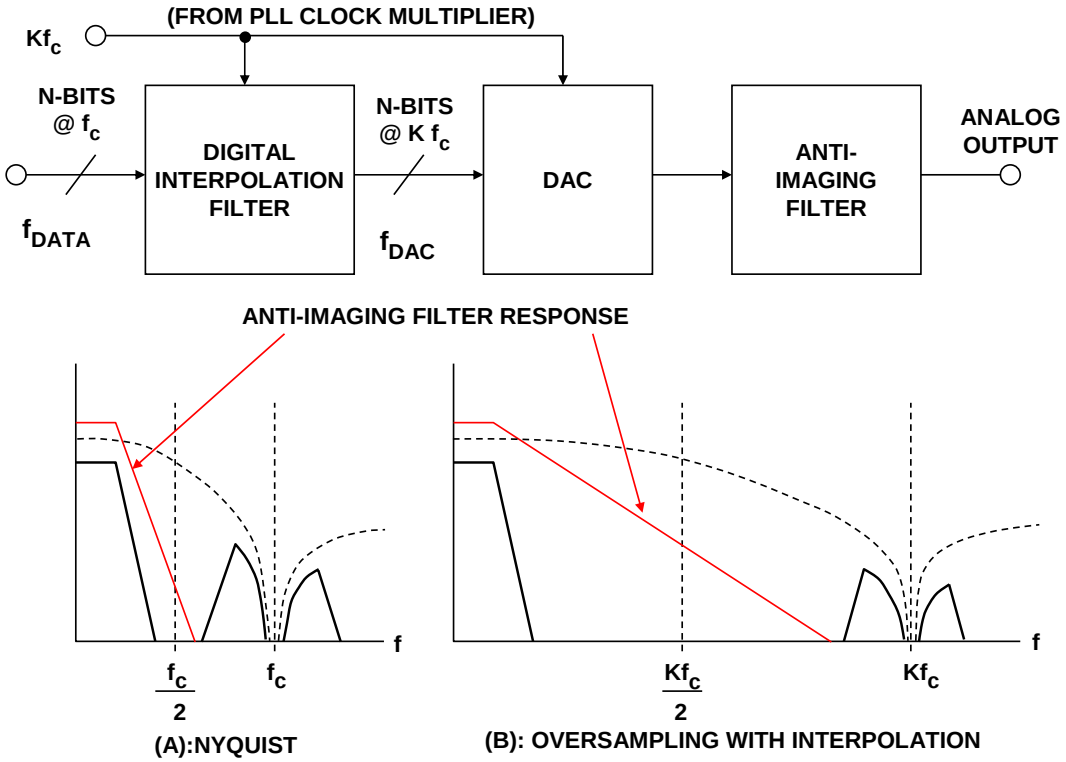
Theoretically, digital upconversion could be achieved by using a bandpass filter to pass one of the higher order images rather than the baseband signal. This method is limited, however, because of the reduced amplitude caused by the sinx/x rolloff. Details of the technique can be found in the following references:

---

1. Ken Gentile, "Digital Upconverter IC Tames Complex Modulation," *Microwaves and RF*, August 2000.

2. Allen Hill and Jim Surber, "Using Aliased-Imaging Techniques in DDS to Generate RF Signals, *RF Design*, September 1993, pp. 31-36.

Oversampling Interpolating DAC

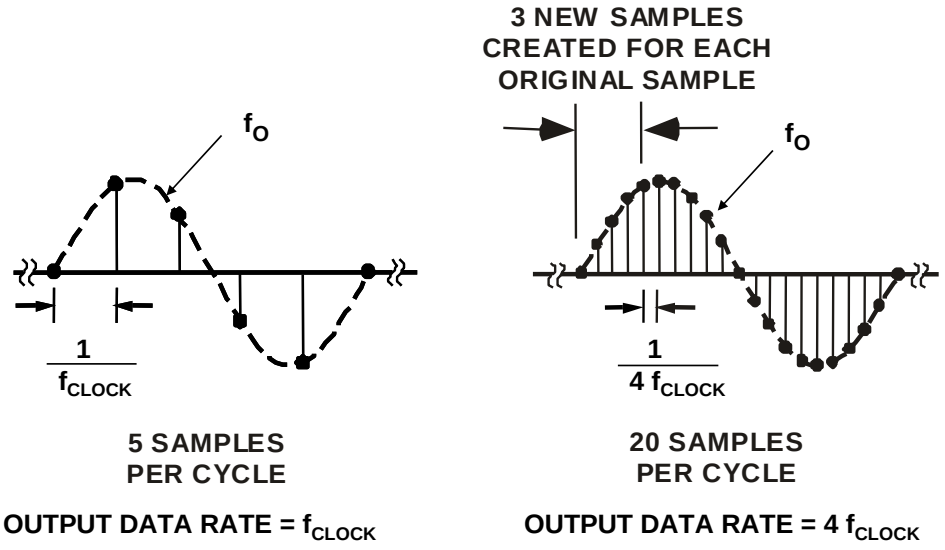


In ADC-based systems, oversampling can ease the requirements on the antialiasing filter. In a DAC-based system (such as DDS), the concept of oversampling and interpolation can be used in a similar manner. This concept is common in digital audio CD players, where the basic update rate of the data from the CD is 44.1kSPS. Early CD players used traditional binary DACs and inserted "Zeros" into the parallel data, thereby increasing the effective update rate to 4-times, 8-times, or 16-times (sometimes more) the fundamental throughput rate. The 4×, 8×, or 16× data stream is passed through a digital interpolation filter which generates the extra data points. The high oversampling rate moves the image frequencies higher, thereby allowing a less complex reconstruction filter with a wider transition band and less phase shift. The sigma-delta 1-bit DAC architecture uses a much higher oversampling rate and represents the ultimate extension of this concept and has become popular in modern CD players.

The same concept of interpolation can be applied to high speed DACs used in communications applications as shown here, relaxing the requirements on the output filter as well as increasing the SNR due to process gain.

Note that the traditional Nyquist condition is shown in (A), where the maximum output frequency of the DAC is generally no more than $f_c/3$. Increasing the DAC output data rate, f_{DAC}, by a factor of K allows a much less complex anti-imaging filter as shown in (B). The digital interpolation filter generates the extra data points as shown in the next figure.

Oversampling and Interpolation in the Time Domain

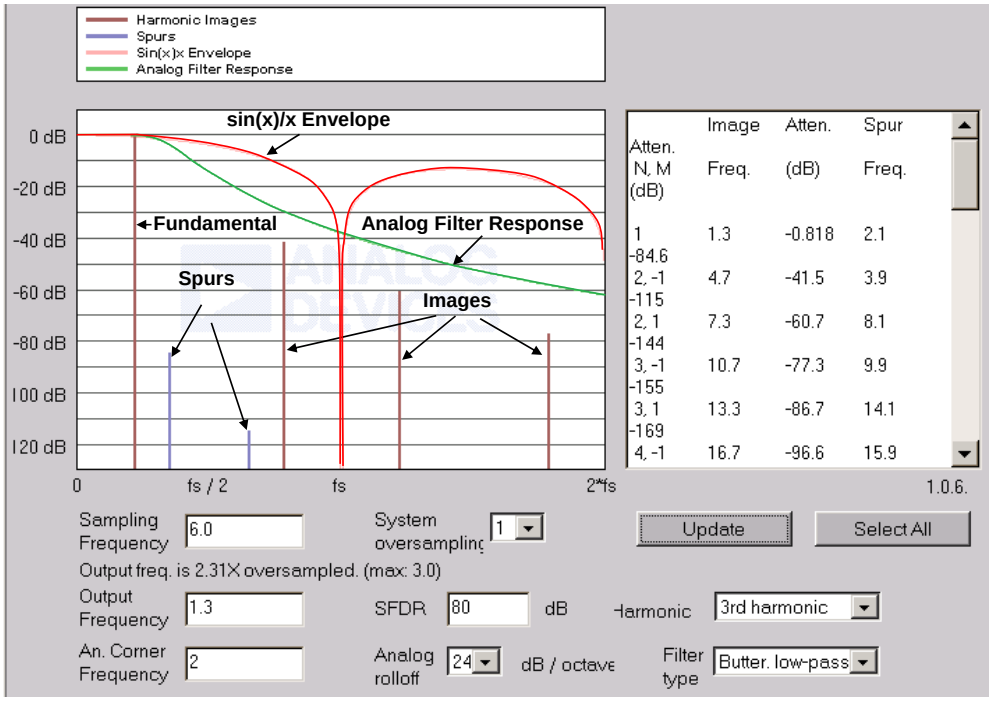


This example shows how oversampling and digital interpolation works in the time domain. The figure on the left shows the basic input data to the interpolating DAC before interpolation. In this example, there are five samples per cycle of the output sinewave. The output data rate is equal to f_{CLOCK}.

The right-hand diagram shows what happens when the interpolation filter is used to increase the sample rate by a factor of 4. Now, there are 20 samples per cycle, and the digital interpolation filter creates three "new" samples for each original sample. The new output data rate is now equal to $4f_{CLOCK}$.

It is important to note that the bandwidth of the output signal is always limited by the Nyquist criteria, which is determined by the initial output data rate, f_{CLOCK}. The interpolation process does not increase the information contained in the original input data stream, it simply adds the extra data points, increases the output data rate, and makes filtering the images an easier problem to solve.

Using the DAC Harmonic Image Tool



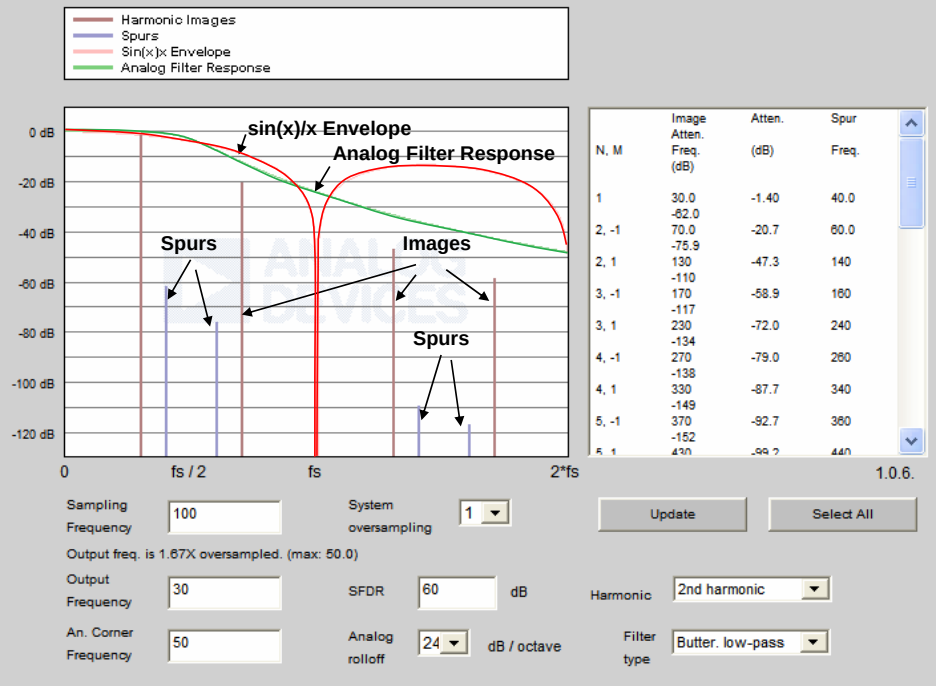
The DAC Harmonic Image tool demonstrates harmonic images and spurs in an idealized DAC output. Second and third harmonics are supported by the tool.

Images are located at N·Fs + M·Fo, where M = ±1. Without external filtering image amplitudes roll off as sin(x)/x where x = π·Fo/Fs. Spurious 2nd or 3rd harmonics of the fundamental are assumed to result from DAC nonlinearities and so remain folded within the baseband. These spurs in turn have their own harmonic images that roll off as sin(x)/x.

To illustrate suppression of these images, the tool can apply a simulated post-DAC analog filter. The output signal is assumed to have been generated at the DAC update rate (or perfectly reconstructed from a lower data rate). Harmonics must be supressed by analog filtering.

The total attenuation of a given harmonic is the sum of the sin(x)/x attenuation and the analog filter attenuation.

Harmonic Images Design Tool (Ideal DAC)
Placement of 2nd Harmonic Spurs



In order to use the tool, enter the Sampling Frequency or Oversampling Ratio in the fields provided.

Hit "Enter" or click "Update" to recompute the display. This slide shows the locations of the second harmonics.

Select the Analog Corner Frequency. Behavior of this hypothetical DAC is assumed frequency-independent, so only frequency ratios matter—the units must be uniform, but are otherwise irrelevant.

Select filter rolloff and type. Butterworth, Chebychev, lowpass and highpass filters are supported with rolloffs up to 48dB/octave. The analog filter response is shown in green.

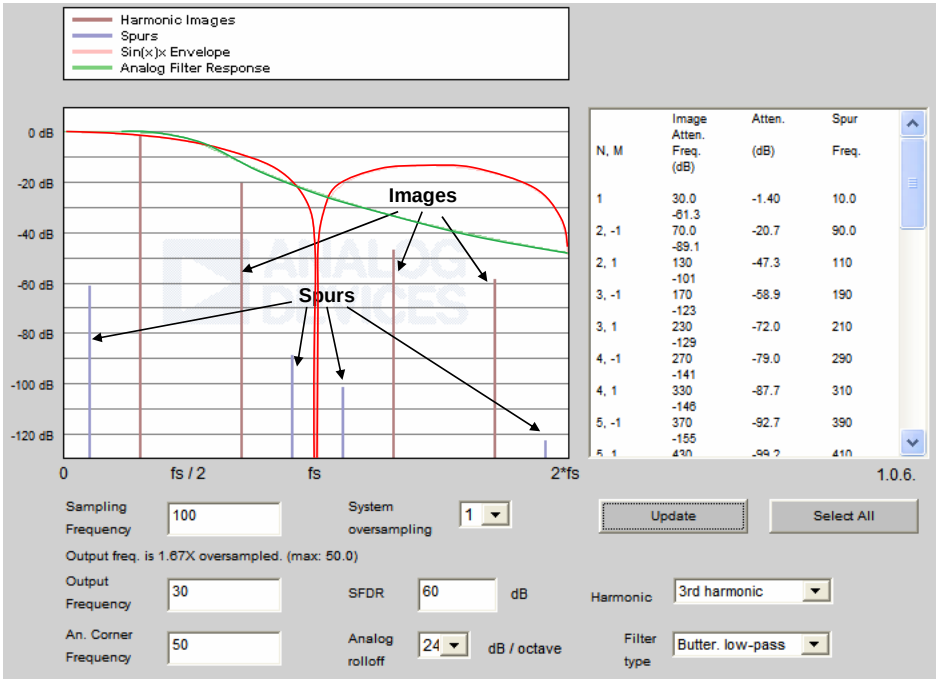
Image frequencies and amplitudes are shown in a table at top right. The first column gives the N value and whether it's ± Fo (M = ±1). The table data is selectable and can be copied and pasted into a spreadsheet. Use "Select all" to conveniently select the entire contents before copying.

Experiment by changing the analog filter parameters and comparing the results to changing the Oversampling Ratio. Changing the oversampling ratio changes the Sampling Frequency but the reverse is not true—it's sampling frequency that's important and the oversampling ratio menu is just a convenience.

SFDR is used to set the relative level of spurs, which are assumed here to be the result of DAC nonlinearity. Harmonic selects whether these distortion spurs are most prominent at 2× or 3× (default) the Output Frequency. By varying the output frequency in small increments, you can see how the harmonics move and fold.

SFDR is a DAC data sheet parameter and, in general, depends on both the sample rate and output frequency, among other variables. However, a single compromise number is often specified.

Harmonic Images Design Tool (Ideal DAC)
Placement of 3rd Harmonic Spurs

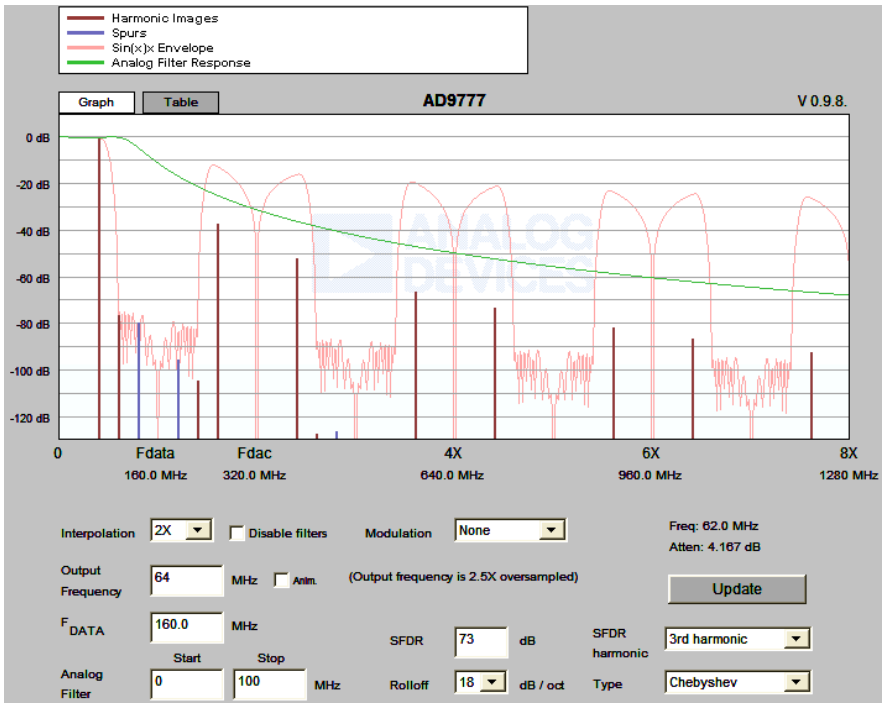


This figure is for the same conditions, but shows the placement of the third harmonics.

Again, the program assumes that the level of the harmonics is equal to the SFDR of 60dB.

For instance, the harmonic at 90MHz is attenuated by the analog filter attenuation (approximately 20dB) and the sin(x)/x rolloff (approximately 20dB) for a total attenuation of 40dB, placing the spur level at 60 + 40 = 100dB below fullscale.

Harmonic Images Tool (AD9777 Interpolating TxDAC)



The tool above shows the harmonic images and spurs for single frequency output from an AD9777. The model of the AD9777 is simplified and idealized—only SFDR is modeled, and it is assumed frequency-independent. See the data sheet for actual performance data.

For an ordinary DAC (see previous DAC Harmonic Images Calculator), images are located at $N \cdot F_{DAC} \pm F_{OUT}$ and follow a sin(x)/x envelope (shown by default). The AD9777 contains an integral interpolator which doubles, quadruples, or octuples the input data rate by stuffing zeros between successive samples and then (optionally) filtering the result. Both the filtered and unfiltered images then create further images and spurs at the DAC data rate, according to the $N \cdot F_{DAC} \pm F_{OUT}$ rule. The magnitude response of the AD9777 combining its internal interpolation with the sin(x)/x envelope is shown.

The AD9777 can optionally modulate the filtered data stream by F_{DAC} / 2, 4, or 8, shifting the output spectrum and creating mirror images around the modulating frequency. These images follow separate magnitude envelopes so two envelopes are shown in different colors in this case. This release only models real modulation. Complex modulation is planned for a future release.

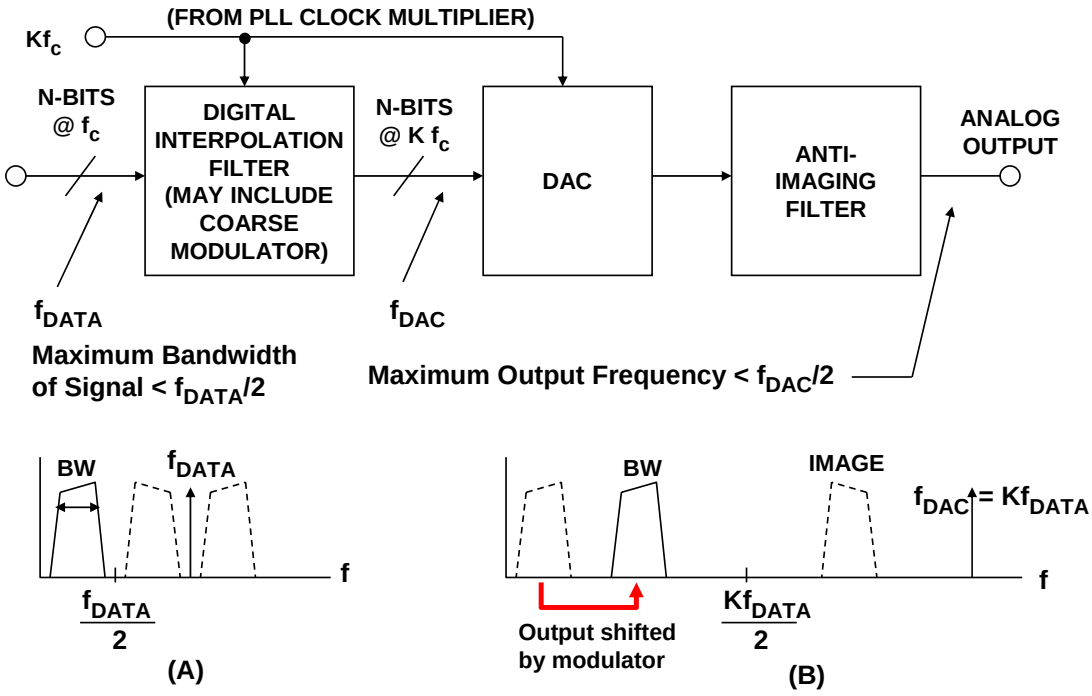
Spurious second or third harmonics of each image are assumed to result from D/A conversion nonlinearities and so are folded within the first Nyquist Zone (NZ) of F_{DAC}. These spurs then have their own harmonic images that roll off as sin(x)/x (where $x = \pi \cdot F_{SPUR}/F_{DAC}$).

To show external selection/suppression of desired/undesired images and spurs, the tool can apply a simulated post-DAC analog filter.

DAC Applications in Transmitters

www.analog.com/txdacs

Applying Nyquist's Criteria to Interpolating and Modulating DACs



Before starting the discussion on DACs in transmitters, it is important to expand upon a thought mentioned in a previous figure. Nyquist's criterion still applies regardless of interpolation or modulation!

The diagram labeled (A) shows the traditional case of data generated at a rate equal to f_{DATA} generating a signal having a bandwidth BW. Nyquist's criteria says that BW must be less than $f_{DATA}/2$ as shown.

The effects of digital interpolation and modulation are shown in (B). In addition to oversampling and interpolation, the spectrum of the signal has been shifted using digital modulation. Even so, the bandwidth of the signal is still BW—limited by the original Nyquist bandwidth, $f_{DATA}/2$.

It is also important to note that the maximum output frequency is limited by the rate at which the DAC is updated, f_{DAC}. Typically the maximum usable output frequency is approximately $f_{DAC}/3$, because of the non-ideal anti-imaging filter.

Although it is possible to use the higher images of the DAC output as the actual signal (the main baseband signal as well as the other images must be remove by filtering), the images suffer from attenuation due to the sin(x)/x rolloff, and may not provide sufficient amplitude to be usable. Therefore, this is not a popular approach.

In summary, the maximum bandwidth of the final DAC output signal is determined by one-half the input data rate, f_{DATA}, and the maximum IF output frequency by $f_{DAC}/2$.

For example, a 4× interpolating DAC which accepts input data at 250MSPS (f_{DATA} = 250MSPS) and outputs data at 1GSPS (f_{DAC} = 1GSPS) could reasonably reconstruct a signal having a bandwidth of 83MHz centered about an IF frequency of 300MHz.

Categories of DACs in the TxDAC® Family

- **Fast LVDS DACs: eg., AD9736 1.2GSPS, 14-bits, 2× interpolation**
  - **f_{DATA} (max) = f_{DAC} (max) = 1.2GSPS**
- **Interpolating DACs**
- **Dual DACs**
- **Dual Interpolating DAC with coarse digital modulation**
  - **f_{DATA} (max) = 250MSPS (CMOS), f_{DAC} (max) = 1GSPS, 2×, 4×, 8× interpolation**
- **Mixer DAC with on-chip digital quadrature modulator: AD9957**
  - **f_{DATA} (max) = 250MHz (CMOS), f_{DAC} (max) = 1.2GSPS, 4× to 252× interpolation (factors of 4 only)**
- ***http://www.analog.com/txdacs***

The TxDAC® family of CMOS DACs from Analog Devices has grown rapidly in the last 10 years. Early products in the family provided the basic DAC with very little added digital functionality. Smaller geometry CMOS processes have allowed the addition of a large number of digital features to the family.

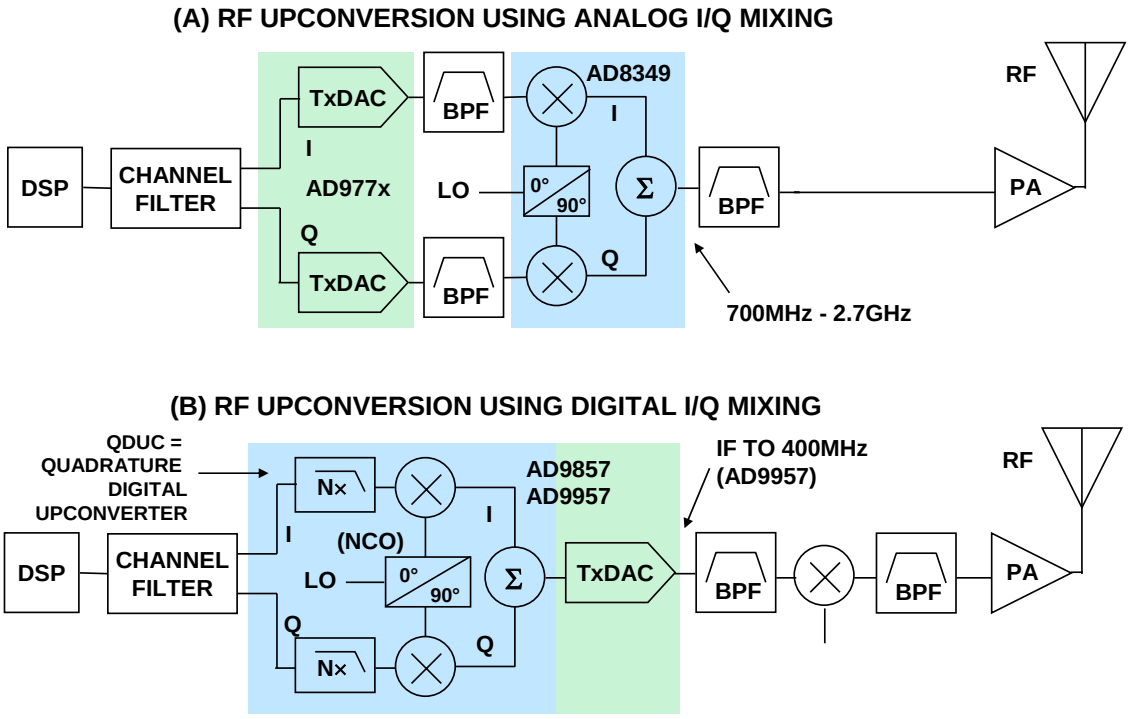
Modern members of the TxDAC family offer such important features as digital interpolation, modulation, dual DACs, and "mixer" DACs containing on-chip digital quadrature modulators.

The product family is currently too broad to do more than describe a few key new technology leading products and refer the reader to

http://www.analog.com/txdacs

For input data rates greater than about 250MSPS, LVDS receivers are utilized rather than traditional single-ended CMOS. For instance, the AD9736 accepts LVDS input data at a rate up to 1.2 GSPS. DACs such as these provide on-chip data alignment circuitry to ensure that input data is clocked at the proper time.

Two Popular Methods for RF Upconversion

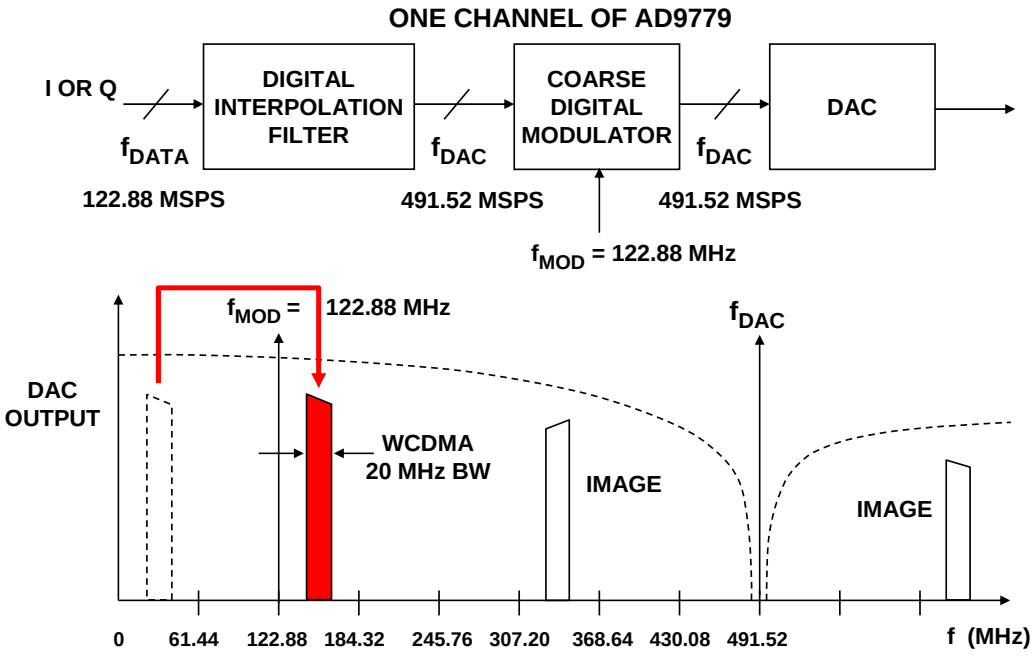


This figure shows two popular methods for performing RF upconversion in a digital transmitter. Traditional analog I/Q mixing is utilized in (A) using a dual DAC (AD977x) and an analog I/Q modulator (AD8349). The output of the quadrature modulator is at the RF frequency and is passed on to the power amplifier.

In (B) the digital I/Q data is passed through a quadrature digital upconverter (QDUC) such as the AD9857 (200MHz) or AD9957 (400MHz) and then to a single on-chip DAC which provides an IF frequency output (up to 400MHz for the AD9957). The IF frequency then passes through a final stage of upconversion using traditional analog techniques. Devices such as the AD9857/AD9957 are commonly referred to as "mixer" DACs.

Both techniques are currently being used in transmitters. Analog I/Q mixing produces the RF signal directly. Digital I/Q mixing requires an additional upconversion stage, but eliminates the need for an analog I/Q mixer.

AD9779 Multicarrier WCDMA Signal, 4× Interpolation, f_{DATA} = 122.88 MSPS, f_{DAC}/4 Modulation

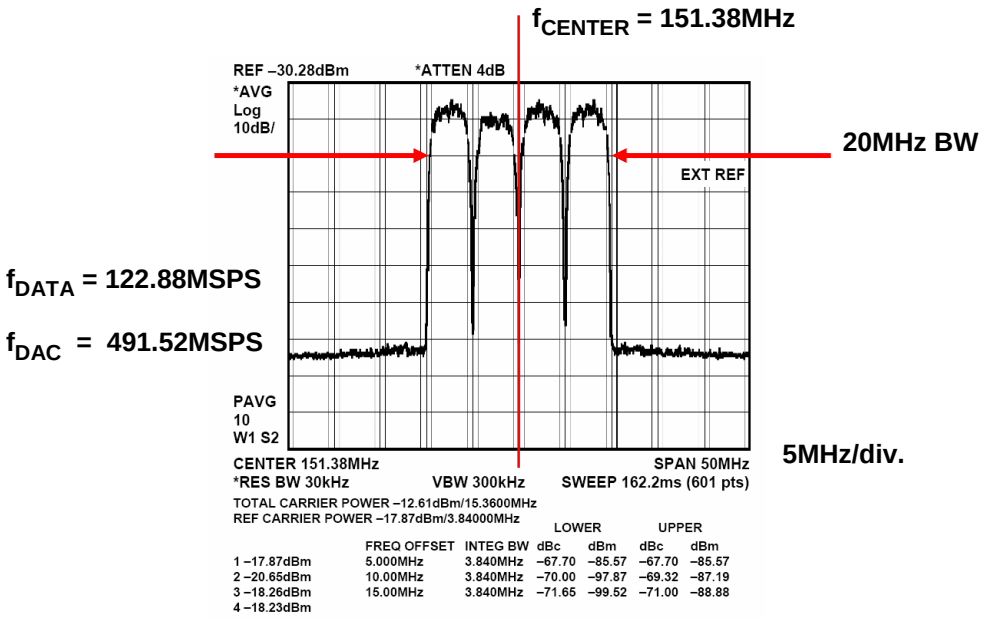


The addition of a digital modulator to an interpolating DAC allows the baseband output IF signal to be positioned in the desired Nyquist zone. In this case, the AD9779 16-bit DAC input data rate is 122.88MSPS. The signal bandwidth is 20MHz which corresponds to a wideband CDMA multicarrier signal (WCDMA) The digital interpolation filter then increases the data rate by 4× to 491.52MSPS.

The on-chip coarse digital modulator in the AD9779 then serves to place the WCDMA signal in the third Nyquist zone referenced to the input data rate.

The AD9776/AD9778/AD9779 are dual 12/14/16-bit DACs capable of output data rates up to 1GSPS with input data rates to 250MSPS.

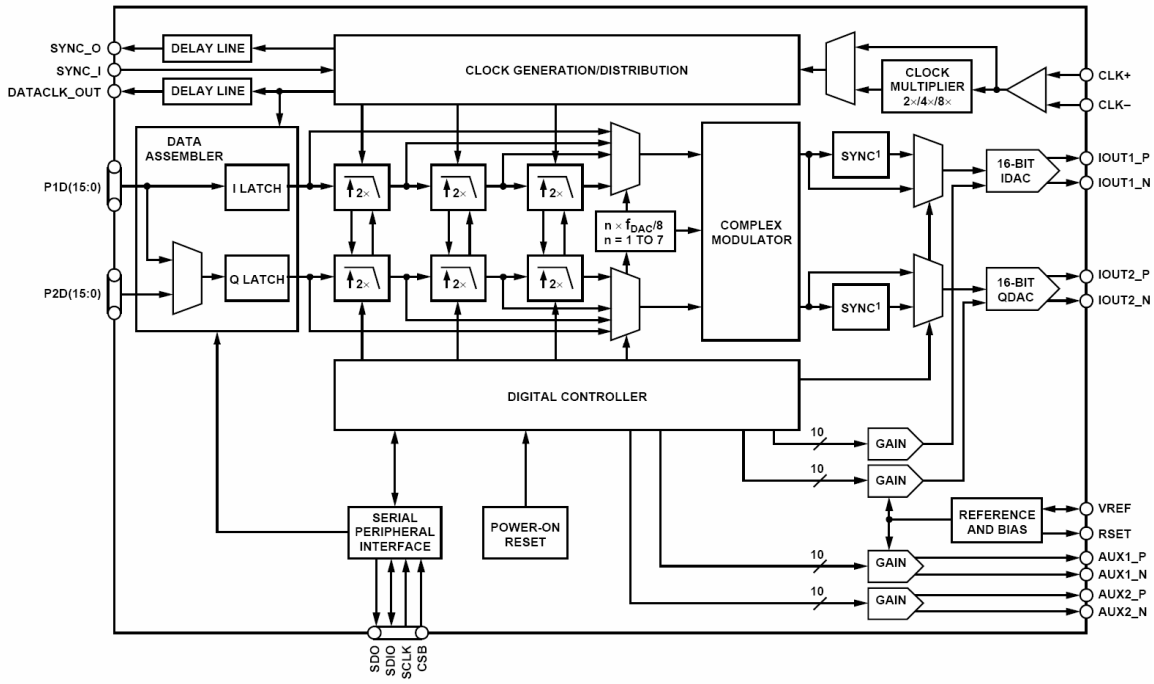
AD9779 Multicarrier WCDMA Signal, 4× Interpolation, f_{DATA} = 122.88 MSPS, f_{DAC}/4 Modulation



This figure shows the actual analog output of the AD9779 reconstructing a WCDMA signal with an input data rate of 122.88MSPS, and an output data rate of 491.52MSPS. The digital modulator is used to position the signal in the third Nyquist zone referenced to the input data rate.

A functional diagram of the AD9779 family is shown in the next figure.

AD9776/AD9778/AD9779 12/14/16-Bit Dual 1GSPS DACs

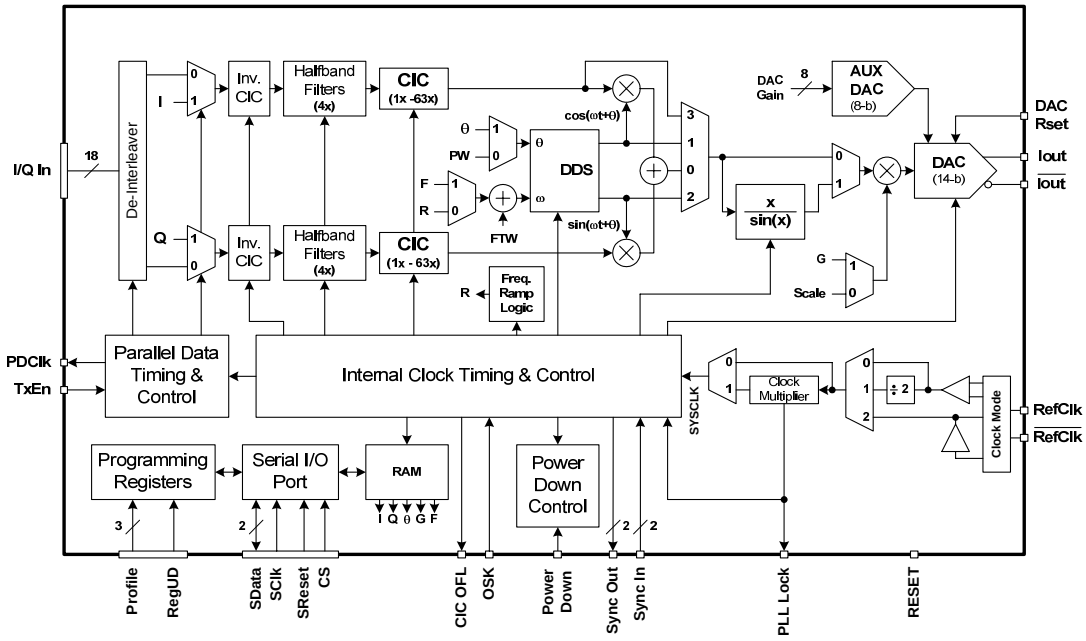


The AD9776/AD9778/AD9779 are dual, 12-/14-/16-bit, high dynamic range DACs that provide an interpolated sample rate of 1 GSPS, thus permitting multicarrier signal generation up to high IF frequencies. As previously discussed, they include features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators, such as the AD8349.

A serial peripheral interface (SPI) provides for programming/readback of many internal parameters. The output current can be programmed over a range of 10mA to 30mA. The devices are manufactured on an advanced 0.18µm CMOS process and operate from 1.8V and 3.3V supplies for a total power consumption of 1.0W. They are enclosed in 100-lead TQFP packages.

The devices provide an SFDR of 78dBc for output frequencies up to 100MHz and have a single carrier WCDMA adjacent channel leakage ratio (ACLR) = 79 dBc @ 80MHz IF.

AD9957 1 GSPS Quadrature Digital Upconverter (QDUC) "Mixer" DAC



The AD9957 is a 1GSPS quadrature digital upconverter capable of generating IF frequencies up to 400MHz. Input data can be accepted on an 18-bit parallel I/Q port at a rate up to 250MHz. The AD9957 allows interpolation rates from 4× to 252×.

The on-chip numerically controlled oscillator (NCO) uses a 32-bit frequency tuning word.

An auxiliary DAC is also included which can be used to provide some on-ramping to the output power of the DAC without sacrificing any of the dynamic range.

The AD9957 is packaged in a 100-lead TQFP.

The following reference describes the details of the operation of the AD9857, the 200MHz predecessor of the AD9957. The parts share many similar operational characteristics.

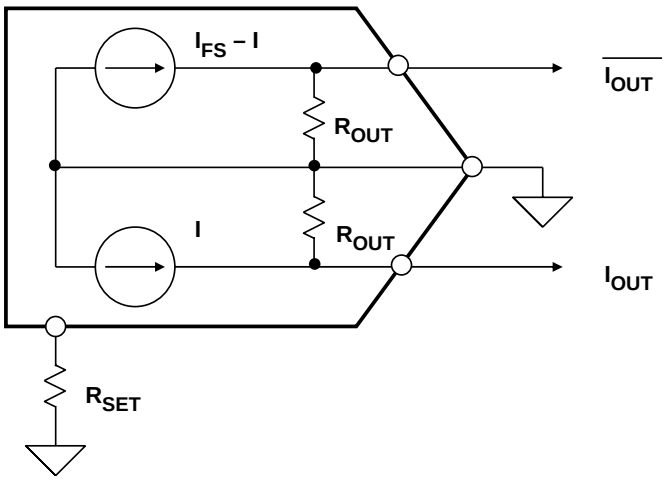
---

1. Ken Gentile, "Digital Upconverter IC Tames Complex Modulation," *Microwaves and RF*, August 2000.

Buffering DAC Outputs

www.analog.com/txdacs
www.analog.com/amps
www.analog.com/diffamps

Generalized Model of a High Speed CMOS DAC Output such as the AD978x and AD977x Series



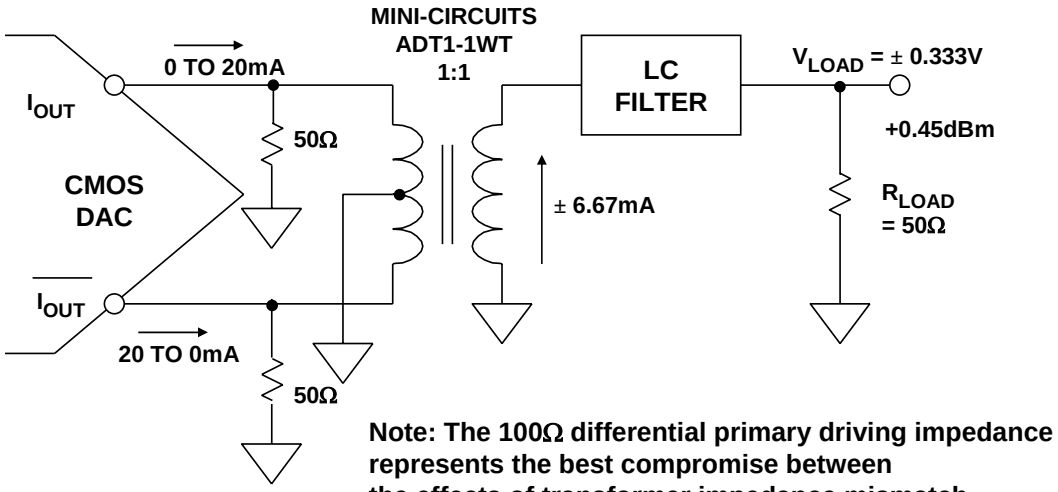
- I_{FS} 2 - 20mA typical
- R_{OUT} > 100kΩ
- Output compliance voltage < ±1V for best performance

Now, we will look at some issues relating to high-speed DAC outputs. This figure shows the equivalent output circuit for the Analog Devices' CMOS TxDAC family.

Outputs are differential currents which can be set from 2 to 20mA FS by an external RSET resistor.

Output impedance is greater than 100kΩ, and the output compliance voltage is ±1V. Best performance in terms of SNR and SFDR is generally obtained with an output voltage between 0.5V p-p and 1V p-p (10mA to 20mA into 50Ω. The next few figures show typical output circuits.

Differential Transformer Coupling



Note: The 100Ω differential primary driving impedance represents the best compromise between the effects of transformer impedance mismatch and DAC SNR performance.

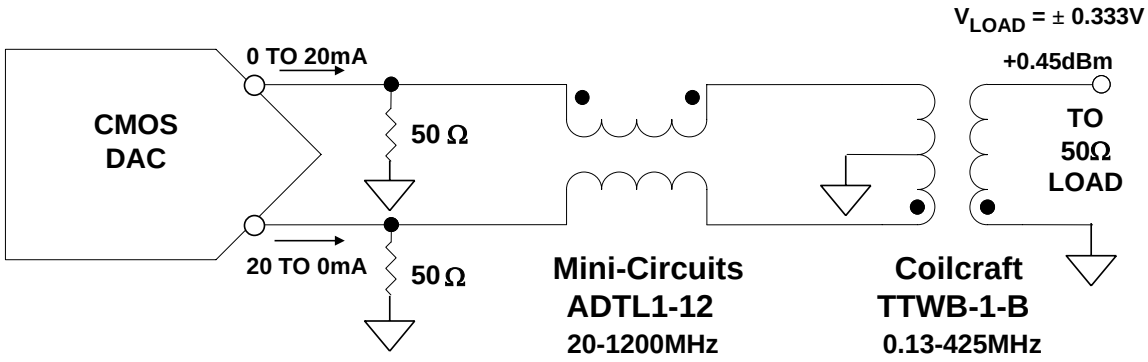
In this application, the differential outputs are configured to drive the primary winding of a transformer. This converts the differential output signal into a single-ended signal.

Note that the 100Ω primary driving impedance was chosen in order to optimize the DAC SNR and SFDR. The resulting impedance mismatch does not significantly affect the performance of the transformer.

The secondary winding single-ended load is 50Ω. This is reflected back to the primary as a 25Ω load on each of the differential DAC outputs. The effective dc load on each DAC output is therefore 50Ω||25Ω = 16.7Ω.

The resulting single-ended output signal level is ±333mV p-p into a 50Ω load, which is +0.45dBm.

Transformer Coupling out of the AD9786 on Evaluation Board

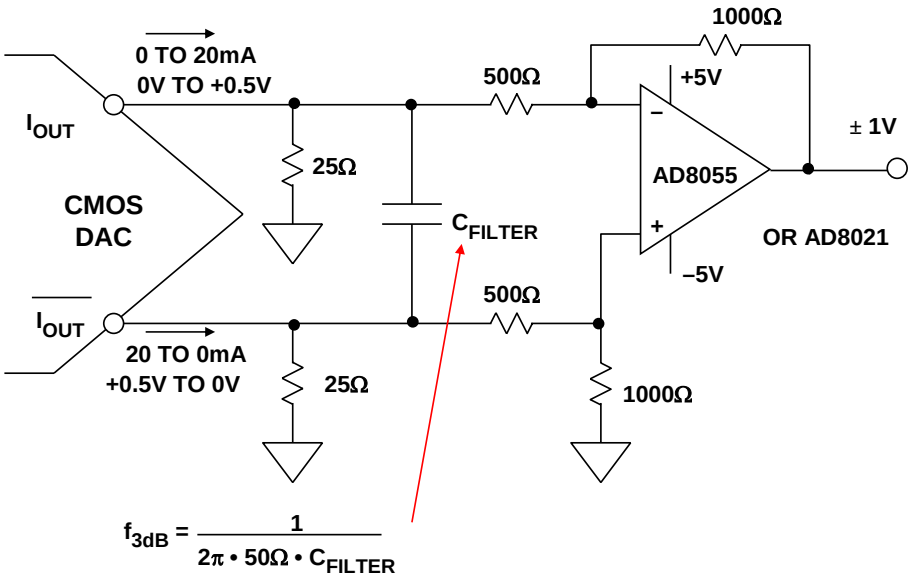


- **Transmission Line Transformer in series with outputs to help cancel HD2**
- **RF Transformer from Coilcraft (TTWB-1-B) shows better performance for IFs at 200-300 MHz**

In order to obtain the best possible second harmonic distortion performance at high IF frequencies (generally > 100MHz), a double transformer output can be used as shown in this figure. The double transformer configuration helps eliminate the unbalance caused by the parasitic capacitance between the primary and secondary windings of the transformers.

In some cases, equivalent performance can be achieved with a more expensive single high performance transformer. In any case, some experimentation may be required to achieve optimum results in demanding applications.

Differential DC Coupling Using a Dual-Supply Op Amp



The output current drive for most members of the TxDAC family can be set for up to 20mA with an external resistor. In most applications this results in sufficient load power so that additional output buffering is not required.

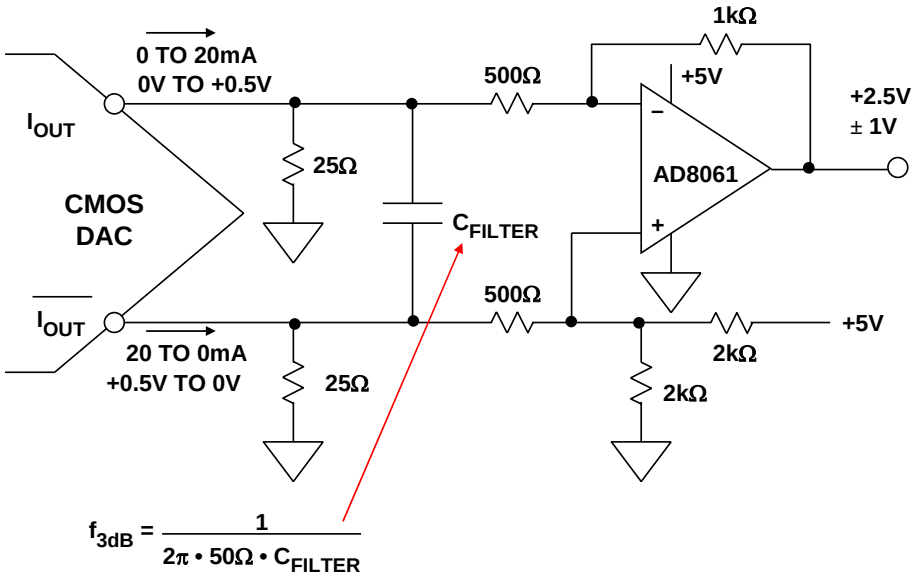
For applications which do require an output buffer, a high speed op amp can be used to perform the differential to single-ended conversion as shown in this figure.

Note that the op amp is not used directly as an I/V converter, but is configured as a "difference" amplifier to amplify the voltage developed across the 25Ω load resistors. The amplifier gain is set for a factor of 2 which develops a final output voltage of 2V p-p. Since the output swings above and below ground, a dual-supply op amp is required.

The C_{FILTER} capacitor forms a differential filter with the equivalent 50Ω differential output load. This filter reduces any slew-induced distortion of the op amp as well as broadband noise, and the optimum cutoff frequency of the filter is determined empirically to give the best tradeoff between SFDR and SNR while maintaining the required bandwidth.

The op amp must be carefully selected such that it meets the overall system noise and distortion requirements. In some cases at high IF frequencies, the optimum performance can only be achieved with a transformer output driver as previously discussed.

Differential DC Coupling with a Single-Supply Op Amp



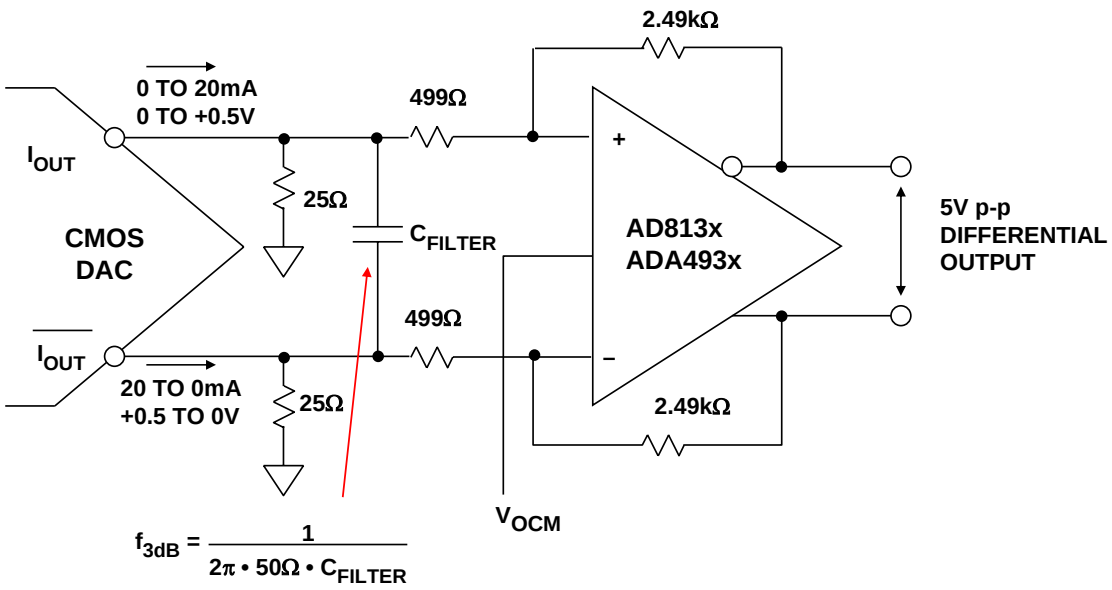
A modified form of the the circuit in the previous figure can be operated on a single supply, provided the common-mode voltage of the op amp is set to mid-supply (+2.5V). This is shown here, where the AD8061 op amp is used.

The input common-mode voltage of the AD8061 is –0.2V to +3.2V when operating on a +5V supply. The output common-mode range is 0.3V to +4.5V when the output is terminated with a 150Ω resistor connected to mid-supply.

The output voltage of the circuit is 2V p-p centered around a common-mode voltage of +2.5V. This common-mode voltage is developed from the +5V supply using a resistor divider, and the supply must be heavily decoupled to prevent amplification of the power supply noise.

An alternative is to eliminate the 2kΩ resistor voltage divider completely and connect the non-inverting input of the op amp to a 2.5V voltage reference through a 1kΩ resistor.

Buffering High-Speed DAC Outputs Using the AD813x or ADA493x Differential Op Amps



If a buffered differential voltage output is required from a current output TxDAC, the AD813x- or ADA493x-series of differential amplifiers can be used as shown here.

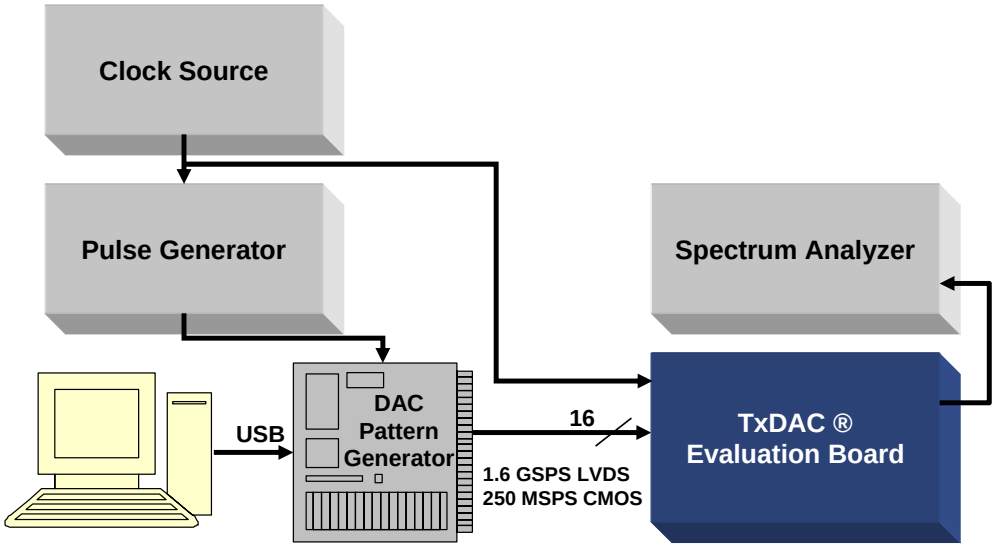
The DAC output current is first converted into a voltage that is developed across the 25Ω resistors. The voltage is amplified by a factor of 5 using the AD813x. This technique is used in lieu of a direct I/V conversion to prevent fast slewing DAC currents from overloading the amplifier and introducing distortion.

The V_{OCM} input on the AD813x can be used to set a final output common-mode voltage within the range of the AD813x. Adding a pair of series output resistors will allow transmission lines to be driven.

As a final note of caution regarding DAC output amplifier buffers, it is extremely important to carefully select the amplifier based on the bandwidth, noise, and distortion requirements of the system. At high IF frequencies, the only acceptable solution may be to either use the DAC current outputs directly or use a suitable RF transformer.

DAC Evaluation Hardware and Software

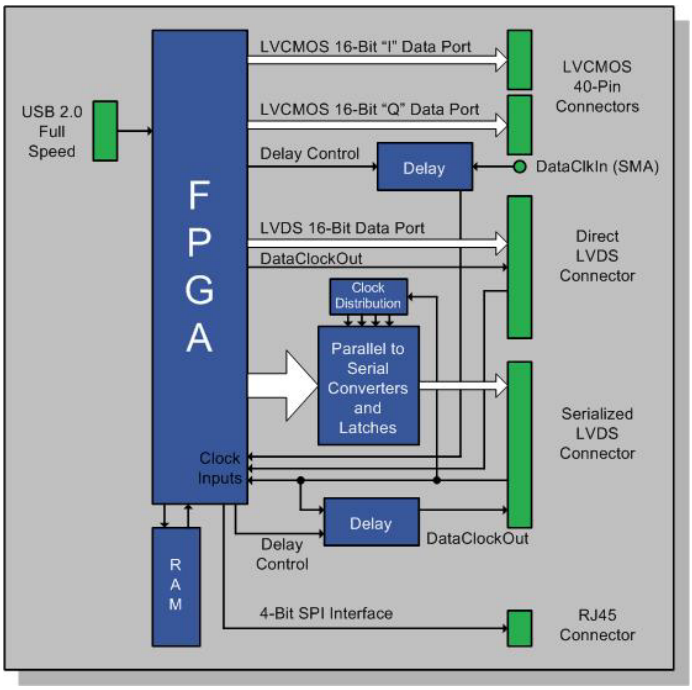
www.analog.com/txdacs



This figure shows a typical test setup for measuring the distortion and noise of a DAC. The first consideration, of course, is the generation of the digital signal to drive the DAC. To achieve this, modern arbitrary waveform generators (for example, Tektronix AWG2021 with Option 4) or word generators (Tektronix DG2020) allow almost any waveform to be synthesized digitally in software, and are mandatory in serious frequency domain testing of DACs. In most cases, these generators have standard waveforms pre-programmed, such as sinewaves and triangle waves, for example. In many communications applications, however, more complex digital waveforms are required, such as two-tone or multi-tone sinewaves, QAM, GSM, and CDMA test signals, etc. In many cases, application-specific hardware and software exists for generating these types of signals and can greatly speed up the evaluation process. Analog Devices offers a DAC Pattern Generator which will be described shortly.

The spectrum analyzer chosen to measure the distortion and noise performance of the DAC should have at least 10dB more dynamic range than the DAC being tested. The "maximum intermodulation-free range" specification of the spectrum analyzer is an excellent indicator of distortion performance. However, spectrum analyzer manufacturers may specify distortion performance in other ways. Modern communications DACs such as the TxDAC®-series require high performance spectrum analyzers such as the Rhode and Schwartz FSEA30. As in the case of oscilloscopes, the spectrum analyzer must not be sensitive to overdrive. This can be easily verified by applying a signal corresponding to the full-scale DAC output, measuring the level of the harmonic distortion products, and then attenuating the signal by 6dB or so and verifying that both the signal and the harmonics drop by the same amount. If the harmonics drop more than the fundamental signal drops, then the analyzer is distorting the signal. In some cases, an analyzer with less than optimum overdrive performance can still be used by placing a bandstop filter in series with the analyzer input to remove the frequency of the fundamental signal being measured. The analyzer looks only at the remaining distortion products. This technique will generally work satisfactorily, provided the attenuation of the bandstop filter is taken into account when making the distortion measurements. Obviously, a separate bandstop filter is required for each individual output frequency tested, and therefore multi-tone testing is cumbersome.

High Speed DAC Pattern Generator (DPG)



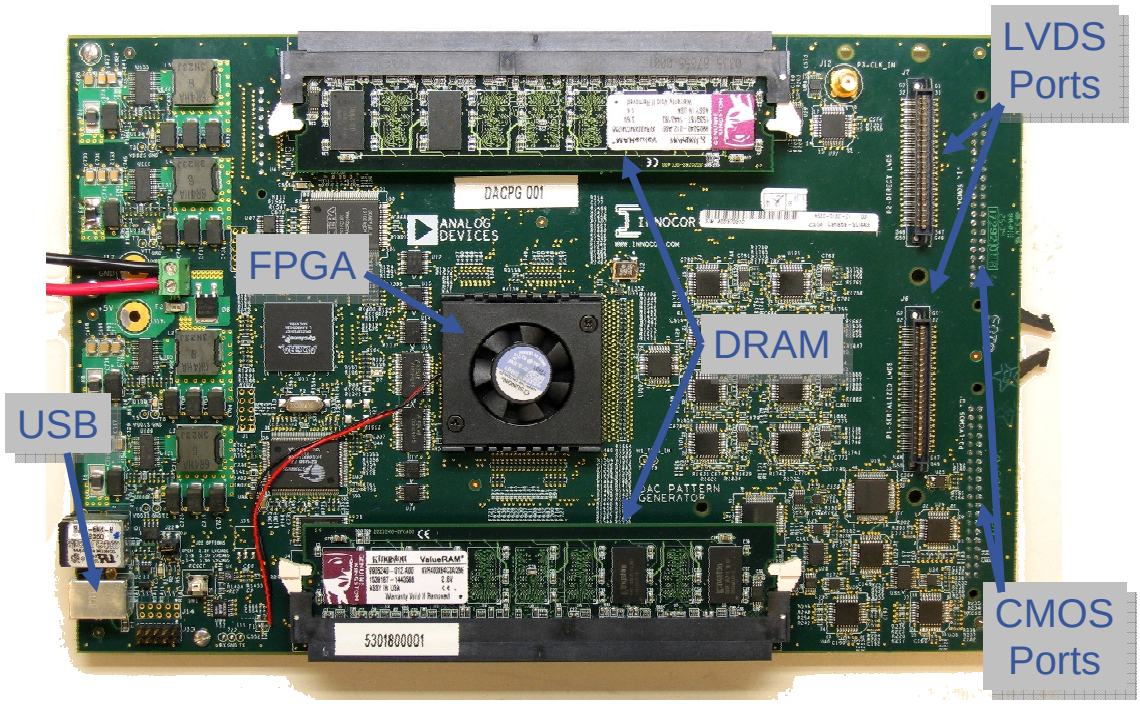
- **Provides high-speed digital data to ADI's DAC Evaluation Boards**
- **CMOS and LVDS data formats supported**
- **Up to 1.6 GSPS in LVDS mode, 250 MSPS in CMOS mode**
- **512 MB RAM for complex waveform generation**

The Analog Devices high speed DAC Pattern Generator (DPG) provides high speed digital data to ADI's DAC evaluation boards. Both CMOS and LVDS data formats are supported.

The board can output data at a rate up to 1.6GSPS in the LVDS mode and 250MSPS in the CMOS mode.

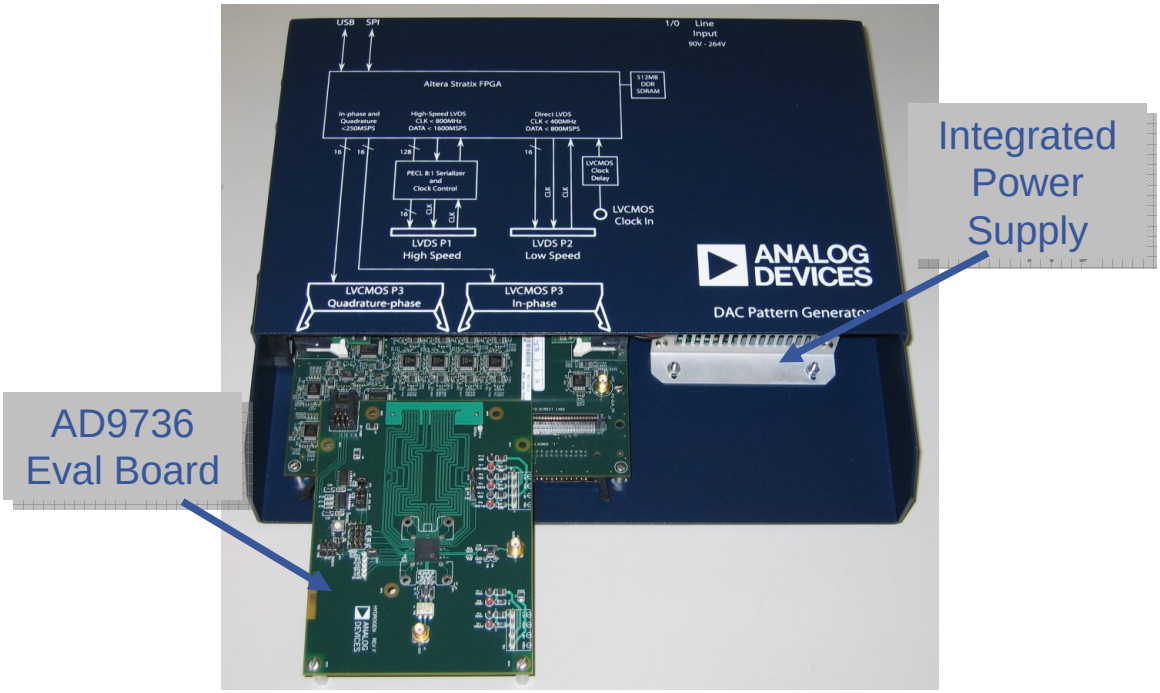
There is 512MB of on-board RAM for complex waveform generation.

High Speed DAC Pattern Generator (DPG)



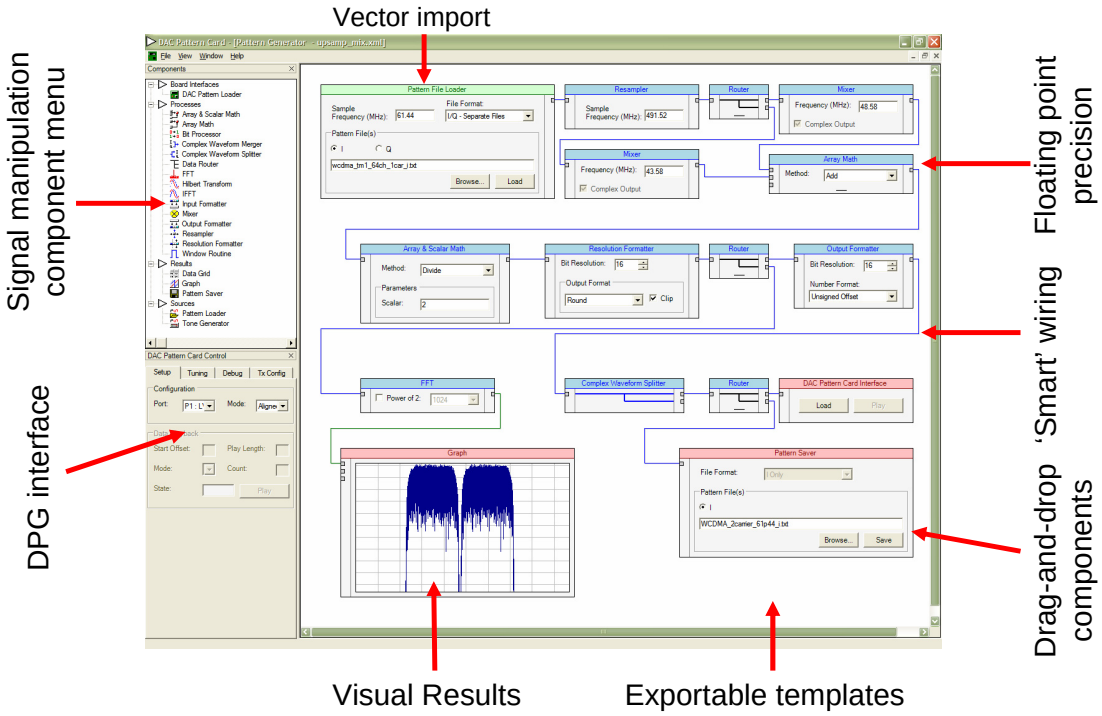
This figure shows a photograph of the DAC Pattern Generator (DPG) board. Note the locations of the USB, LVDS, and CMOS data ports. The DPG interfaces to the PC via a standard USB port.

High Speed DAC Pattern Generator (DPG)



The DAC Pattern Generator board is designed to interface with the individual TxDAC evaluation boards as shown here for the AD9736. The DPG is shown here with an integrated power supply.

VisualDAC™

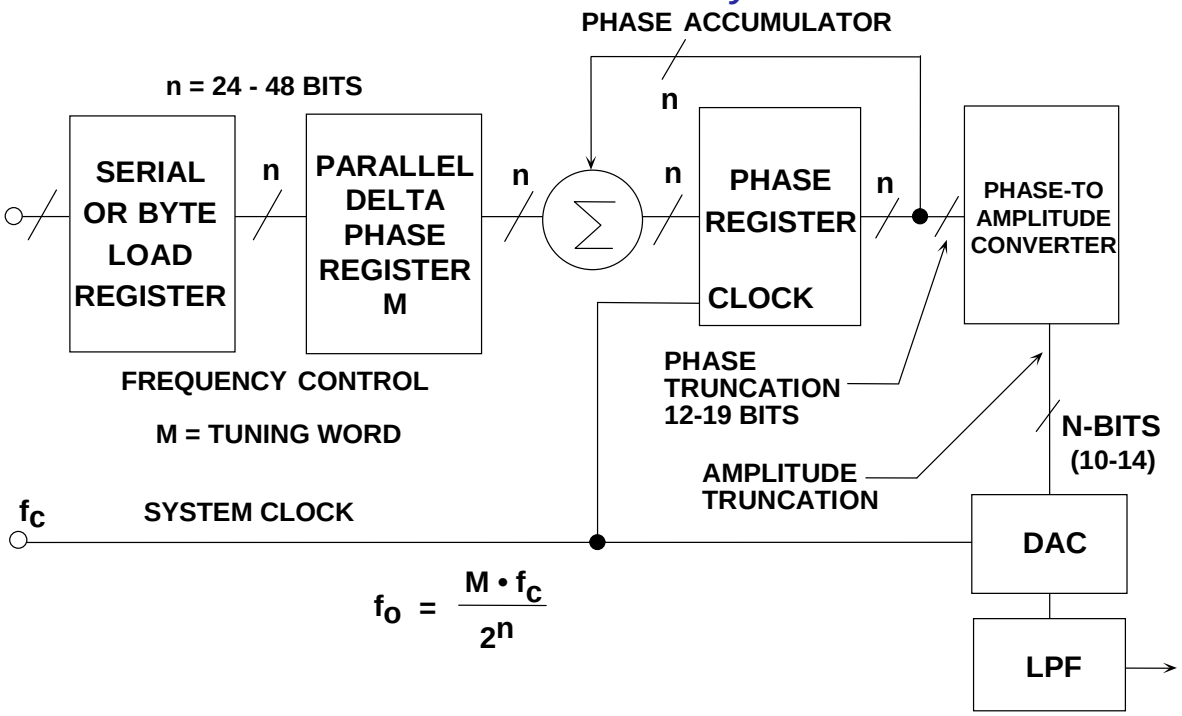


The DPG board is operated using VisualDAC™ software which is a graphical user interface as shown in this figure. The software is used to generate the various complex waveforms required to test the TxDAC series.

Direct Digital Synthesis

www.analog.com/dds

A Flexible DDS System

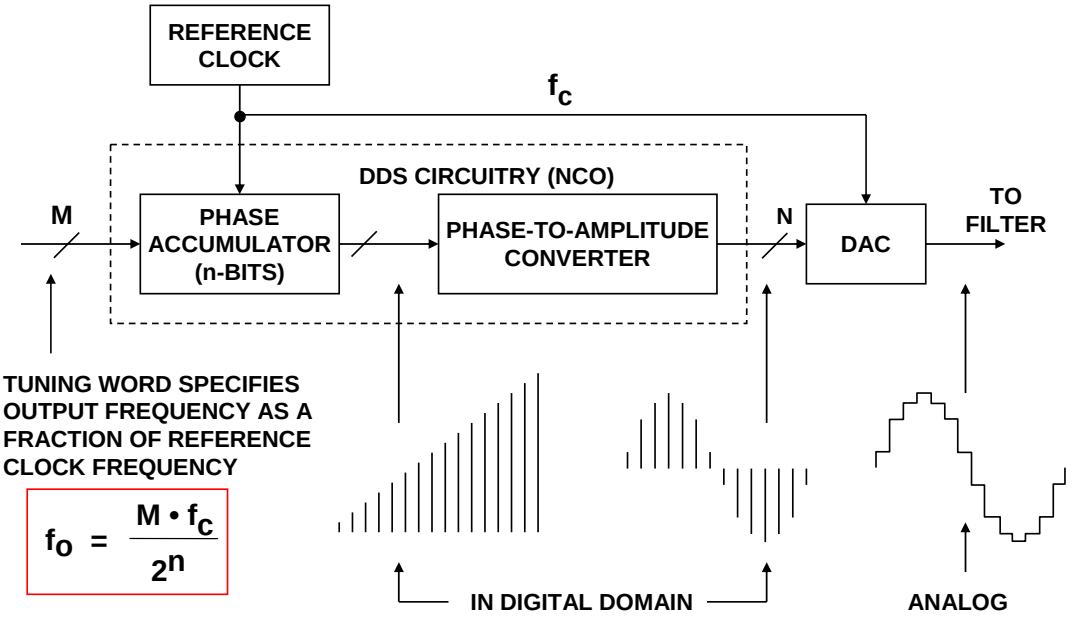


The heart of the DDS system is the phase accumulator whose contents are updated once each clock cycle. Each time the phase accumulator is updated, the digital number, M, stored in the delta phase register is added to the number in the phase accumulator register. Assume that the number in the delta phase register is 00...01 and that the initial contents of the phase accumulator is 00...00. The phase accumulator is updated by 00...01 on each clock cycle. If the accumulator is 32-bits wide, 232 clock cycles (over 4 billion) are required before the phase accumulator returns to 00...00, and the cycle repeats.

The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each address in the lookup table corresponds to a phase point on the sinewave from 0° to 360°. The lookup table contains the corresponding digital amplitude information for one complete cycle of a sinewave. The lookup table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives the DAC. In practice, only data for 90° is required because the quadrature data is contained in the two MSBs. In order to further reduce the size of the lookup tables, various proprietary algorithms have been developed to compute the sine values, however, the fundamental concept is still the same.

For an n-bit phase accumulator (n generally ranges from 24 to 32 in most DDS systems), there are 2^n possible phase points. The digital word in the delta phase register, M, represents the amount the phase accumulator is incremented each clock cycle. If f_c is the clock frequency, then the frequency of the output sinewave is equal to $Mf_c/2^n$. This equation is known as the DDS "tuning equation." Note that the frequency resolution of the system is equal to $f_c/2^n$. For n = 32, the resolution is greater than one part in four billion! In a practical DDS system, all the bits out of the phase accumulator are not passed on to the lookup table, but are truncated, thereby reducing the size of the lookup table without affecting frequency resolution. The amount of truncation depends upon the resolution and performance of the output DAC. In general, the phase address information should have two to four bits more resolution than the DAC, but this can vary some from product to product. The objective is to use enough resolution in the lookup table address so that the overall noise and distortion of the analog output signal is limited by the DAC and not the effects of phase truncation.

Signal Flow Through the DDS Architecture



This figure shows the signal flow through the DDS architecture. The phase accumulator is actually a modulus M counter that increments its stored number each time it receives a clock pulse. The magnitude of the increment is determined by the binary input number or word (M) contained in the delta phase register that is summed with the overflow of the counter. The digital phase information from the phase accumulator is converted into a corresponding digital amplitude by the phase-to-amplitude converter. Finally, the DAC converts the digital amplitude into a corresponding analog signal.

The DDS architecture allows the frequency to be changed instantaneously by simply changing the tuning word M. There is no phase hit when the frequency is changed, thereby making the DDS approach ideal for frequency hopping applications.

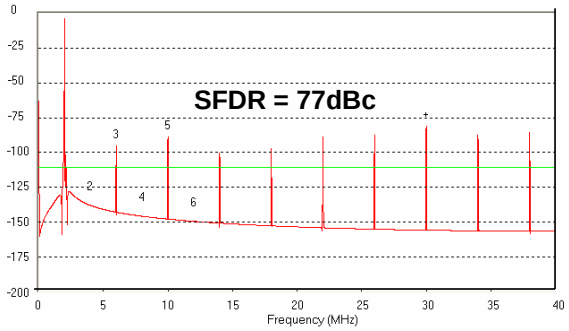
When IC DDS systems became popular in the mid 1980s, the digital NCO was generally fabricated on a CMOS process, and the high speed DAC on a bipolar process, thereby yielding a two-chip solution. Today, however, modern CMOS processes are suitable for not only the digital circuits but for the high performance DAC as well (as illustrated by the many TxDACs currently offered by Analog Devices). Modern DDS systems therefore are fully integrated and include many additional options as well.

The following article is an excellent reference on DDS operation, especially the analysis of output spurious components.

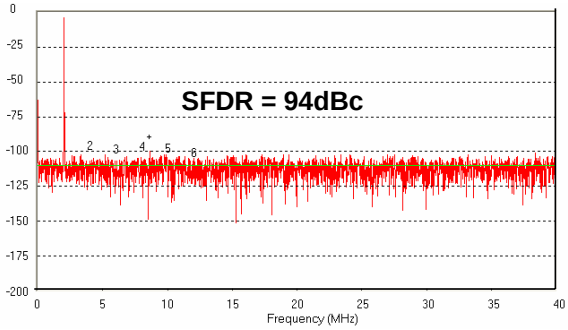
David Brandon, "DDS Design," *EDN*, May 13, 2004, pp. 71-84.

Effect of Ratio of Sampling Clock to Output Frequency on SFDR for Ideal 12-bit DAC

(A) f_{OUT} = 2.0000 MHz, f_S = 80.0000 MHz



(B) f_{OUT} = 2.0111 MHz, f_S = 80.0000 MHz



FFT SIZE = 8192
THEORETICAL 12-BIT SNR = 74dB
FFT PROCESS GAIN = 36dB
FFT NOISE FLOOR = 110dBFS

In DDS systems it is important to utilize frequency planning so that the output frequency is not an exact submultiple of the clock frequency. This can be demonstrated using the ADIsimADC program and the ideal 12-bit ADC model. Note that the same effect occurs in ADCs as well as DACs. In ADC applications, however, the noise on the input signal tends to mask the effect somewhat, although it can still be observed.

In (A), the clock frequency is 80.0000MHz, and the output frequency is 2.0000MHz (an exact ratio of 40). Note that the quantization noise is concentrated at harmonics of the fundamental frequency. This limits the SFDR to approximately 77dBc, even though the calculated SNR is still 74dB.

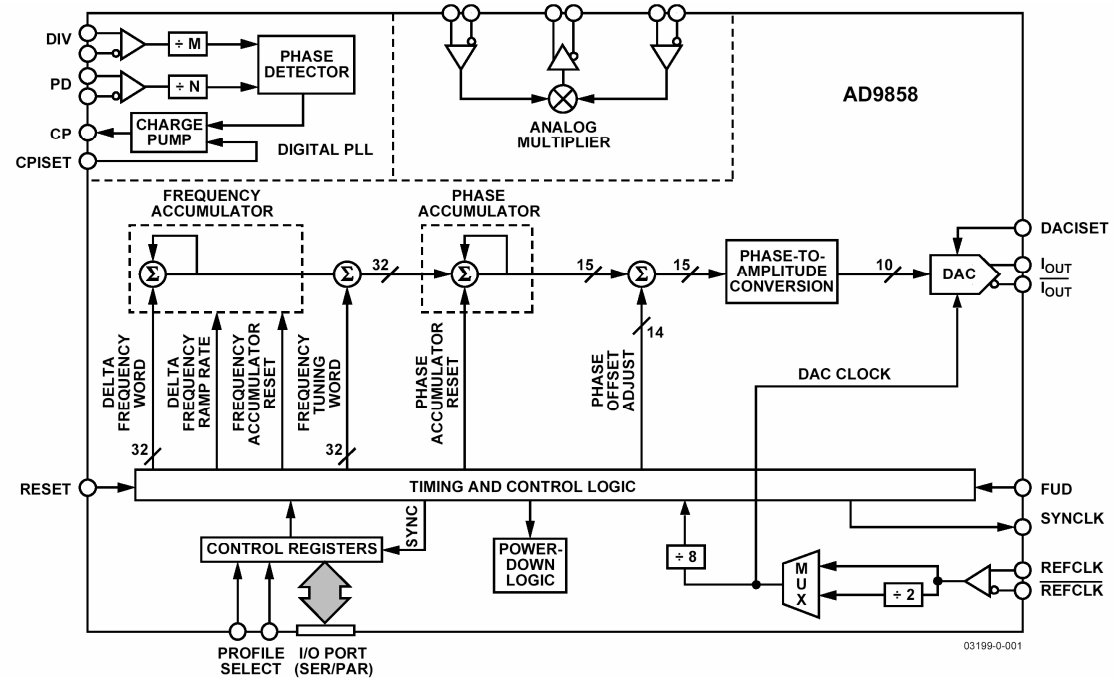
In (B), the output frequency is changed to 2.0111MHz. Now, the quantization noise is spread more or less uniformly over the entire Nyquist bandwidth. The SFDR is approximately 94dBc (just slightly above the FFT noise floor of 110dBFS—averaging a number of FFTs will cause the SFDR to approach the noise floor even closer).

Note that for each bit added to the ideal DAC, the above numbers increase by approximately 6dB.

This effect can be largely avoided by careful selection of clock and output frequencies in systems using DDS.

Recent DDS technology (SpurKiller) which will be discussed later helps ease the frequency planning imposed constraints by the targeted reduction of specific spurs.

AD9858 1GSPS DDS with Phase Detector and Analog Multiplier



This figure shows a block diagram of one of Analog Devices' recent DDS ICs. The AD9858 is a direct digital synthesizer (DDS) featuring a 10-bit DAC operating up to 1GSPS. The AD9858 uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sine wave at up to 400MHz.

The AD9858 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9858 via parallel (8-bit) or serial loading formats. The AD9858 contains an integrated charge pump (CP) and phase frequency detector (PFD) for synthesis applications requiring the combination of a high speed DDS along with phase-locked loop (PLL) functions.

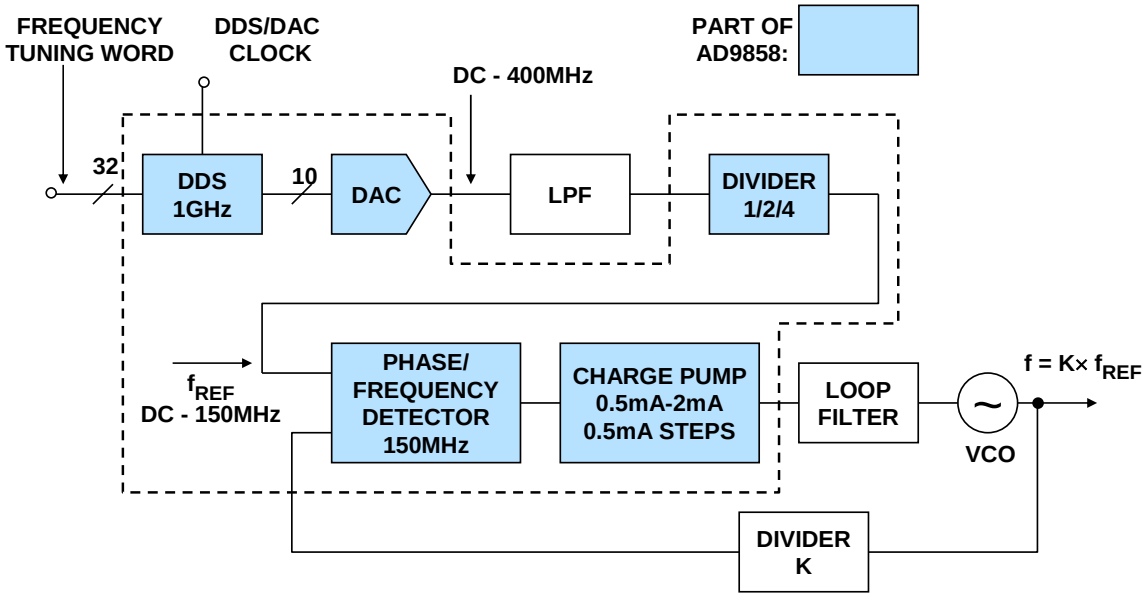
Another benefit of the DDS approach to frequency synthesis is the ability to very accurately and reliably inject phase offsets. 14 bits of phase control allow fine adjustments to ~0.022 degrees as well as supporting phase hopping in the same way that frequency hopping is supported.

Note that a second accumulator has been included in the DDS architecture. Shown here specifically driving the frequency tuning word, this enables a very easy and well controlled method for sweeping across a range of frequencies rather than hold at, or jumping between specific frequencies. The newest DDS chips allow the second accumulator to drive the phase and amplitude control functions of the DDS as well, so that either of these may be swept instead of the frequency.

An analog mixer is also provided on-chip for applications requiring the combination of a DDS, PLL, and mixer, such as frequency translation loops, tuners, and so on. The AD9858 also features a divide-by-two on the clock input, allowing the external clock to be as high as 2 GHz.

The AD9858 is specified to operate over the extended industrial temperature range of –40°C to +85°C.

DDS Single Loop Upconversion Using the AD9858

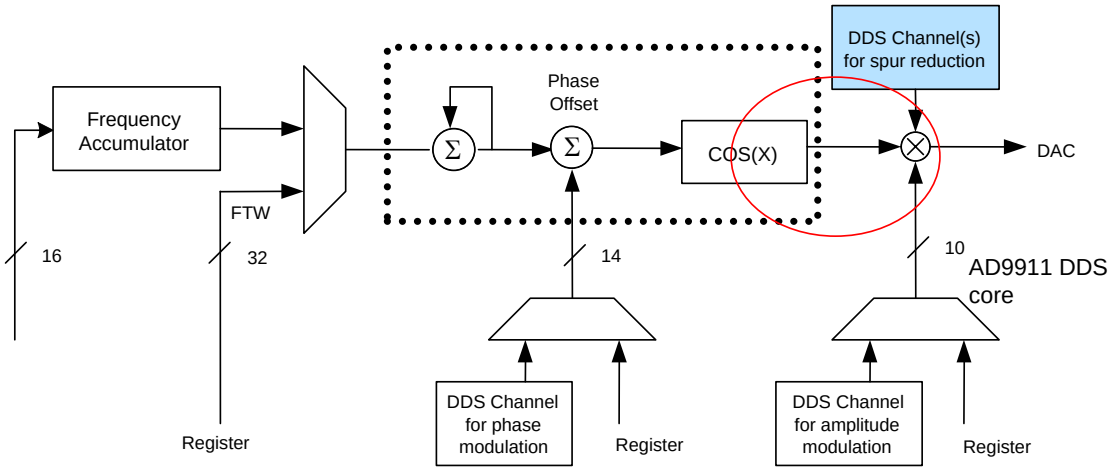


This figure shows the AD9858 configured as an upconverter using the internal phase detector and charge pump along with external filtering and a VCO to form a high-speed PLL.

The basic AD9858 DDS can generate a frequency up to 400MHz. The PLL circuitry, in conjunction with a high frequency VCO and divider, is capable of multiplying the reference frequency well up into the GHz region. The reference frequency into the phase detector can be as high as 150MHz.

SpurKiller Technology

- **Use an auxiliary DDS channel to add in a signal at the same frequency and amplitude as the spur, but 180° out of phase with the highest spur…**



The frequencies at which spurs appear in a DDS output spectrum are simple functions of the sampling rate and the programmed output frequency and are therefore predictable. In addition, they are fairly repeatable from device to device (assuming the same sampling rate and output frequency). In addition, the relative phase of each spur does not change.

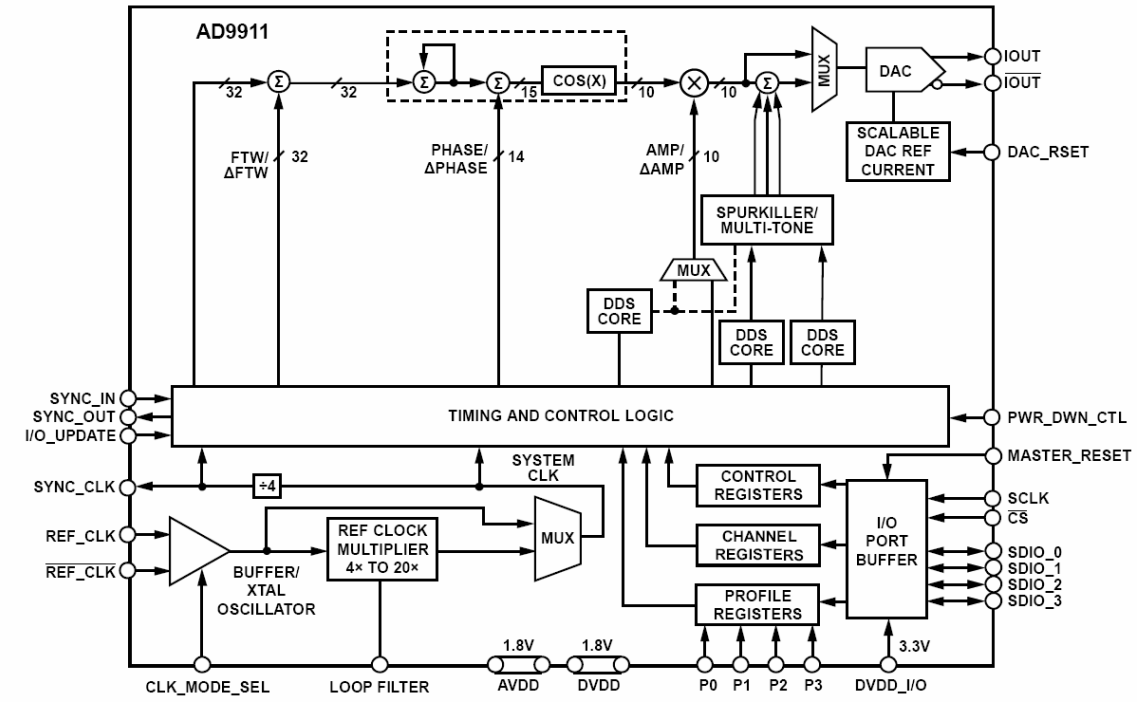
The amplitude of the spur does change somewhat over temperature and with supply voltage as well as process variation.

The Analog Devices' SpurKiller technology uses an auxilary DDS channel to add in a signal at the same frequency and amplitude as the worst spur, but 180° out of phase. In effect, this removes most of the spur from the output spectrum.

This figure shows the basic concept used in the first SpurKiller DDS, the AD9911. The auxiliary DDS spur reduction channel is shaded in the figure.

The AD9911 is described in more detail in the next figure.

AD9911 SpurKiller 500MHz DDS



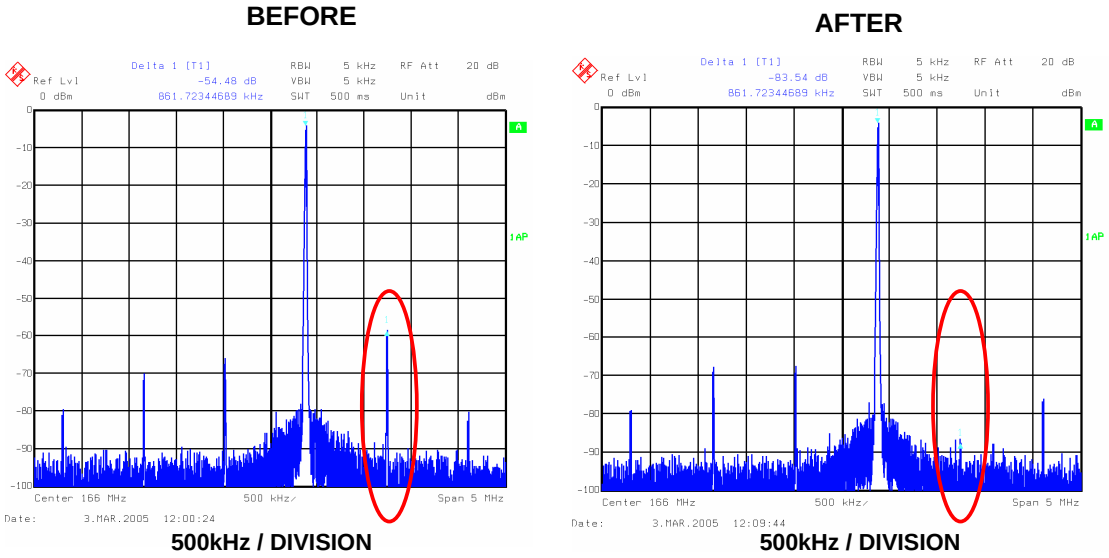
The AD9911 is a complete direct digital synthesizer (DDS) that operates up to 500MSPS. This device includes a high speed DAC with excellent wideband and narrowband spurious-free dynamic range (SFDR) as well as three auxiliary DDS cores without assigned digital-to-analog converters (DACs). These auxiliary channels are used for spur reduction, multitone generation, or test-tone modulation.

The AD9911 is the first DDS to incorporate SpurKiller technology and multitone generation capability. Multitone mode enables the generation up to four concurrent carriers; frequency, phase, and amplitude can be independently programmed. Multitone generation can be used for system tests, such as inter-modulation distortion and receiver blocker sensitivity. SpurKilling enables customers to improve SFDR performance by reducing the magnitude of harmonic components and/or the aliases of those harmonic components.

Test-tone modulation efficiently enables sine wave modulation of amplitude on the output signal using one of the auxiliary DDS cores.

The AD9911 can perform modulation of frequency, phase, or amplitude (FSK, PSK, ASK). Modulation is implemented by storing profiles in the register bank and applying data to the profile pins. In addition, the AD9911 supports linear sweep of frequency, phase, or amplitude for applications such as radar and instrumentation.

The Results of Using SpurKiller Technology on a DDS Output Spur



OUTPUT FREQUENCY = 166MHz

This figure shows the AD9911 DDS output spectrum before and after applying the SpurKiller technique. The output frequency is 166MHz, and the update rate is 500MHz. The worst spur is highlighted and appears approximately 60dB below fullscale.

The basic SpurKiller procedure is as follows:

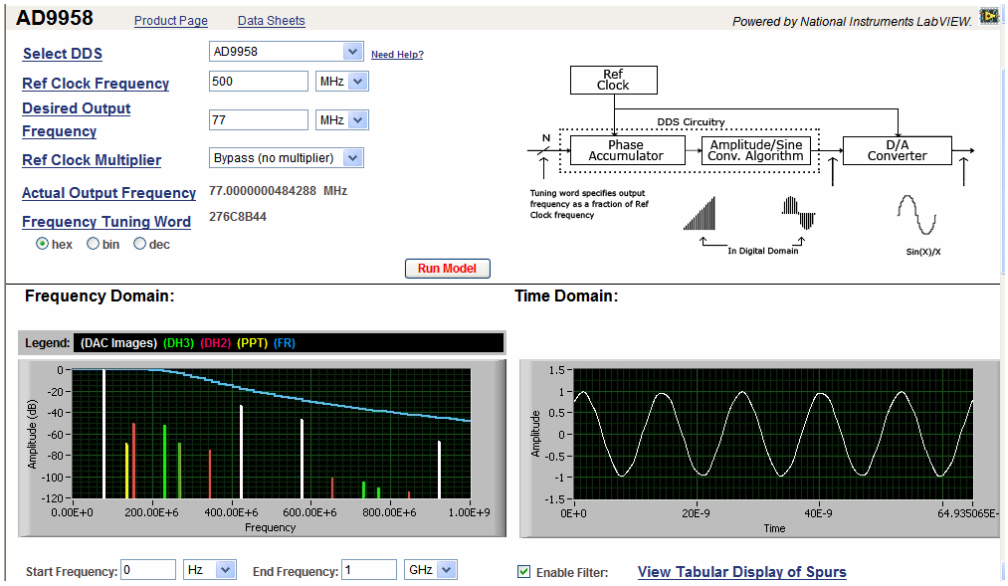
1. Locate the worst spur.
2. Program the SpurKiller DDS channel to produce a signal at a frequency slightly higher than the spur frequency.
3. Program the SpurKiller signal so that its amplitude matches that of the worst spur.
4. Program the SpurKiller signal to match the exact frequency of the worst spur. The frequency of the spur can be determined mathematically based on the update rate and the output frequency. The interactive DDS Interactive On-Line Design Tool can be of great assistance here.
5. Adjust the phase of the SpurKiller signal so that the worst spur is minimized.
6. Depending upon how accurately the SpurKiller frequency matches that of the spur, the SpurKiller frequency may require a slight adjustment for optimum results. In most cases, this won't be necessary if the spur frequency is calculated using the design tool.

The figure shows that after applying the SpurKiller technique, the worst spur is reduced in amplitude by nearly 30dB.

The current design of the AD9911 has a considerable amount of part to part variation in terms of spur magnitude. The next generation SpurKiller parts should be released in 2007. Initial silicon on these parts shows the ability to reduce spurs by at least 10dB using a single programming word across multiple parts.

DDS On-Line Interactive Design Tool (ADIsimDDS)

DDS Design Tool Main Screen



The purpose of this on-line interactive design tool is to assist a user in selecting and evaluating Analog Devices' DDS ICs. It allows a user to select a device, enter the desired operating conditions, and evaluate its general performance. It should be noted that the tool uses mathematical equations to approximate the overall performance of the selected device and does not calculate all possible errors. Therefore, the tool should be used as a design aid only and is not intended to be used as a replacement for actual hardware testing and evaluation. The basic procedure for operating the DDS tool is as follows:

1. Select a DDS device from the pulldown menu at the upper left. The "Need Help?" link (at right) can be used to obtain additional information and to make selections from a sortable DDS Interactive Selection Table (IST)

2. Input the Reference Clock Frequency

3. Input the Desired Output Frequency. Due to Nyquist requirements, the output frequency is generally limited to approximately 40% of the Reference Clock Frequency

4. Input the Ref. Clock Multiplier, if applicable. Some DDS devices offer an internal Ref. Clock Multiplier Circuit that can be used to increase the Clock Frequency

5. The Actual Output Frequency will be displayed. The actual output frequency is determined by the value of the digital tuning word and, therefore, will be slightly different than the desired output frequency.

6. The Frequency Tuning Word is displayed. This is the required digital word to be written to the DDS to obtain the desired output frequency. The tuning word value can be displayed in decimal, hexadecimal or binary by selecting the corresponding radio button.

7. Run the model. Observe the locations of the spurs as well as the time domain representation of the output signal.

DDS Design Tool: Tabular Display of Spurs

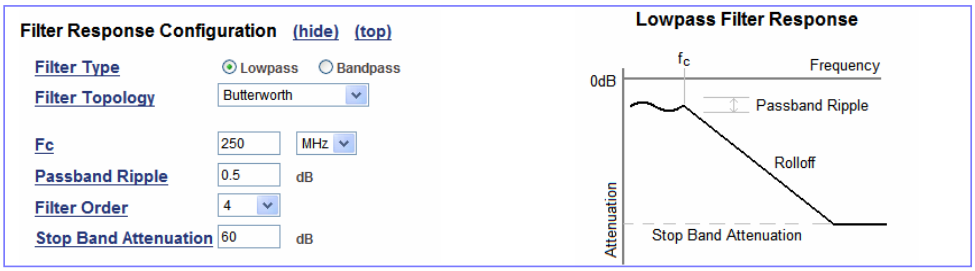
Tabular Display of Spurs (hide) (top) KEY: f1 = Ref Clock, f2 = Desired Output Frequency, PPT Spur = Primary Phase Truncation Spur

DAC Images			DAC Harmonics 2nd Order			DAC Harmonics 3rd Order			Other Spurs		
Formula	Frequency (Hz)	Attenuation (dBc)	Formula	Frequency (Hz)	Attenuation (dBc)	Formula	Frequency (Hz)	Attenuation (dBc)	Name	Frequency (Hz)	Attenuation (dBc)
f1	7.700000E+7	-0.341531	2f1	1.540000E+8	-50.341531	3f1	2.310000E+8	-50.341531	PPT Spur	1.360016E+8	-70.014874
f2-f1	4.230000E+8	-15.138524	f2-2f1	3.460000E+8	-65.138524	f2-3f1	2.690000E+8	-65.138524			
f2+f1	5.770000E+8	-17.835233	f2+2f1	6.540000E+8	-67.835233	f2+3f1	7.310000E+8	-67.835233			
2f2-f1	9.230000E+8	-21.915751	2f2-2f1	8.460000E+8	-71.915751	2f2-3f1	7.690000E+8	-71.915751			
2f2+f1	1.077000E+9	-23.256031	2f2+2f1	1.154000E+9	-73.256031	2f2+3f1	1.231000E+9	-73.256031			
3f2-f1	1.423000E+9	-25.675815	3f2-2f1	1.346000E+9	-75.675815	3f2-3f1	1.269000E+9	-75.675815			
3f2+f1	1.577000E+9	-26.568351	3f2+2f1	1.654000E+9	-76.568351	3f2+3f1	1.731000E+9	-76.568351			
4f2-f1	1.923000E+9	-28.291302	4f2-2f1	1.846000E+9	-78.291302	4f2-3f1	1.769000E+9	-78.291302			
4f2+f1	2.077000E+9	-28.960447	4f2+2f1	2.154000E+9	-78.960447	4f2+3f1	2.231000E+9	-78.960447			
5f2-f1	2.423000E+9	-30.298785	5f2-2f1	2.346000E+9	-80.298785	5f2-3f1	2.269000E+9	-80.298785			
5f2+f1	2.577000E+9	-30.834005	5f2+2f1	2.654000E+9	-80.834005	5f2+3f1	2.731000E+9	-80.834005			
6f2-f1	2.923000E+9	-31.928293	6f2-2f1	2.846000E+9	-81.928293	6f2-3f1	2.769000E+9	-81.928293			
6f2+f1	3.077000E+9	-32.374267	6f2+2f1	3.154000E+9	-82.374267	6f2+3f1	3.231000E+9	-82.374267			
7f2-f1	3.423000E+9	-33.299855	7f2-2f1	3.346000E+9	-83.299855	7f2-3f1	3.269000E+9	-83.299855			
7f2+f1	3.577000E+9	-33.682096	7f2+2f1	3.654000E+9	-83.682096	7f2+3f1	3.731000E+9	-83.682096			
8f2-f1	3.923000E+9	-34.484083	8f2-2f1	3.846000E+9	-84.484083	8f2-3f1	3.769000E+9	-84.484083			
8f2+f1	4.077000E+9	-34.818531	8f2+2f1	4.154000E+9	-84.818531	8f2+3f1	4.231000E+9	-84.818531			
9f2-f1	4.423000E+9	-35.526056	9f2-2f1	4.346000E+9	-85.526056	9f2-3f1	4.269000E+9	-85.526056			
9f2+f1	4.577000E+9	-35.823335	9f2+2f1	4.654000E+9	-85.823335	9f2+3f1	4.731000E+9	-85.823335			
10f2-f1	4.923000E+9	-36.456313	10f2-2f1	4.846000E+9	-86.456313	10f2-3f1	4.769000E+9	-86.456313			

8. View Tabular Display of Spurs. Clicking the View Tabular Display of Spurs Link located below the Time Domain Plot allows the user to view Sur Data in a Tabular Format.

9. The log box shown below the time domain plot is used to display and flag errors that may occur. Additionally, it may contain suggestions for resolving the issue.

DDS Design Tool: Display Options and Filter Selection



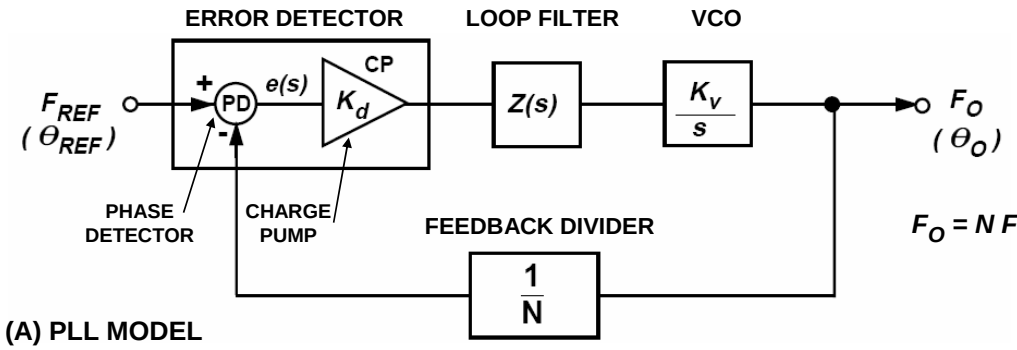
10. Modify the Display Response if desired. The tool provides check boxes and cofiguration capabilities just below the frequency domain plot. These allow a user to configure and to select to include or exclude images and spurs in the frequency domain plot.

11. Configure the Filter Response if desired. This part of the tool allows selection of the Filter Type, Filter Topology, Cutoff Frequency, Passband Ripple, Filter Order, and Stopband Attenuation.

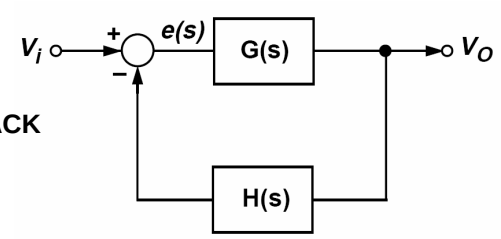
Phase Locked Loops

www.analog.com/pll

Basic Phase Locked Loop (PLL) Model



(A) PLL MODEL



(B) STANDARD NEGATIVE FEEDBACK CONTROL SYSTEM MODEL

The top diagram (A) shows the basic model for a PLL. A PLL is a feedback system combining a voltage controlled oscillator (VCO) and a phase detector connected so that the VCO maintains a constant phase angle relative to a reference signal. The PLL can be analyzed as a negative feedback system using Laplace Transform theory with a forward gain term, G(s), and a feedback term, H(s), as shown in diagram (B). The usual equations for a negative feedback system apply:

$$Forward\ Gain = G(s),\ [s = j\omega = j2\pi f]$$

$$Loop\ Gain = G(s) \times H(s)$$

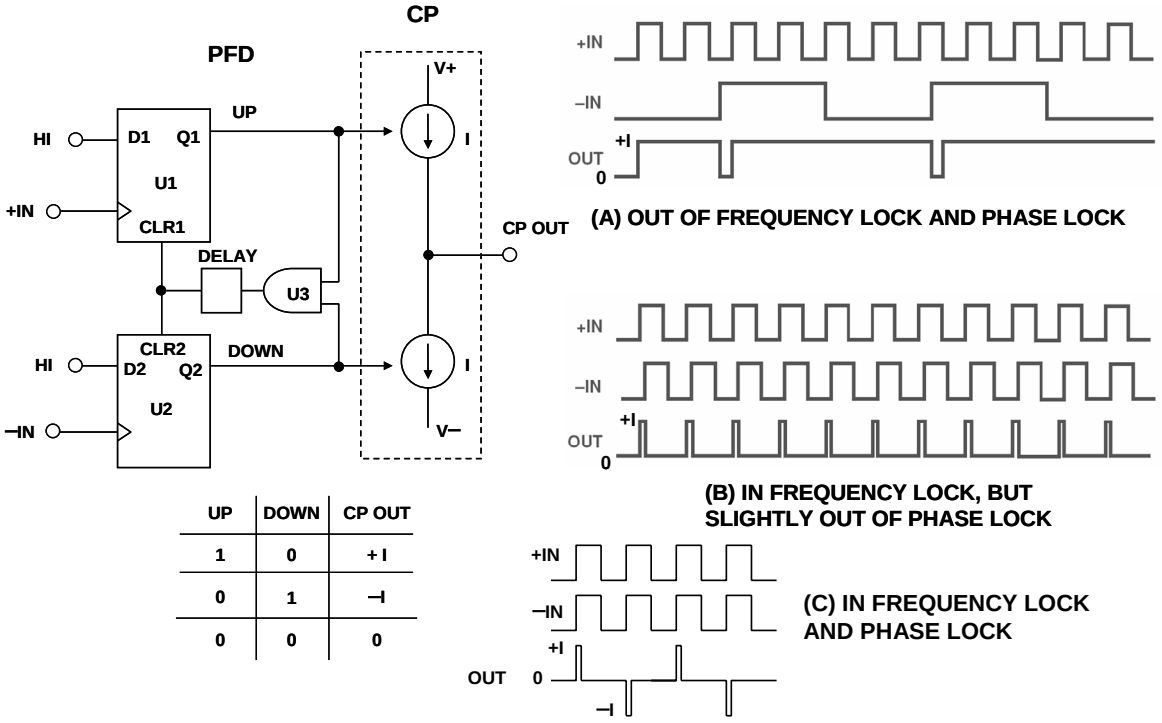
$$Closed\text{-}Loop\ Gain = \frac{G(s)}{1 + G(s)H(s)}$$

The basic blocks of the PLL are the Error Detector (composed of a phase detector and a charge pump), Loop Filter, VCO, and a Feedback Divider.

Negative feedback forces the error signal, e(s), to approach zero at which point the feedback divider output and the reference frequency are in phase and frequency lock, and $F_O = NF_{REF}$.

Referring to the above diagram, a system for using a PLL to generate higher frequencies than the input, the VCO oscillates at an angular frequency of ω_O. A portion of this signal is fed back to the error detector, via a frequency divider with a ratio 1/N. This divided down frequency is fed to one input of the error detector. The other input in this example is a fixed reference signal. The error detector compares the signals at both inputs. When the two signal inputs are equal in phase and frequency, the error will be constant and the loop is said to be in a "locked" condition.

Phase/Frequency Detector (PFD) Driving Charge Pump (CP)



UP	DOWN	CP OUT
1	0	+ I
0	1	–I
0	0	0

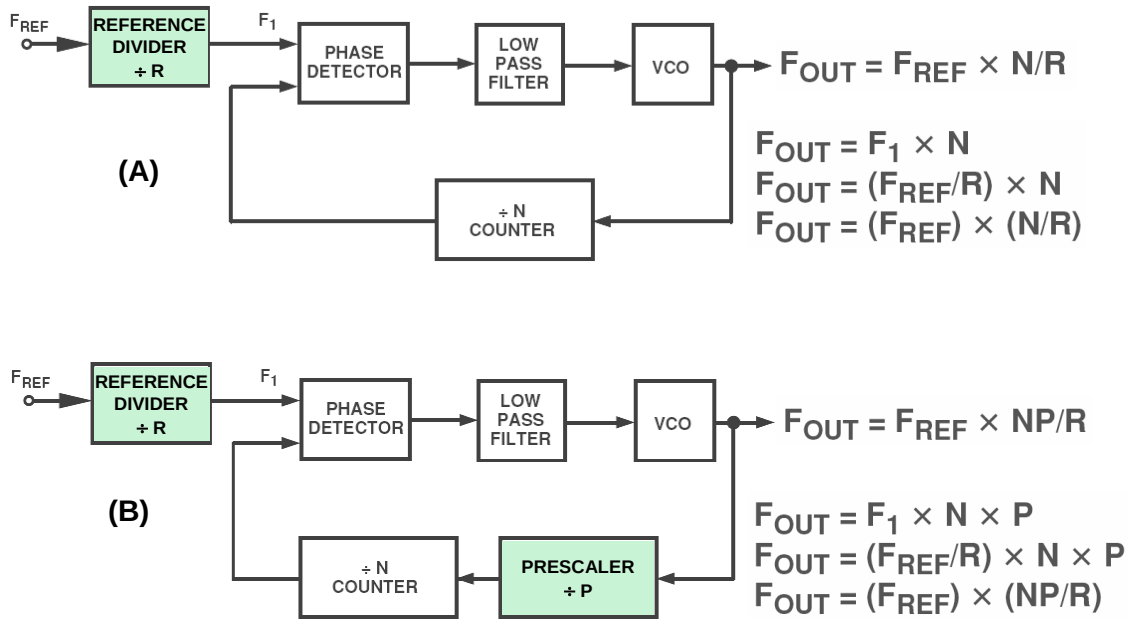
This shows a popular implementation of a PFD, basically consisting of two D-type flip flops. One Q output enables a positive current source; and the other Q output enables a negative current source. Assuming that, in this design, the D-type flip flop is positive-edge triggered, the possible states are shown in the logic table.

Consider now how the circuit behaves if the system is out of lock and the frequency at +IN is much higher than the frequency at –IN, as shown in (A).

Since the frequency at +IN is much higher than that at –IN, the UP output spends most of its time in the high state. The first rising edge on +IN sends the output high and this is maintained until the first rising edge occurs on –IN. In a practical system this means that the output, and thus the input to the VCO, is driven higher, resulting in an increase in frequency at –IN. This is exactly what is desired. If the frequency on +IN were much lower than on –IN, the opposite effect would occur. The output at OUT would spend most of its time in the low condition. This would have the effect of driving the VCO in the negative direction and again bring the frequency at –IN much closer to that at +IN, to approach the locked condition. Figure (B) shows the waveforms when the inputs are frequency-locked and close to phase-lock. Since +IN is leading –IN, the output is a series of positive current pulses. These pulses will tend to drive the VCO so that the –IN signal become phase-aligned with that on +IN. When this occurs, if there were no delay element between U3 and the CLR inputs of U1 and U2, it would be possible for the output to be in high-impedance mode, producing neither positive nor negative current pulses. This would not be a good situation. The VCO would drift until a significant phase error developed and started producing either positive or negative current pulses once again. Over a relatively long period of time, the effect of this cycling would be for the output of the charge pump to be modulated by a signal that is a subharmonic of the PFD input reference frequency. Since this could be a low frequency signal, it would not be attenuated by the loop filter and would result in very significant spurs in the VCO output spectrum, a phenomenon known as the "backlash" effect. The delay element between the output of U3 and the CLR inputs of U1 and U2 ensures that it does not happen. With the delay element, even when the +IN and –IN are perfectly phase-aligned, there will still be a current pulse generated at the charge pump output as shown in (C). The duration of this delay is equal to the delay inserted at the output of U3 and is known as the anti-backlash pulse width.

Note that if the +IN frequency is lower than the −IN frequency and/or the +IN phase lags the −IN phase, then the output of the charge pump will be a series of negative current pulses—the reverse of the condition shown in (A) and (B) above.

Adding an Input Reference Divider and a Prescaler to the Basic PLL

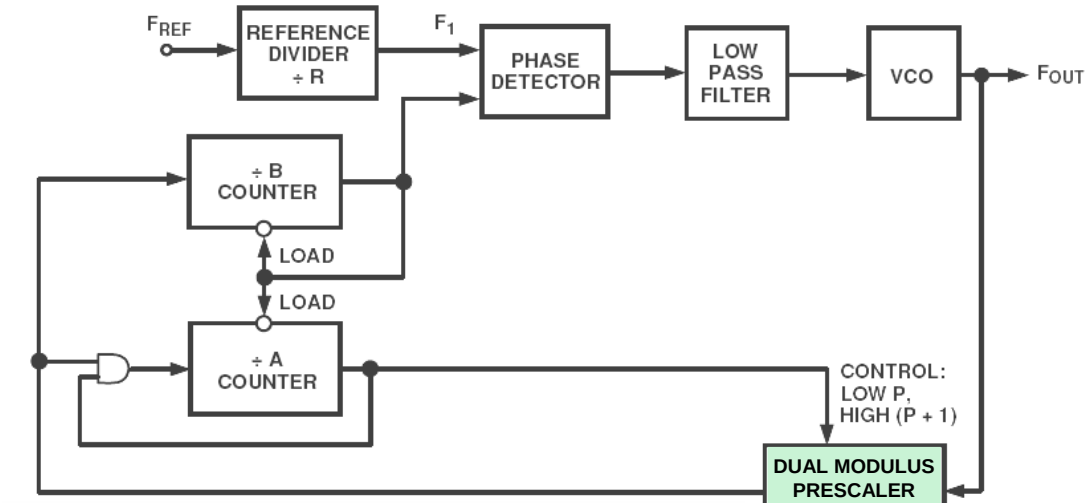


In the classical Integer-N synthesizer, the resolution of the output frequency is determined by the reference frequency applied to the phase detector. So, for example, if 200kHz spacing is required (as in GSM phones), then the reference frequency must be 200kHz. However, getting a stable 200kHz frequency source is not easy. A sensible approach is to take a good crystal-based high frequency source and divide it down. For example, the desired frequency spacing could be achieved by starting with a 10MHz frequency reference and dividing it down by 50. This approach is shown in the diagram (A).

The "N counter," also known as the N divider, is the programmable element that sets the relationship between the input and output frequencies in the PLL. The complexity of the N counter has grown over the years. In addition to a straightforward N counter, it has evolved to include a prescaler, which can have a dual modulus. This structure has grown as a solution to the problems inherent in using the basic divide-by-N structure to feed back to the phase detector when very high-frequency outputs are required. For example, let’s assume that a 900MHz output is required with 10Hz spacing. A 10MHz reference frequency might be used, with the R-Divider set at 1000. Then, the N-value in the feedback would need to be of the order of 90,000. This would mean at least a 17- bit counter capable of dealing with an input frequency of 900MHz. To handle this range, it makes sense to precede the programmable counter with a fixed counter element to bring the very high input frequency down to a range at which standard CMOS will operate. This counter, called a prescaler, is shown in diagram (B).

However, note that using a standard prescaler as shown reduces the system resolution to F1×P. This issue can be addressed by using a dual-modulus prescaler which has the advantages of a standard prescaler, but without loss of resolution. A dual-modulus prescaler is a counter whose division ratio can be switched from one value to another by an external control signal. It's use is described in the next figure.

Adding a Dual Modulus Prescaler to the PLL



TOTAL NUMBER OF COUNTS OF F_{OUT} IN A FULL F_1 CYCLE

$A \times (P + 1) + (B - A)P$ =

$AP + A + BP - AP$ =

$BP + A$, THEREFORE

$F_{OUT} = F_1 \times (BP + A)$

$F_{OUT} = (F_{REF}/R) \times (BP + A)$

By using the dual-modulus prescaler with an A and B counter, one can still maintain output resolution of F1. However, the following conditions must be met:

1. The output signals of both counters are High if the counters have not timed out.
2. When the B counter times out, its output goes Low, and it immediately loads both counters to their preset values.
3. The value loaded to the B counter must always be greater than that loaded to the A counter.

Assume that the B counter has just timed out and both counters have been reloaded with the values A and B. Let's find the number of VCO cycles necessary to get to the same state again.

As long as the A counter has not timed out, the prescaler is dividing down by P + 1. So, both the A and B counters will count down by 1 every time the prescaler counts (P + 1) VCO cycles. This means the A counter will time out after ((P + 1) × A) VCO cycles. At this point the prescaler is switched to divide-by-P. It is also possible to say that at this time the B counter still has (B – A) cycles to go before it times out. How long will it take to do this: ((B – A) × P).

The system is now back to the initial condition where we started.

The total number of VCO cycles needed for this to happen is :

$$N = [A \times (P + 1)] + [(B - A) \times P]$$
$$= AP + A + BP - AP$$
$$= BP + A.$$

Therefore, $F_{OUT} = (F_{REF}/R) \times (BP + A)$.

Key PLL Specifications

- **Input RF Frequency (Minimum/Maximum)**
- **Channel Spacing**
- **Loop Bandwidth and Phase Margin**
- **Frequency Lock Time**
- **Phase Lock Time**
- **Output Frequency Error**
- **Output Phase Error**
- **Phase Noise and Phase Jitter**
- **Reference Spurs**

There are many specifications to consider when designing a PLL. The input RF frequency range and the channel spacing determine the value of the R and N counter and the prescaler parameters.

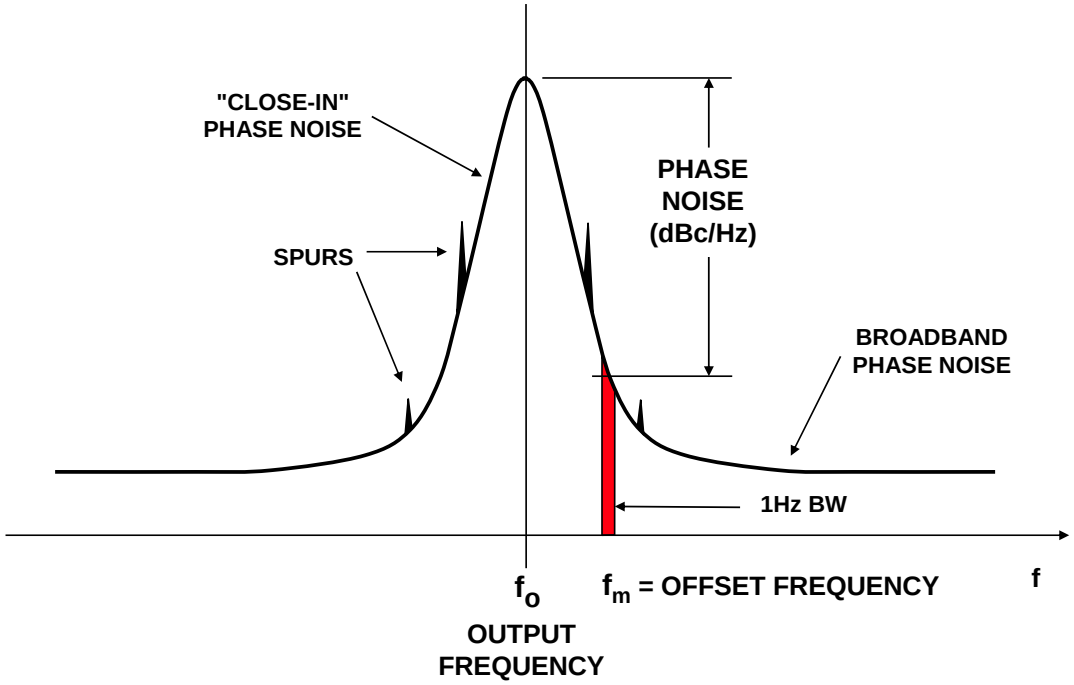
The loop bandwidth determines the frequency and phase lock time. Since the PLL is a negative feedback system, phase margin and stability issues must be considered.

Spectral purity of the PLL output is specified by the phase noise and the level of the reference-related spurs.

Many of these parameters are interactive; for instance, lower values of loop bandwidth lead to reduced levels of phase noise and reference spurs, but at the expense of longer lock times and less phase margin.

Because of the many tradeoffs involved, the use of a PLL design program such as the Analog Devices' ADIsimPLL allows these tradeoffs to be evaluated and the various parameters adjusted to fit the required specifications. The program not only assists in the theoretical design, but also aids in parts selection and determines component values.

Oscillator Phase Noise and Spurs



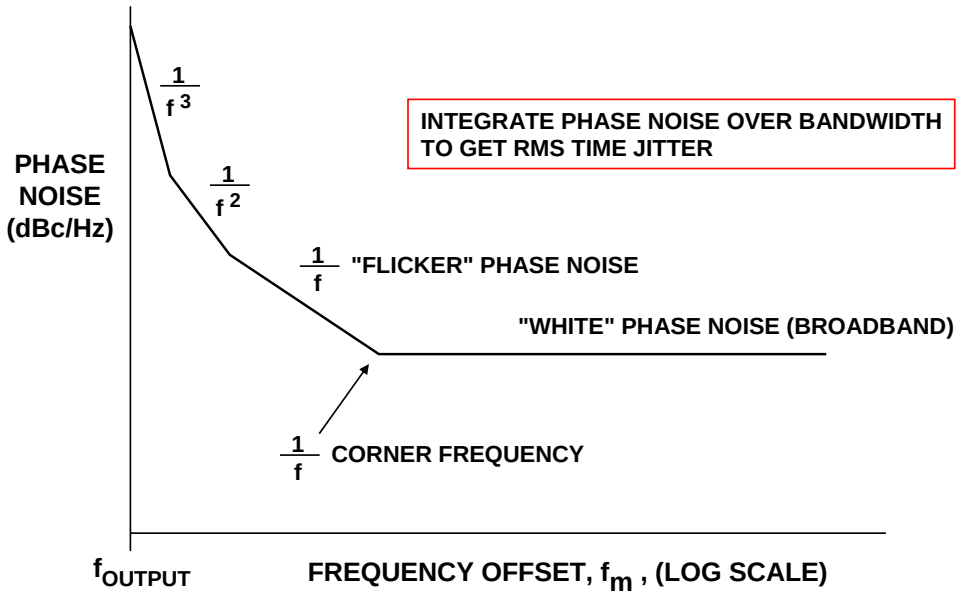
A PLL is a type of oscillator, and in any oscillator design, frequency stability is of critical importance. We are interested in both long-term and short-term stability. Long-term frequency stability is concerned with how the output signal varies over a long period of time (hours, days, or months). It is usually specified as the ratio, $\Delta f/f$ for a given period of time, expressed as a percentage or in dB.

Short-term stability, on the other hand, is concerned with variations that occur over a period of seconds or less. These variations can be random or periodic. A spectrum analyzer can be used to examine the short-term stability of a signal. This diagram shows a typical spectrum, with random and discrete frequency components causing a broad skirt and spurious peaks.

The discrete spurious components could be caused by known clock frequencies in the signal source, power line interference, and mixer products. The broadening caused by random noise fluctuation is due to phase noise. It can be the result of thermal noise, shot noise, and/or flicker noise in active and passive devices.

The phase noise spectrum of an oscillator shows the noise power in a 1Hz bandwidth as a function of frequency. Phase noise is defined as the ratio of the noise in a 1Hz bandwidth at a specified frequency offset, f_m, to the oscillator signal amplitude at frequency f_o.

Phase Noise in dBc/Hz Versus Frequency Offset from Output Frequency



It is customary to characterize an oscillator in terms of its single-sideband phase noise as shown here, where the phase noise in dBc/Hz is plotted as a function of frequency offset, f_m, with the frequency axis on a log scale. Note the actual curve is approximated by a number of regions, each having a slope of $1/f^x$, where x = 0 corresponds to the "white" phase noise region (slope = 0dB/decade), and x = 1 corresponds to the "flicker" phase noise region (slope = –20dB/decade). There are also regions where x = 2, 3, 4, and these regions occur progressively closer to the carrier frequency.

Note that the phase noise curve is somewhat analogous to the input voltage noise spectral density of an amplifier. Like amplifier voltage noise, low 1/f corner frequencies are highly desirable in an oscillator.

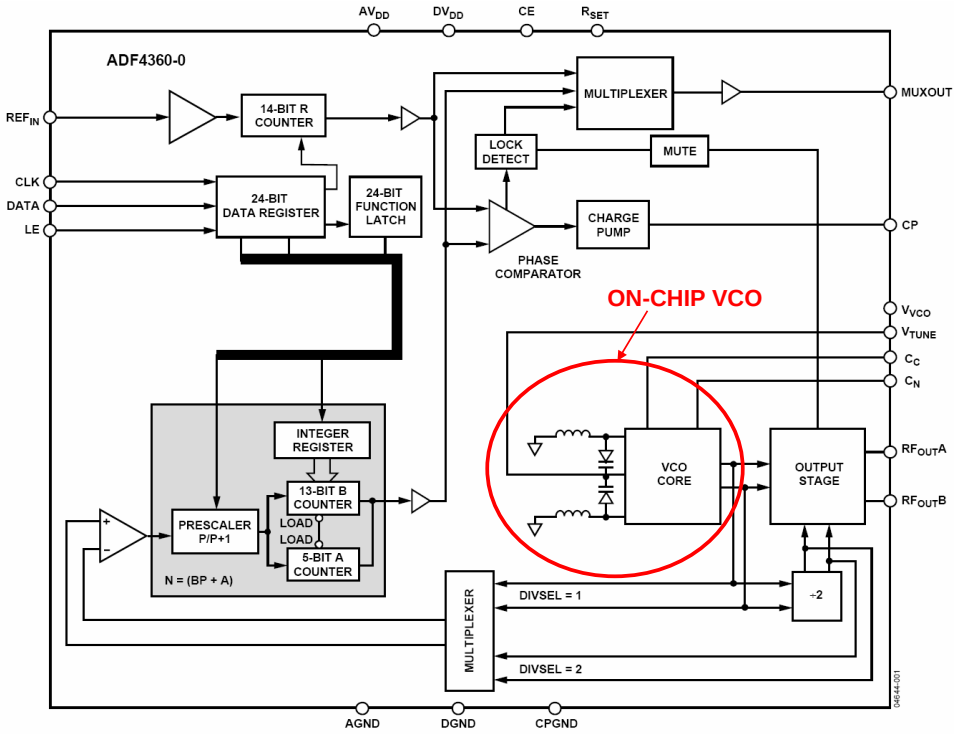
In some cases, it is useful to convert phase noise into time jitter. This can be done by basically integrating the phase noise plot over the desired frequency range. The ADIsimPLL program performs this calculation if needed. Details of how to convert phase noise into time jitter can be found in the following reference:

Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN-0916550273 Chapter 6. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410, Chapter 6.

The ability to perform this conversion between phase noise and time jitter is especially useful when using the PLL output to drive an ADC sampling clock. Once the time jitter is known, its effect on the overall ADC SNR can be evaluated.

The ADIsimPLL program (to be discussed shortly) performs the conversion between phase noise and time jitter.

ADF4360 Family of Integrated PLLs



We will now examine a couple of examples of PLL ICs from Analog Devices. It would be impossible to discuss all of them, so for complete coverage refer to www.analog.com/PLL.

The ADF4360 family of integrated PLLs include the integer-N synthesizer with prescalars and VCO. They are optimized for the output frequency ranges given in parentheses: ADF4360-0 (2400MHz to 2725MHz), ADF4360-1 (2050MHz to 2450MHz), ADF4360-2 (1850MHz to 2150MHz), ADF4360-3 (1600MHz to 1950MHz), ADF4360-4 (1450MHz to 1750MHz), ADF4360-5 (1200MHz to 1400MHz), ADF4360-6 (1050MHz to 1250MHz), ADF4360-7 (350MHz to 1800MHz). The reference input frequency can range from 10MHz to 250MHz.

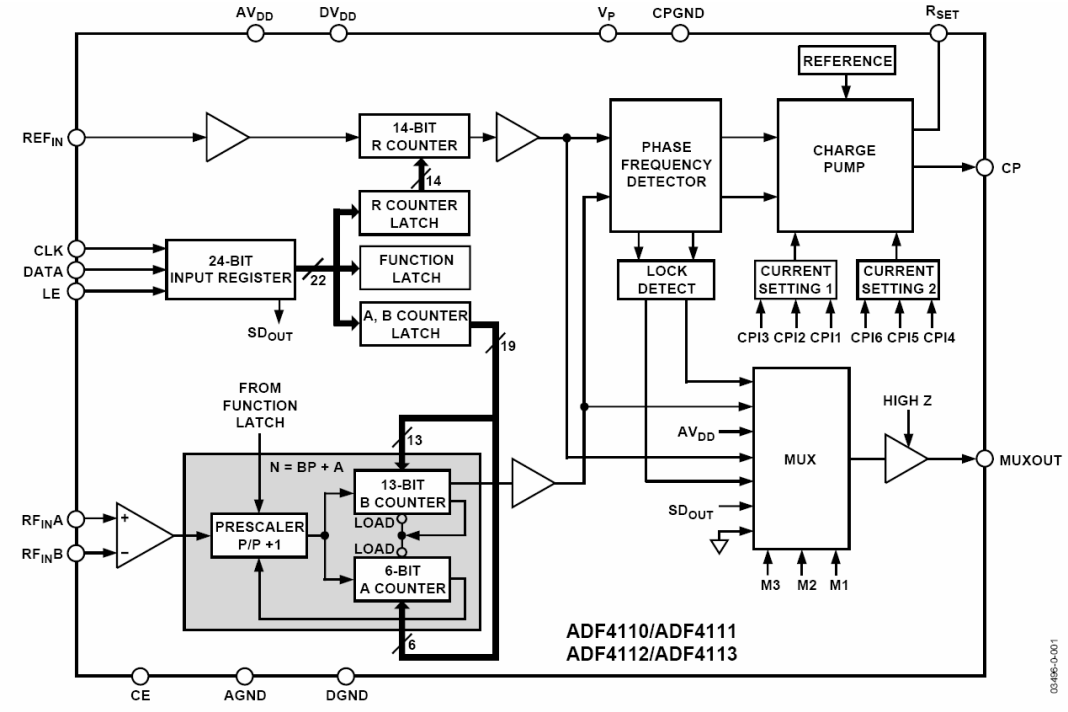
The ADF4360-7 has a prescaler, but the center frequency is set by external inductors.

The ADF4360-8 also has the center frequency set by external inductors. This allows an output frequency range of between 65MHz to 400MHz. The ADF4360-8 has no RF prescaler.

All members of the ADF 4360 family operate on +3.0V to +3.6V and have 1.8V logic interface compatibility. The output power level can be programmed from −13dBm to −4dBm, and the VCO current is programmable in 5mA steps between 5mA and 20mA. The total power supply current ranges between 25mA to 50mA (or 45mA), depending on the particular part and the programmed settings.

All members of the family are packaged in a 24-lead CSP.

Block Diagram of ADF4110 Family



The ADF4110 family of synthesizers consists of single devices, and the ADF4210 family consists of dual versions. The block diagram for the ADF4110 is shown here. It contains the reference counter, the dual-modulus prescaler, the N counter and the PFD blocks previously described. The VCO must be supplied externally, and for low phase noise applications, crystal VCOs (VCXOs) are often used.

The ADF4110 family of frequency synthesizers can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. They consist of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R counter) allows selectable REF_{IN} frequencies at the PFD input.

A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7V to 5.5V and can be powered down when not in use.

RF input frequencies for the various parts in the family are as follows (+5V supply).

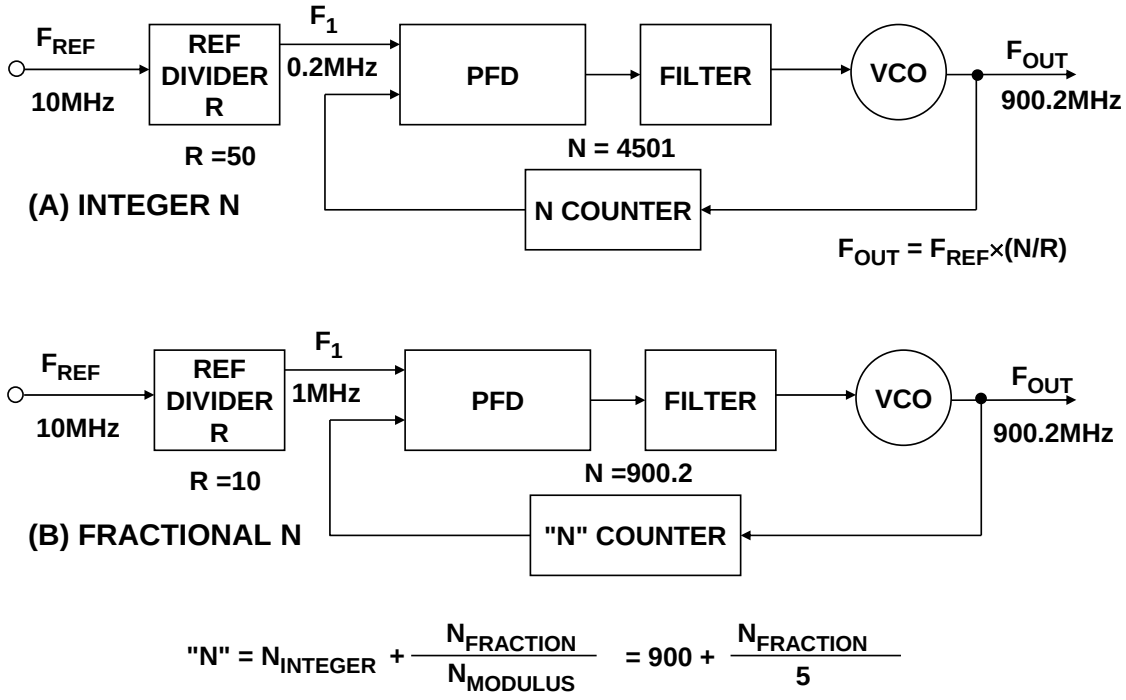
ADF4110: 80/550 MHz (min/max)

ADF4111: 0.08/1.4 GHz (min/max)

ADF4112: 0.1/3.0 GHz (min/max)

ADF4113: 0.2/4.0 GHz (min/max)

Integer-N Compared to Fractional-N Synthesizer

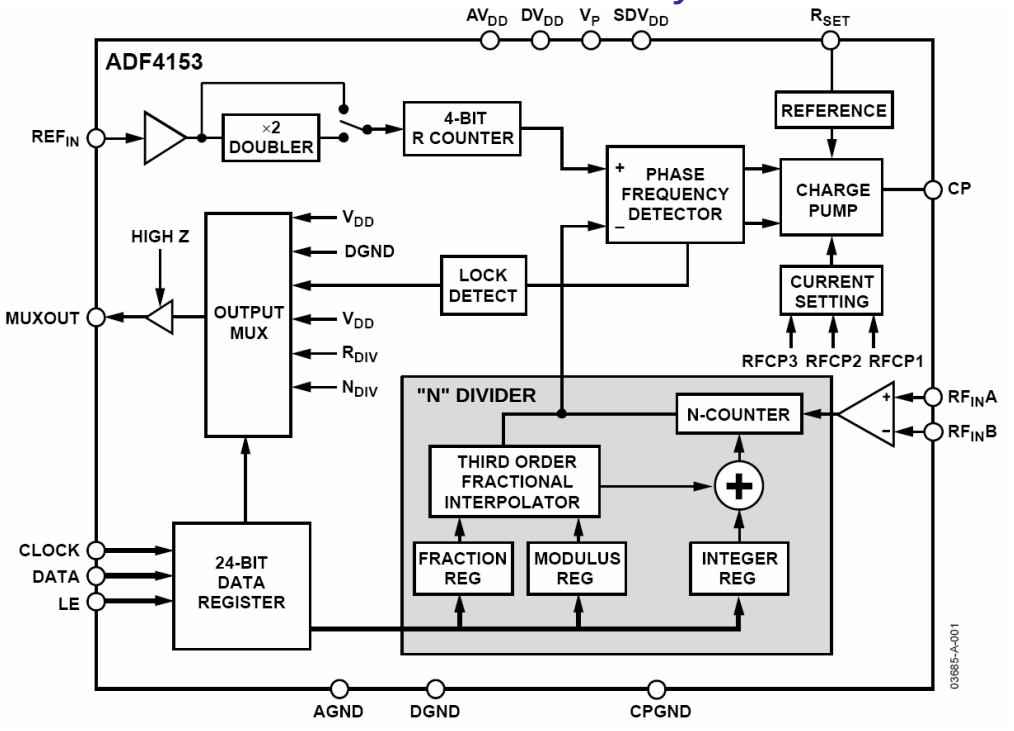


$$\text{"N"} = N_{INTEGER} + \frac{N_{FRACTION}}{N_{MODULUS}} = 900 + \frac{N_{FRACTION}}{5}$$

Fractional-N PLLs have been utilized since the 1970s. As has been discussed, the resolution at the output of an integer-N PLL is limited to steps of the PFD input frequency as shown in (A), where the PFD input is 0.2MHz. Fractional-N allows the resolution at the PLL output to be reduced to small fractions of the PFD frequency as shown in (B), where the PFD input frequency is 1MHz. It is possible to generate output frequencies with resolutions of 100s of Hz, while maintaining a high PFD frequency. As a result the N-value is significantly less than for integer-N. Since noise at the charge pump is multiplied up to the output at a rate of 20logN, significant improvements in phase noise are possible. For a GSM900 system, the fractional-N ADF4252 offers phase noise performance of –103dBc/Hz, compared with –93dBc/Hz for the ADF4106 integer-N PLL. Also offering a significant advantage is the lock-time improvement made possible by fractional-N. The PFD frequency set to 20MHz and loop bandwidth of 150kHz will allow the synthesizer to jump 30MHz in less than 30µs. Current base stations require two PLL blocks to ensure that LOs can meet the timing requirements for transmissions. With the super-fast lock times of fractional-N, future synthesizers will have lock time specs that allow the two "ping-pong" PLLs to be replaced with a single fractional-N PLL block.

The downside of fractional-N PLLs is higher spurious levels. A fractional-N divide by 900.2 consists of the N-divider dividing by 900 80% of the time, and by 901 20% of the time. The average division is correct, but the instantaneous division is incorrect. Because of this, the PFD and charge pump are constantly trying to correct for instantaneous phase errors. The heavy digital activity of the sigma-delta modulator, which provides the averaging function, creates spurious components at the output. The digital noise, combined with inaccuracies in matching the hard-working charge pump, results in spurious levels greater than those allowable by most communications standards. Only recently have fractional-N parts, such as the ADF4252, made the necessary improvements in spurious performance to allow designers to consider their use in traditional integer-N markets.

ADF4153 Fractional-N Synthesizer



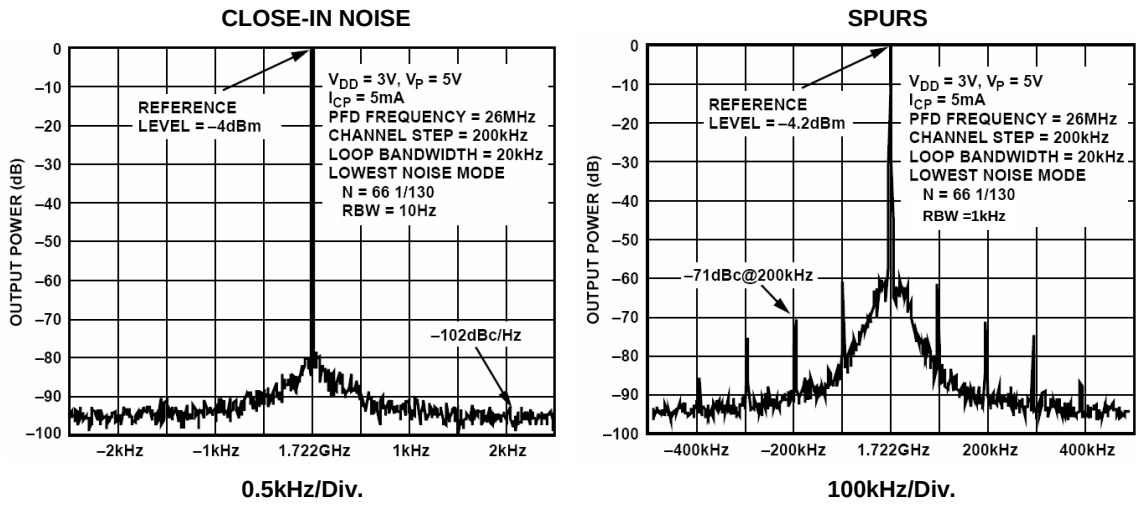
"N" = $N_{INTEGER}$ + $N_{FRACTION}$ / $N_{MODULUS}$

The ADF4153 is a fractional-N frequency synthesizer that implements local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a third order Σ-Δ-based fractional interpolator to allow programmable fractional-N division. The INTEGER, FRACTION, and MODULUS registers define an overall N divider, where "N" = NINTEGER + NFRACTION/NMODULUS.

In addition, the 4-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and a voltage controlled oscillator (VCO). Control of all on-chip registers is via a simple 3-wire interface. The device operates with a power supply ranging from 2.7V to 3.3V and can be powered down when not in use.

"Noise" and "spur" mode allows the user to optimize a design either for improved spurious performance or for improved phase noise performance. When the lowest spur setting is chosen, dither is enabled. This randomizes the fractional quantization noise so that it looks more like white noise rather than spurious noise. This means that the part is optimized for improved spurious performance. This operation would normally be used when the PLL closed-loop bandwidth is wide, for fast-locking applications. (Wide-loop bandwidth is seen as a loop bandwidth greater than 1/10 of the RFOUT channel step resolution (fRES)). A wide-loop filter does not attenuate the spurs to a level that a narrow-loop bandwidth would. When the low noise and spur setting is enabled, dither is disabled. This optimizes the synthesizer to operate with improved noise performance. However, the spurious performance is degraded in this mode compared to the lowest spurs setting. To further improve noise performance, the lowest noise setting option can be used, which reduces the phase noise. As well as disabling the dither, it also ensures that the charge pump is operating in an optimum region for noise performance. This setting is extremely useful where a narrow-loop filter bandwidth is available. The synthesizer ensures extremely low noise, and the filter attenuates the spurs.

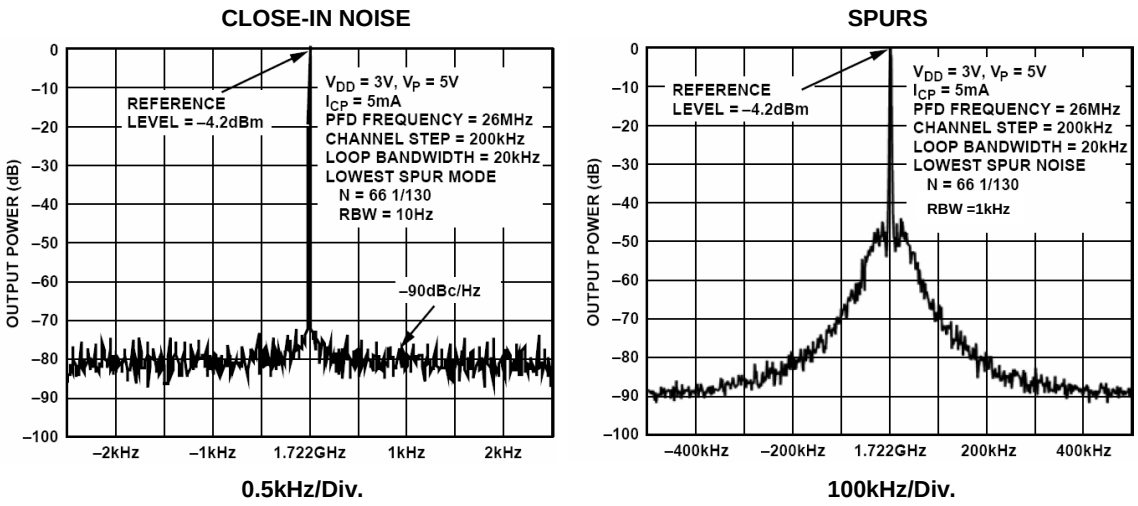
ADF4153 Operating in Lowest Noise Mode for N = 8581/130



This figure shows the noise and spur performance for the ADF4153 operating in the lowest noise mode. The PFD input frequency is 26MHz, channel step size is 200kHz, loop bandwidth is 20kHz, N = 66 1/130, and the receiver bandwidth is set for 10Hz. The output frequency is 1.7162GHz.

Note that the noise is approximately –102dBc/Hz, and the spur at 200kHz offset is –71dBc.

ADF4153 Operating in Lowest Spur Mode for N = 8581/130

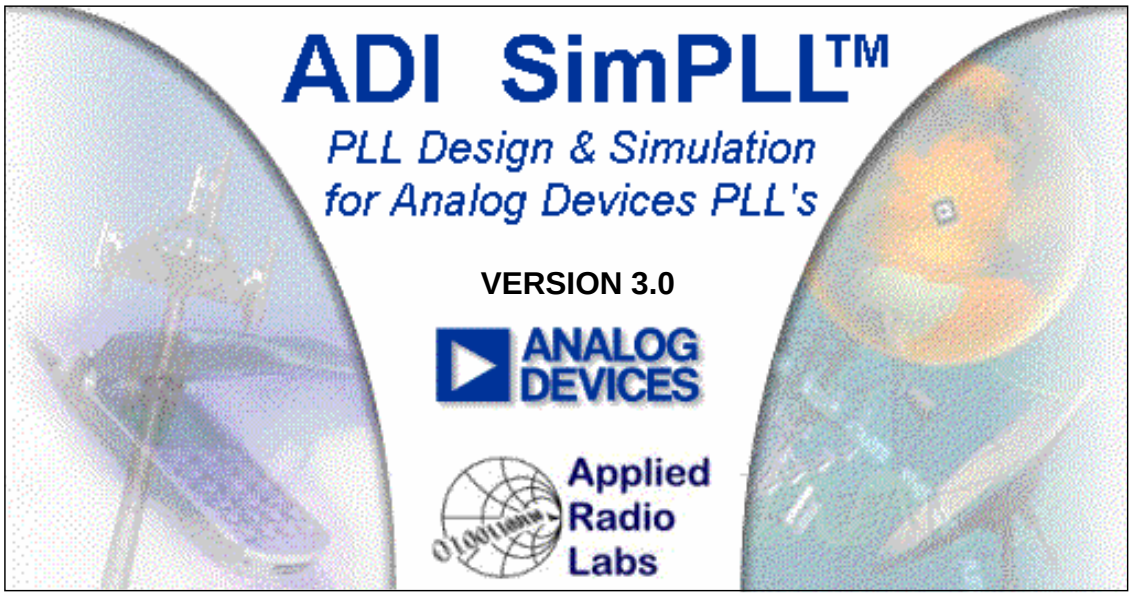


This figure shows the noise and spur performance for the ADF4153 operating in the lowest spur mode. The PFD input frequency is 26MHz, channel step size is 200kHz, loop bandwidth is 20kHz, N = 66 1/130, and the receiver bandwidth is set for 10Hz. The output frequency is 1.7162GHz.

Note that the noise is approximately –90dBc/Hz, and the spur at 200kHz offset indistinguishable from the noise level which is –80dBc.

The ADF4153 also has a "lowest noise and spur" mode. In this mode, the noise is approximately –95dBc/Hz, and the spur at 200kHz offset is –74dBc. These values are measured under the same conditions as the data presented in the two figures.

PLL Design Software



www.analog.com/adisimpll

The ADIsimPLL™ software is a complete PLL design package which can be downloaded from the Analog Devices' website at www.analog.com/adisimpll. The software has a user-friendly graphical interface, and a complete comprehensive tutorial for first-time users.

Traditionally, PLL Synthesizer design relied on published application notes to assist in the design of the PLL loop filter. It was necessary to build prototype circuits to determine key performance parameters such as lock time, phase noise, and reference spurious levels. Optimization was accomplished by "tweaking" component values on the bench and repeating lengthy measurements.

ADIsimPLL both streamlines and improves the traditional design process. Starting with the “new PLL wizard,” a designer constructs a PLL by specifying the frequency requirements of the PLL, selecting an integer-N or fractional-N implementation, and then choosing from a library of PLL chips, library or custom VCO, and a loop filter from a range of topologies. The program designs a loop filter and displays key parameters including phase noise, reference spurs, lock time, lock detect performance, and others.

ADIsimPLL operates with spreadsheet-like simplicity and interactivity. The full range of design parameters such as loop bandwidth, phase margin, VCO sensitivity, and component values can be altered with real-time updates of the simulation results. This allows the user to easily optimize the design for specific requirements. Varying the bandwidth, for example, enables the user to observe the tradeoff between lock time and phase noise in real-time, and with bench-measurement accuracy.

ADIsimPLL includes accurate models for phase noise, enabling reliable prediction of the synthesizer closed-loop phase noise. Users report excellent correlation between simulation and measurement. If required, the designer can work directly at the component level and observe the effects of varying individual component values.

ADIsimPLL Design Process

- **Choose reference frequency, output frequency range, and channel spacing**
- **Select PLL chip from list**
- **Select VCO**
- **Select loop filter configuration**
- **Select loop filter bandwidth and phase margin**
- **Run simulation**
- **Evaluate time and frequency domain results**
- **Optimize**

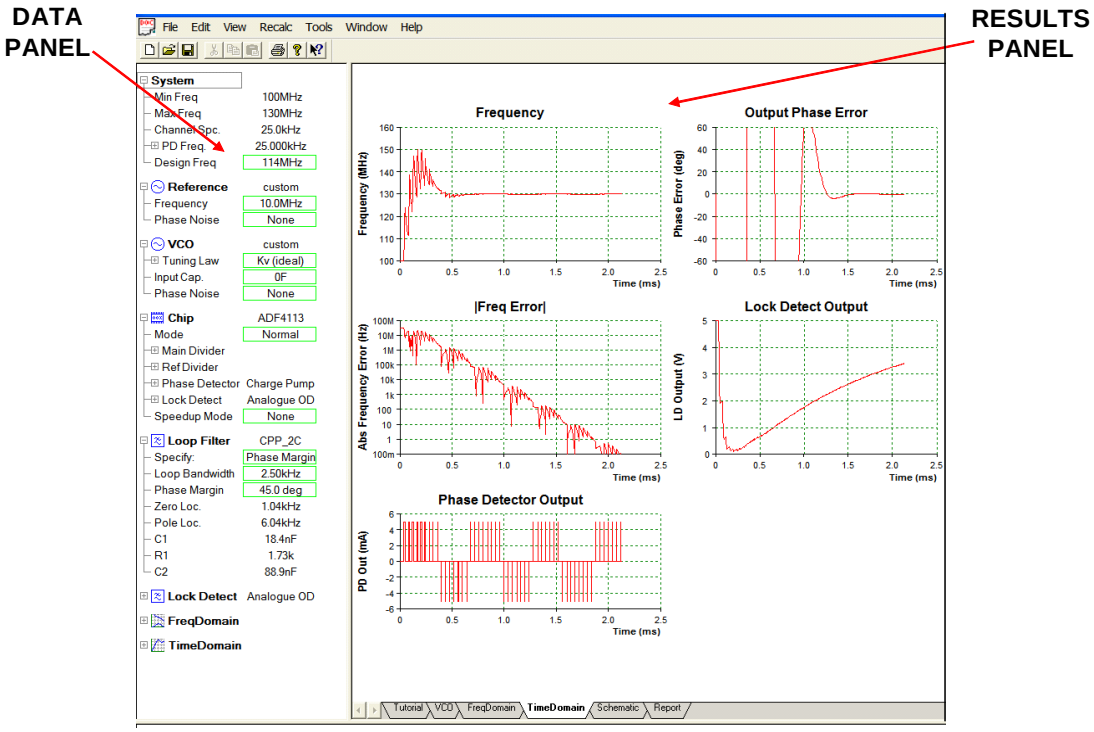
- **Works for integer-N or fractional-N but does not simulate fractional-N spurs. Phase noise prediction for fractional-N devices assumes the device is operating in the "lowest phase noise" mode.**

This figure shows the basic steps in creating a design with ADisimPLL.

ADIsimPLL accurately simulates locking behavior in the PLL, including the most significant non-linear effects. Unlike simple linear simulators based on Laplace transform solutions, ADIsimPLL includes the effects of phase detector cycle slipping, charge pump saturation, curvature in the VCO tuning law, and the sampling nature of the phase-frequency detector. As well as providing accurate simulation of frequency transients, giving detailed lock-time predictions for frequency and phase lock, ADIsimPLL also simulates the lock detect circuit. For the first time, designers can easily predict how the lock detect circuit will perform without having to resort to measurements.

The simulation engine in ADIsimPLL is fast, with all results typically updating "instantaneously," even transient simulations. As well as providing an interactive environment that enables the design to be easily optimized, it also encourages the designer to explore the wide range of design options and parameters available. Contrary to the traditional methods where to design, to build, and then to measure parameters takes days, ADIsimPLL enables the user to change the PLL circuit design and to observe instantly the performance changes. ADIsimPLL allows the designer to work at a higher level and to directly modify derived parameters such as the loop bandwidth; phase margin, pole locations, and the effects of the changes on performance are shown instantly (and without burning fingers with a soldering iron!).

Data Panel and Time Domain Results Panel



This figure shows the data panel on the left and the time domain results panel on the right. If values are changed in the data panel, the results of the changes are instantly computed and displayed in the results panel.

ADIsimPLL Version 3.0 includes many enhancements including:

1. The program includes a short-form selector guide for choosing the PLL chip, displaying short-form data for all chips, with built-in links to the product pages on the Analog Devices website.

2. Similar short-form selector guides are available for choosing the VCO, and these contain links to detailed device data on vendor's websites.

3. The chip-programming assistant enables rapid calculation of programming register values to set the chip to any specified frequency. This is also good for checking channels that cannot be reached due to prescaler restrictions.

4. The range of loop filters has been expanded to include a 4-pole passive filter and a non-inverting active filter. As with all loop filter designs in ADIsimPLL, these models accurately include the thermal noise from resistors, the op-amp voltage and current noise, as well as predicting reference spurs resulting from the op-amp bias current.

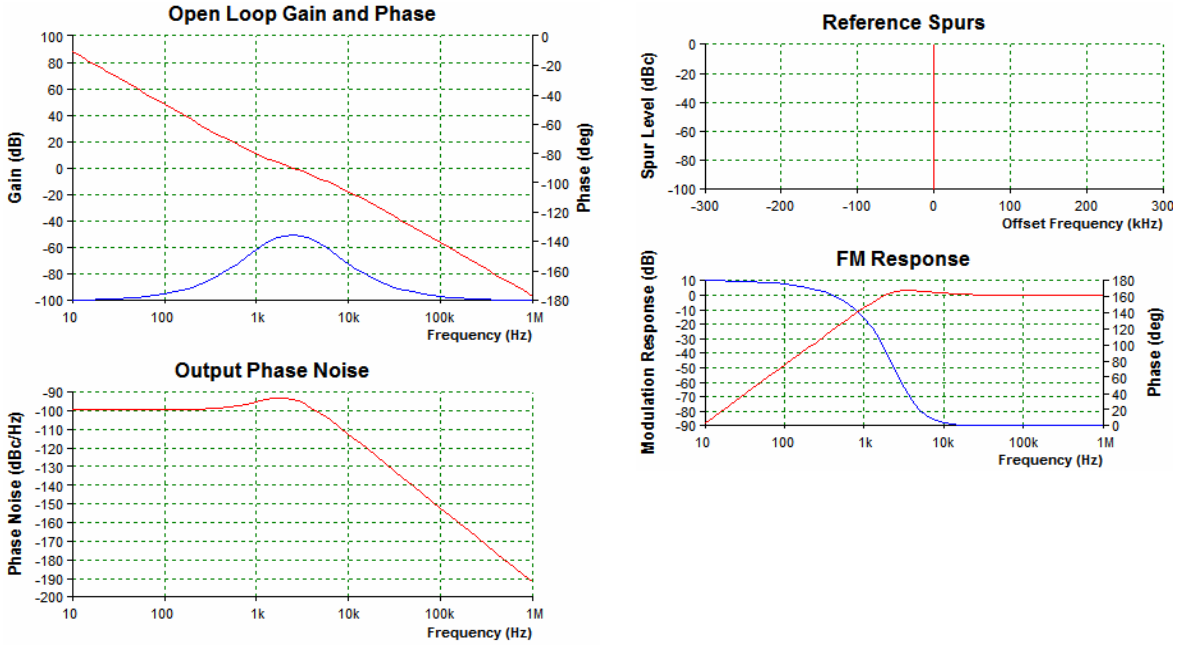
5. Phase jitter results can now be displayed in degrees, seconds or Error Vector Magnitude (EVM)

6. It is now possible to simulate the power-up frequency transient.

7. Support has been included for the new Analog Devices PLL chips with integrated VCOs.

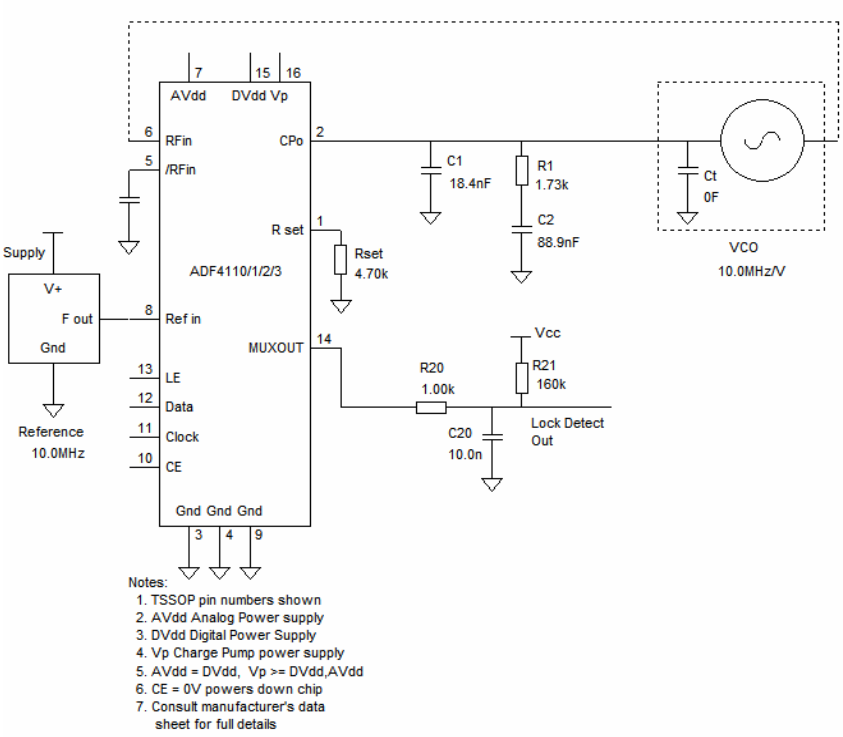
8.The program works for both integer-N and fractional-N devices. However, Phase noise prediction for fractional-N devices assumes the device is operating in the "lowest phase noise" mode.

Frequency Domain Results



This figure shows a typical display of the frequency domain results in ADIsimPLL. Note that an ideal reference with no spurs was chosen for this particular program demonstration.

ADIsimPLL—Schematic



This figure shows the schematic output for the final design, including component values.

All the information required to build the actual PLL is available from the output of ADIsimPLL.

PLL References

1. **Mike Curtin and Paul O'Brien, "Phase-Locked Loops for High-Frequency Receivers and Transmitters"**
   - **Part 1, *Analog Dialogue*, 33-3, Analog Devices, 1999**
   - **Part 2, *Analog Dialogue*, 33-5, Analog Devices, 1999**
   - **Part 3, *Analog Dialogue*, 33-7, Analog Devices, 1999**
2. **Roland E. Best, *Phase Locked Loops, 5th Edition*, McGraw-Hill, 2003, ISBN: 0071412018.**
3. **Floyd M. Gardner, *Phaselock Techniques, 2nd Edition*, John Wiley, 1979, ISBN: 0471042943.**
4. **Dean Banerjee, *PLL Performance, Simulation and Design, 3rd Edition*, Dean Banerjee Publications, 2003, ISBN: 0970820712 .**
5. **Bar-Giora Goldberg, *Digital Frequency Synthesis Demystified*, Newnes, 1999, ISBN: 1878707477.**
6. **Brendan Daly, "Comparing Integer-N and Fractional-N Synthesizers," *Microwaves and RF*, September 2001, pp. 210-215.**
7. **Adrian Fox, "Ask The Applications Engineer-30 (Discussion of PLLs)," *Analog Dialogue*, 36-3, 2002.**
8. **Walt Kester, *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410, Chapter 6, pp. 427-440.**
9. **Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006.**

This figure shows a list of key references on PLLs and PLL design. They should be very helpful for users inexperienced in PLLs. Reference 1 is a particularly good overview of PLL design. Reference 2 and 3 are classic textbooks on PLLs, and References 4-8 are more recent articles and books.

Clock Generation and Distribution

www.analog.com/clocks

Dimensions of Performance in Clock Generation and Distribution ICs

FUNCTIONS

- Clock Generation
- Clock Cleanup
- Clock Division
- Clock Multiplication
- Delay Adjustment
- Phase Adjustment
- Clock Distribution
- Fanout Buffers
- Logic Level Translation

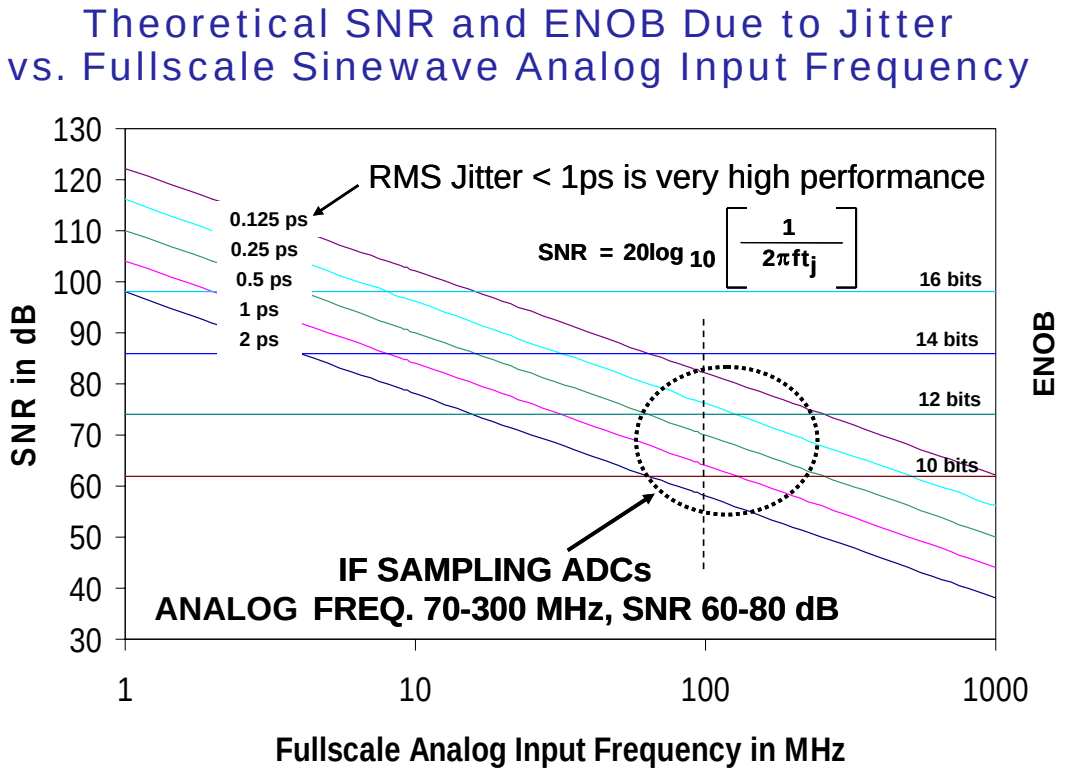
SPECIFICATIONS

- Speed
- Slew Rate
- Edge Skew
- Rise/Fall Time
- Phase Noise
- Jitter
- Channel Isolation
- EMI/RFI
- Design Tools

System clock management has become much more complex in the last few years. In addition to the requirement for multiple synchronized clocks, the proliferation of data converters has added a new dimension of performance requirements.

Because of the effect of jitter on converter SNR, the converter sampling clock must have very low jitter regardless of how corrupt the other clocks in the system may be.

This figure shows the basic functions of clock generation and distribution and the important performance specifications. The need for these functions has resulted in an entirely new product family of clock and clock distribution ICs which did not exist a decade ago.



This figure shows the effects of sampling clock jitter on system SNR. It can be shown that jitter on the sampling clock degrades the overall SNR per the simple equation:

$$SNR = 20\log_{10}[1/2\pi ft_j],$$

where f is the fullscale analog input frequency and t_j is the total clock jitter (the root-sum-square of the ADC aperture jitter and the external sampling clock jitter).

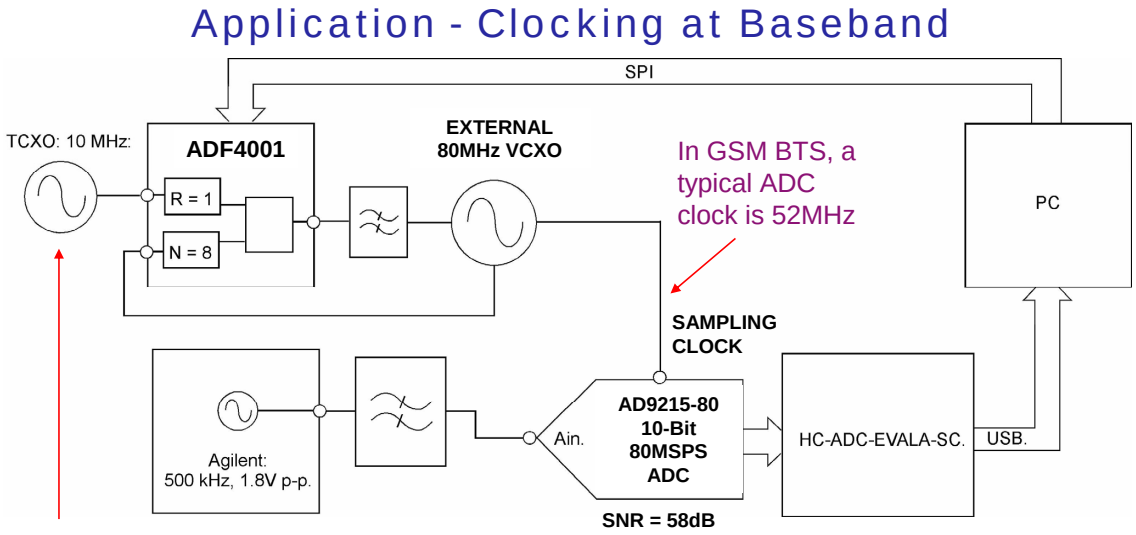
It should be noted that this equation assumes an ADC of infinite resolution, where the only error is the noise produced by the clock jitter.

This figure shows SNR on the left and ENOB on the right, related by the simple equation SNR = 6.02N + 1.76dB, where N is the resolution of the data converter.

Typical IF sampling ADCs have IF inputs between 70MHz and 300MHz. The SNR requirement is generally between 60dB and 80dB shown by the circled area in the figure. Note that in order to obtain 80dB SNR for a 100MHz input, the total jitter should be no more than 0.125ps which represents extremely high performance.

Another consideration is that clock jitter adds on an rms basis. The total jitter of a number of series-connected gates is equal the root-sum-square of the jitter associated with each gate:

$$\text{TOTAL JITTER} = \sqrt{J_1^2 + J_2^2 + J_3^2 + \ldots}$$



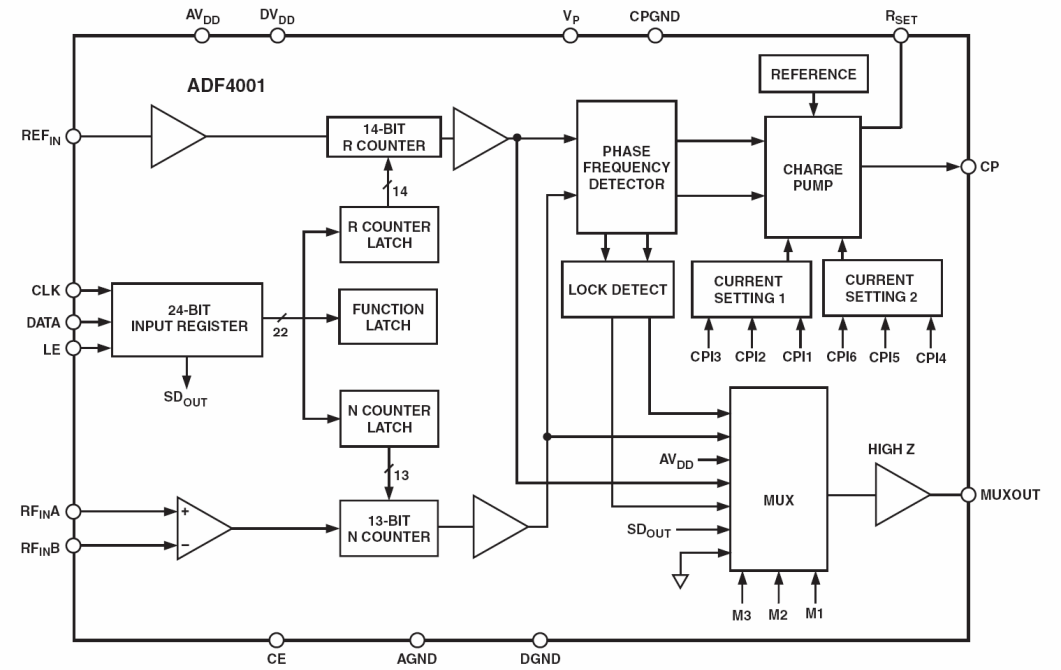
ADF4001 Converter Clock Test Setup

This figure shows a method of generating an ADC sampling clock using a PLL chip such as the ADF4001. The reference clock frequency is 10MHz, but in a GSM basestation it would be 13MHz. The ADF4001 is a clock generation PLL which operates up to 200MHz. It requires an external loop filter and VCO. The R-divider is set for 1, and the N-divider is set for 8 to produce the 80MHz output frequency. Note that in a GSM basestation, the ADC clock is typically 52MSPS. A VCXO rather than a VCO is used for lower phase noise.

The ADC in this application is the AD9215-80 10-bit, 80MSPS converter which has an SNR specification of 58dB. Since this is a baseband application, the maximum ADC input frequency is 40MHz. The SNR due to jitter should be at least 6dB better than the ADC SNR, or 64dB. From the equation on the previous page, SNR = $20\log_{10}[1/2\pi ft_j]$, the jitter corresponding to an SNR of 64dB and an input frequency of 40MHz is approximately 2.5ps.

The measured jitter of the PLL in the above circuit using the ADF4001 was 1.1ps rms, which is more than adequate for the 10-bit baseband application.

ADF4001 200MHz Clock Generator PLL



The ADF4001 clock generator can be used to implement clock sources for PLLs that require very low noise, stable reference signals as in the previous example. It consists of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, and a programmable 13-bit N counter. In addition, the 14-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete PLL (phase-locked loop) can be implemented if the synthesizer is used with an external loop filter and VCO (voltage controlled oscillator) or VCXO (voltage controlled crystal oscillator). The N minimum value of 1 allows flexibility in clock generation.

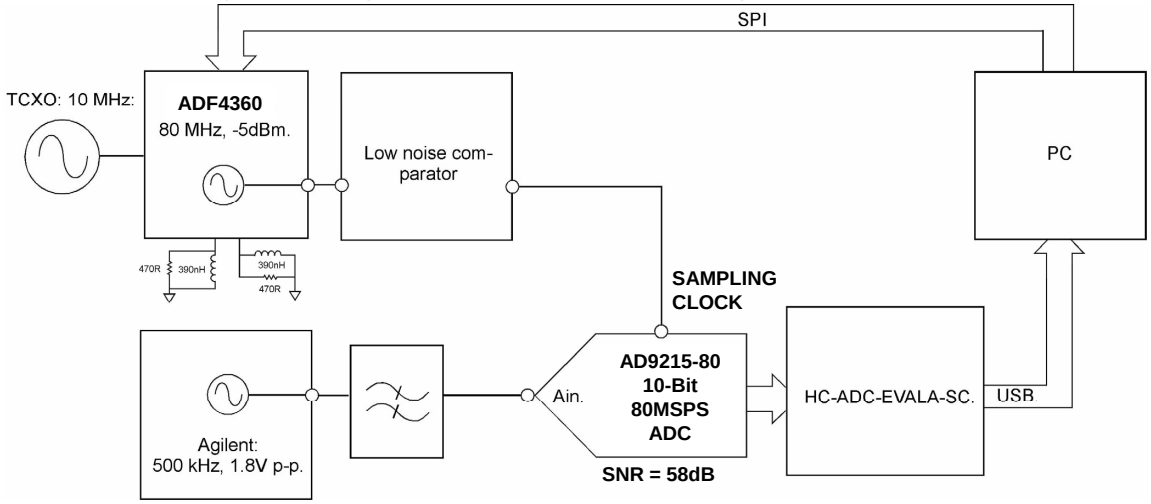
The ADF4001 has 200MHz bandwidth, operates on a 2.7V to 5.5V power supply, and has a hardware and software power-down mode.

There is a separate charge pump supply, VP, which allows extended tuning voltage in 5V systems.

The device has programmable charge pump currents and a simple 3-wire serial control interface.

Typical operating current is 4.5mA, and the part comes in either a 16-lead TSSOP or a 20-lead LFCSP.

Reducing the Complexity of Clocking at Baseband by Using ADF4360-8 Integrated PLL

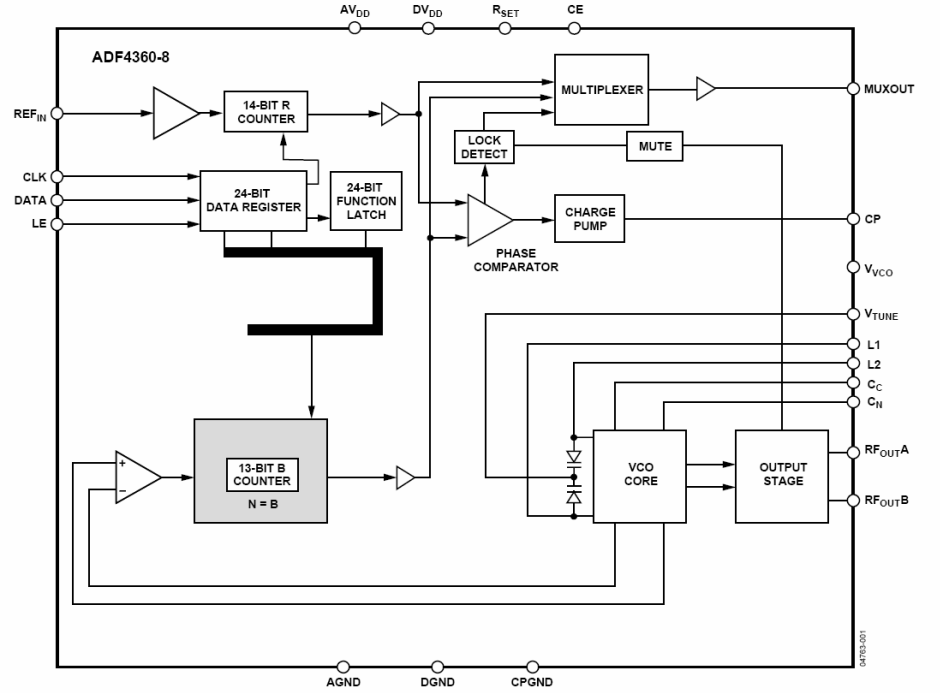


- **The ADF4360-8 integrates a VCO on-chip to further reduce cost and board space**
- **In this configuration, the ADF4360-based clock will produce 2.45 ps rms jitter. This is fine for most baseband applications.**

This baseband clock generator utilizes the ADF4360-8 to perform the PLL function. This is a simpler solution, because the ADF4360-series contains an integrated VCO. An external low noise comparator is used to boost the amplitude of the output of the ADF4360 to a level suitable for driving the ADC.

The measured jitter of this generator is 2.45ps which is approximately the system requirement for 64dB SNR (due to jitter only) with an input frequency of 40MHz. (See Figure 3.72).

ADF4360-8 Integrated Synthesizer and VCO Output: 65MHz to 400MHz



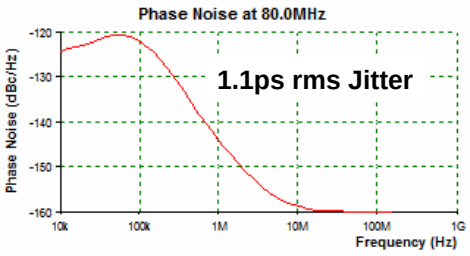
The ADF4360-8 is an integrated integer-N synthesizer and voltage controlled oscillator. The ADF4360-8 center frequency is set by external inductors. This allows a frequency range of between 65MHz and 400MHz.

Control of all the on-chip registers is through a simple 3-wire interface. The device operates with a power supply ranging from 3.0V to 3.6V and can be powered down when not in use.

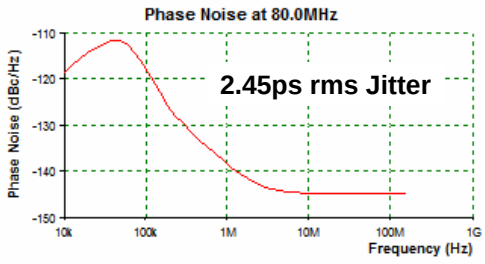
ADF4001/ADF4360-8 Jitter and Phase Noise

- **ADF4001 with external VCXO, 1.1ps rms jitter**
- **ADF4360-8, 2.45ps rms jitter**
- **Both meet min jitter requirement for many baseband sampling applications**
- **Simulations shown using ADI's free PLL/VCO design tool, ADIsimPLL found at www.analog.com/ADIsimPLL**
- **The ADF4002 increases usable output bandwidth to 400MHz compared to 200MHz on the ADF4001.**

ADF4001



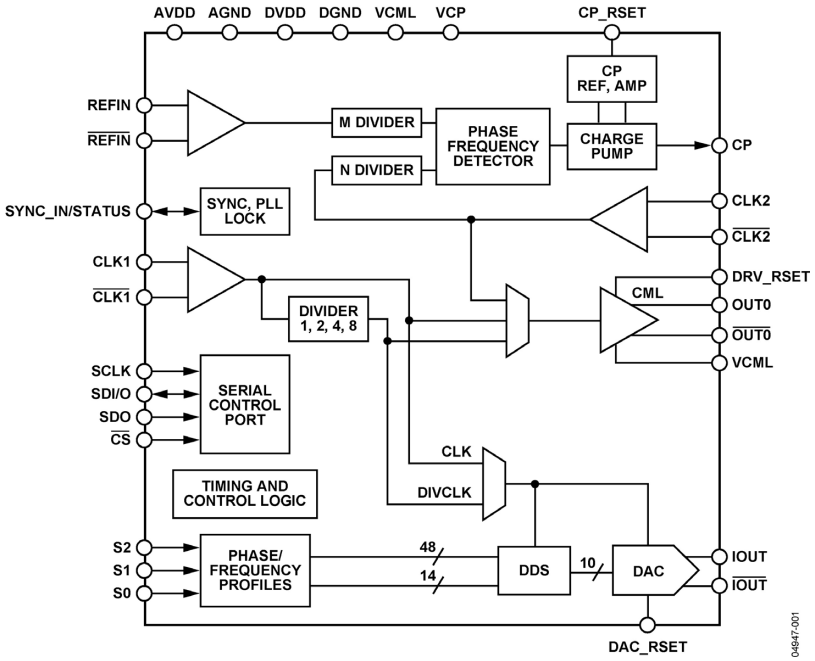
ADF4360-8



This figure compares the phase noise and jitter performance of the ADF4001 design (external VCXO) and the ADF4360-8 design (internal VCO). Both approaches meet the jitter requirement for many baseband sampling applications.

The ADF4002 is similar to the ADF4001, but increases the usable output bandwidth to 400MHz compared to 200MHz for the ADF4001.

AD9540 655 MHz Low Jitter Clock Generator



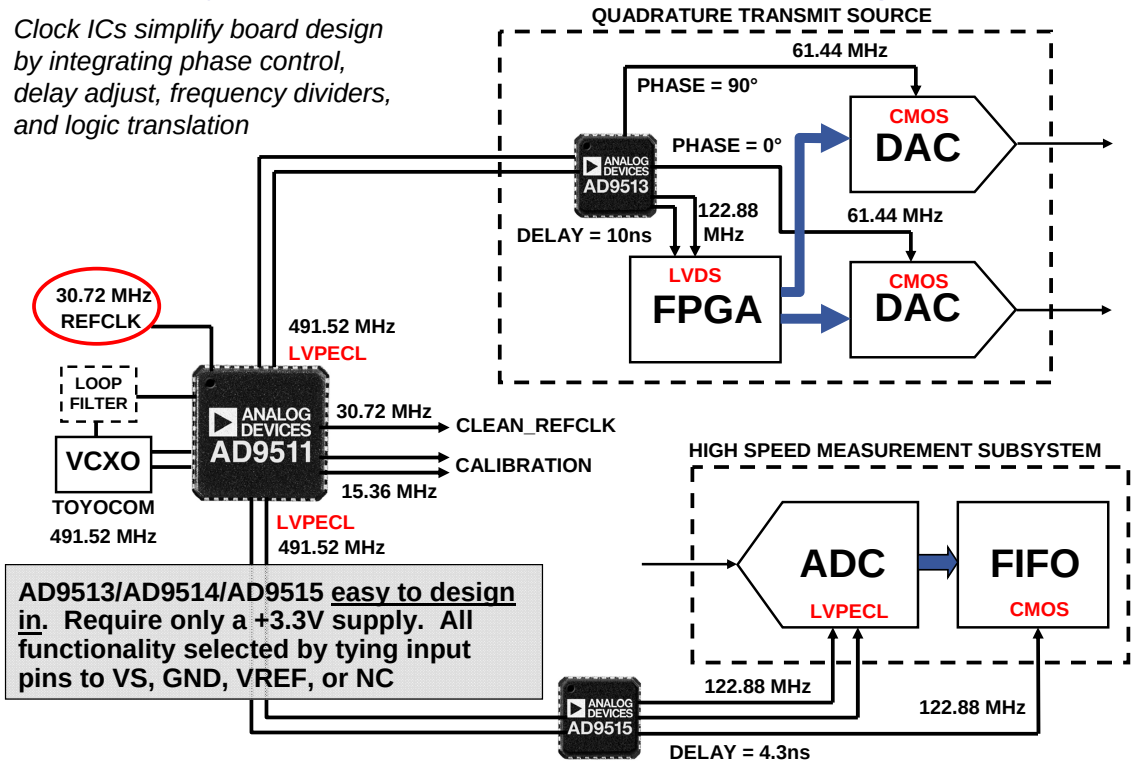
The AD9540 is Analog Devices' first dedicated clocking product specifically designed to support the extremely stringent clocking requirements of the highest performance data converters. The device features high performance PLL (phase-locked loop) circuitry, including a flexible 200MHz phase frequency detector and a digitally controlled charge pump current.

The device also provides a low jitter (720fs), 655MHz CML-mode), PECL-compliant output driver with programmable slew rates. External VCO rates up to 2.7GHz are supported. Extremely fine tuning resolution (steps less than 2.33µHz) is another feature supported by this device.

Information is loaded into the AD9540 via a serial I/O port that has a device write speed of 25Mbps. The AD9540 frequency divider block can also be programmed to support a spread spectrum mode of operation. The AD9540 is specified to operate over the extended automotive range of −40°C to +85°C.

System Clock Distribution Examples

Clock ICs simplify board design by integrating phase control, delay adjust, frequency dividers, and logic translation



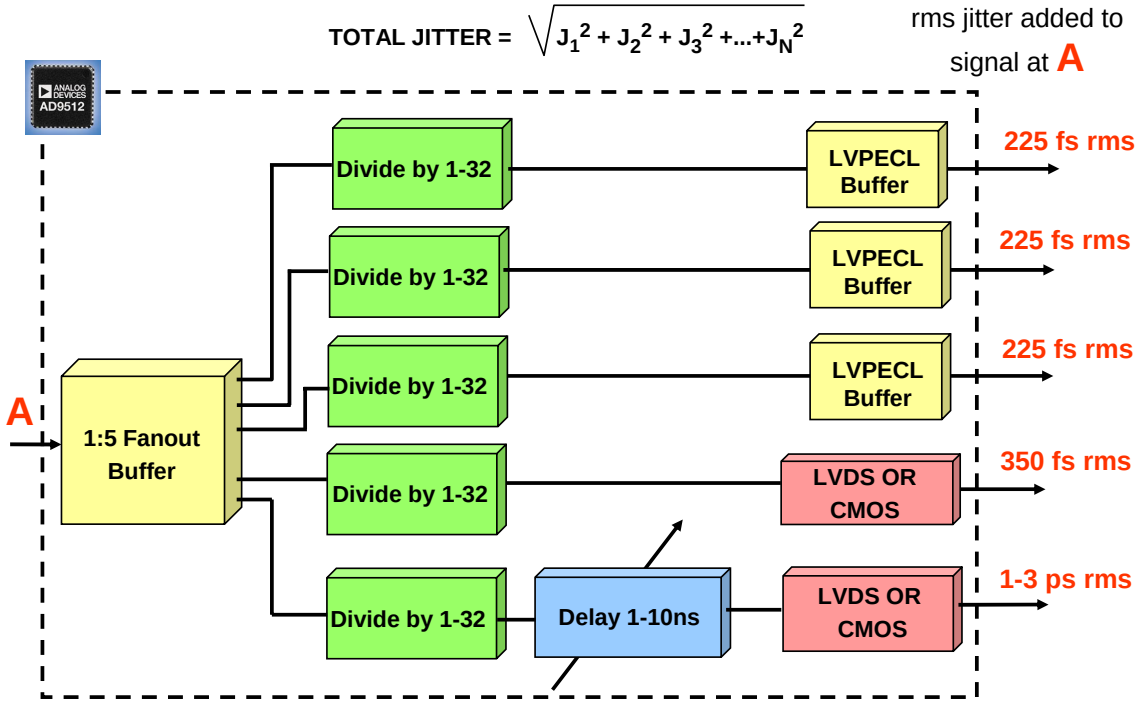
This figure illustrates a typical system clock generation and distribution application. The system reference clock is 30.72MHz and circled on the left. The PLL function of the AD9511 IC is used to generate a "clean" low jitter 491.52MHz clock from the reference clock. Note that the loop filter and the VCXO are external to the AD9511.

One of the 491.52MHz low voltage PECL (LVPECL—see footnote below) outputs is sent to the AD9515 clock distribution IC which contains two programmable divider channels (1 to 32) with a coarse delay adjustment in one channel. The AD9615 is used as the clock distribution chip for the high speed measurement system. The dividers are set to divide by 4 to generate the 122.88MHz sampling clock to the ADC and the data strobe to the FIFO. Note that the delay is set for 4.3ns in the FIFO strobe such that the ADC data is clocked into the FIFO at the proper time. The ADC is clocked with the LVPECL output, and the second output (with the delay) is set to generate a CMOS logic level for the FIFO. The additive jitter of the AD9515 is approximately 300fs.

A second 491.52MHz LVPECL output from the AD9511 is used as the master clock for the quadrature transmit source. It drives an AD9513 clock distribution IC which contains three divider channels (1 to 32), one of which includes a delay adjustment. In this application, the delay adjustment is used to properly time the 122.88MHz clock to the FPGA by introducing a delay of 10ns. The other two channels in the AD9513 are set to divide by 8 to generate the 61.44MHz clocks for the DACs. The coarse phase adjustment in the AD9513 is used to generate the 90° phase shift between the I/Q DAC clocks. The additive jitter of the AD9513 is approximately 300fs.

LVPECL is basically ECL logic operated between ground V_S = +3.3V. Under these conditions, a logic "1" is approximately V_S – 0.96V = +2.34V and a logic "0" is approximately V_S – 1.76V = +1.54V with 50Ω terminations to V_S – 2V = +1.3V.

AD9512 1.2GHz Clock Distribution IC



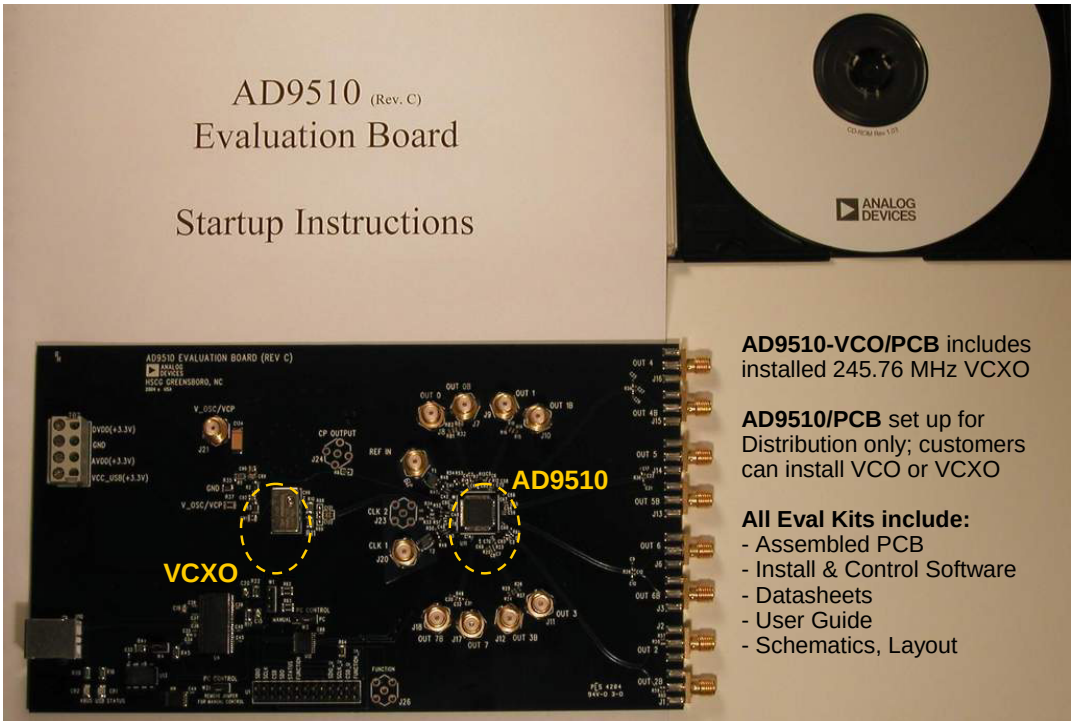
The AD9512 1.2GHz clock distribution IC provides a multi-output clock distribution in a design that emphasizes low jitter and low phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements can also benefit from this part. There are five independent clock outputs. Three outputs are LVPECL (1.2GHz), and two are selectable as either LVDS (800MHz) or CMOS (250MHz) levels.

Each output has a programmable divider that may be bypassed or set to divide by any integer up to 32. The phase of one clock output relative to another clock output may be varied by means of a divider phase select function that serves as a coarse timing adjustment. There is a small jitter penalty when using the variable phase output.

One of the LVDS/CMOS outputs features a programmable delay element with a range of up to 10 ns of delay. This fine tuning delay block has 5-bit resolution, giving 32 possible delays from which to choose. The AD9512 is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

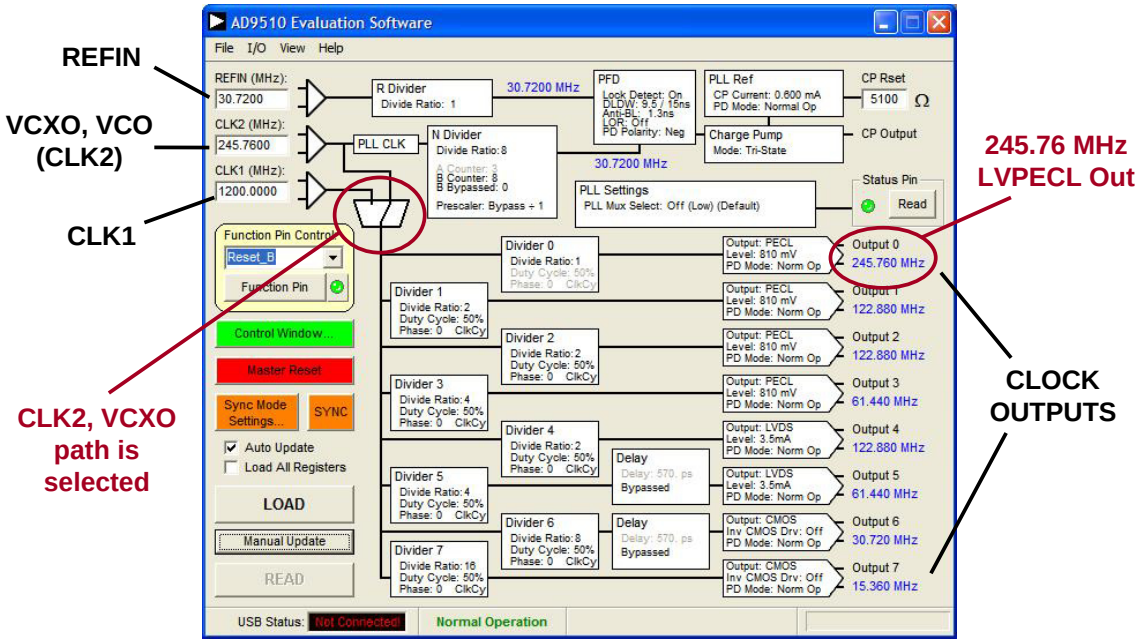
The AD9512 is available in a 48-lead LFCSP and can be operated from a single 3.3 V supply. The temperature range is −40°C to +85°C.

Clock Evaluation Kits



The Analog Devices' clock generator and distribution products have a complete set of evaluation boards. This shows the board for the AD9510 which includes an installed 245.76MHz VCXO. The board can also be set up for a user-installed VCO or VCXO.

Clock Evaluation Board User Interface Is Intuitive; Looks Like Block Diagram of Chip



The clock evaluation board software has an intuitive user interface as shown here. The screen format follows the block diagram of the individual chip for ease of use.

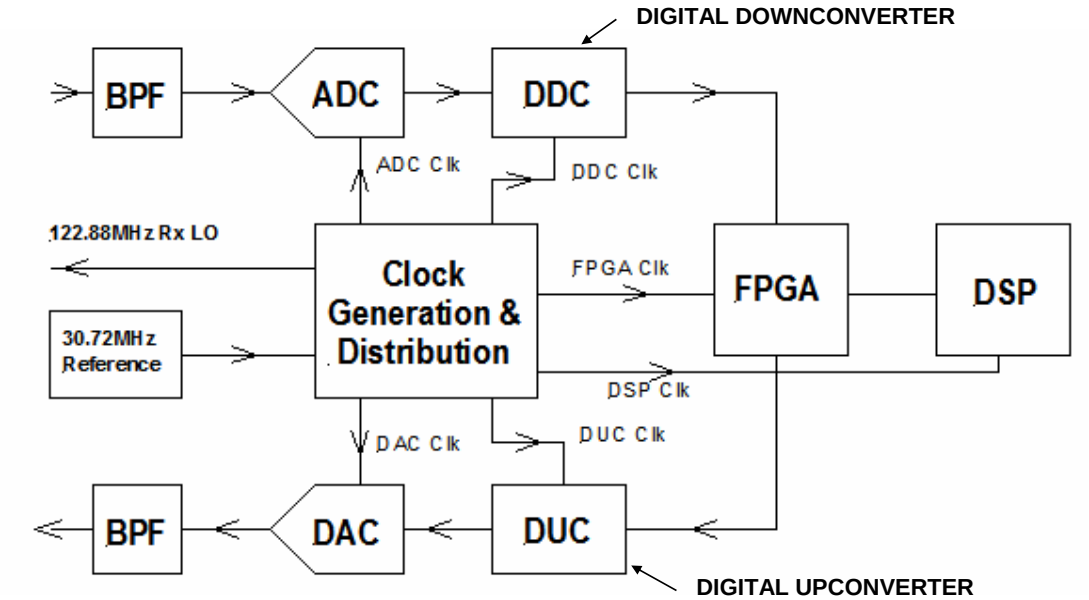
ADIsimCLK Design and Simulation Software

Free download from ADI website @ www.analog.com/clocks

The ADIsimCLK design and simulation software is designed to aid in the application of the clock product families.

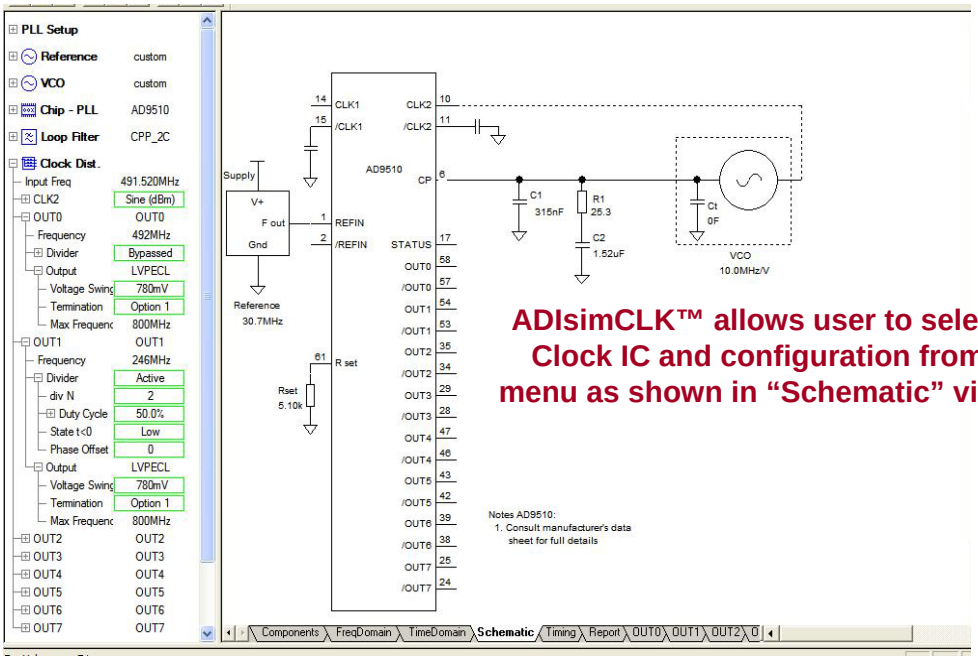
Because many of the clock products contain PLLs, ADIsimCLK makes use of a large portion of ADIsimPLL for the PLL part of the design.

ADIsimCLK Design Block Diagram



This shows a block diagram of the design interface for ADIsimCLK.

ADIsimCLK Is Schematic Driven



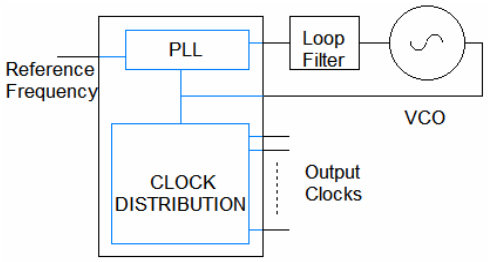
ADIsimCLK™ allows user to select Clock IC and configuration from menu as shown in “Schematic” view

The ADIsimCLK program is schematic driven and allows the user to select the clock IC and the configuration from the menu when in the "schematic" view.

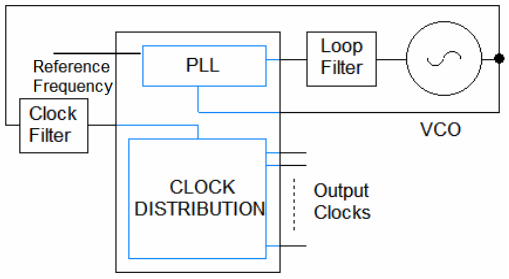
Data in the table on the left can be modified and the results displayed instantaneously in the "results" table, similar to the ADIsimPLL program.

ADIsimCLK Configuration Options

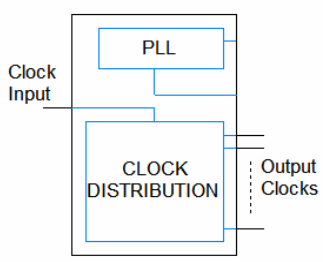
(A) INTEGRATED PLL WITH CLOCK CLEANUP, FREQUENCY TRANSLATION AND CLOCK DISTRIBUTION



(B) ADDING AN EXTERNAL FILTER TO (A) FOR LOWER PHASE NOISE



(C) CLOCK DISTRIBUTION CIRCUIT ONLY



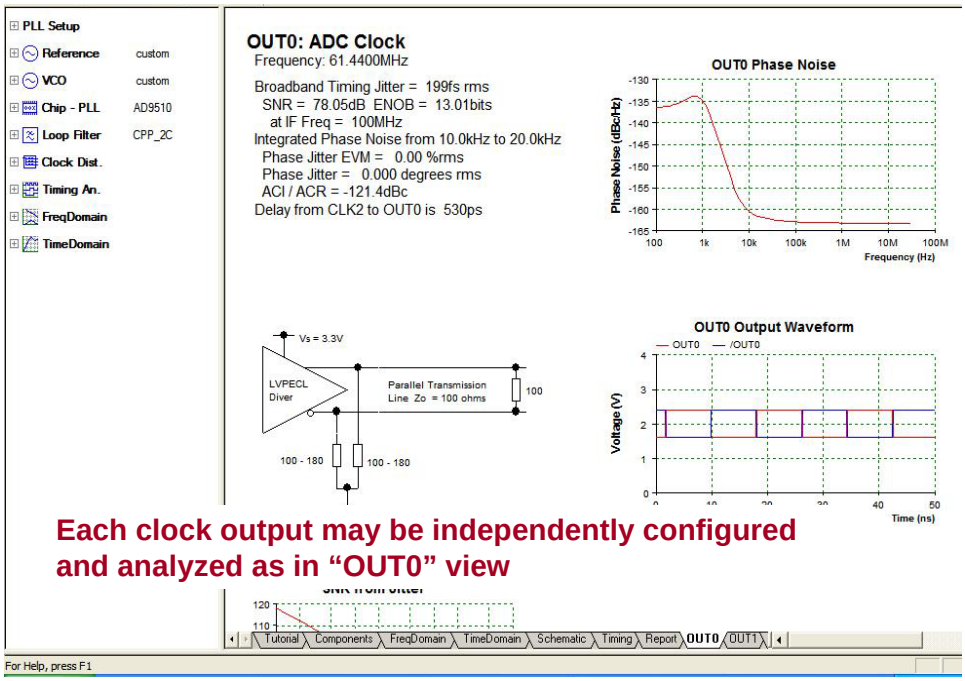
This shows the three basic configuration options currently available with ADIsimCLK.

The (A) configuration is for a clock generation product with an integrated PLL and clock distribution circuit.

The (B) configuration allows the addition of an external filter to the PLL output for lower phase noise and jitter.

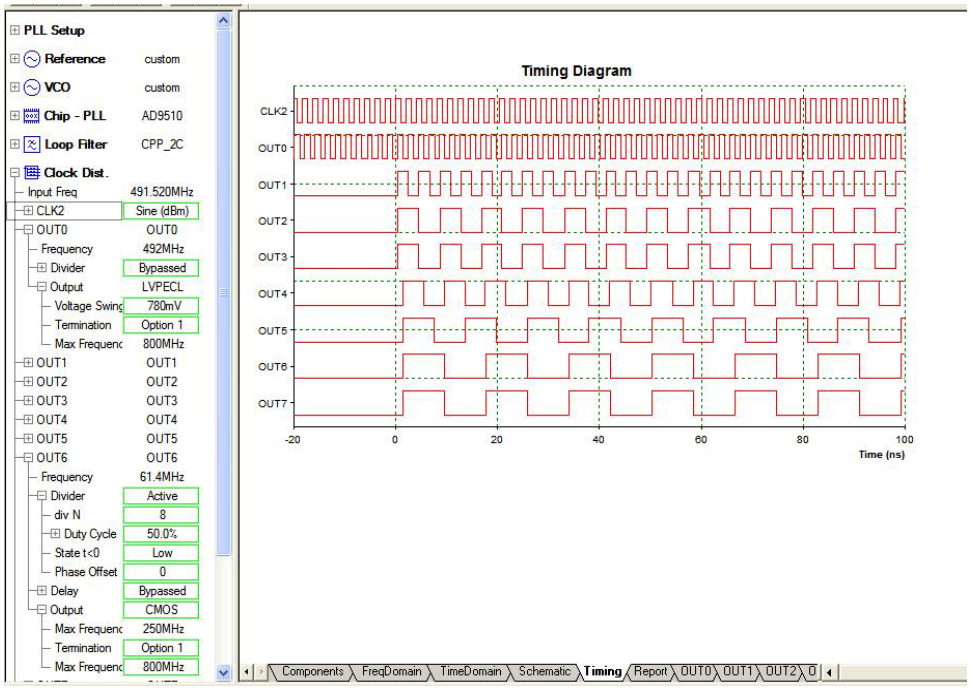
The (C) configuration is for distribution products only.

ADIsimCLK Outputs



The various outputs of the clock product can be independently configured and analyzed as shown here.

Relative Timing of All Clocks Is Available in the "Timing" View



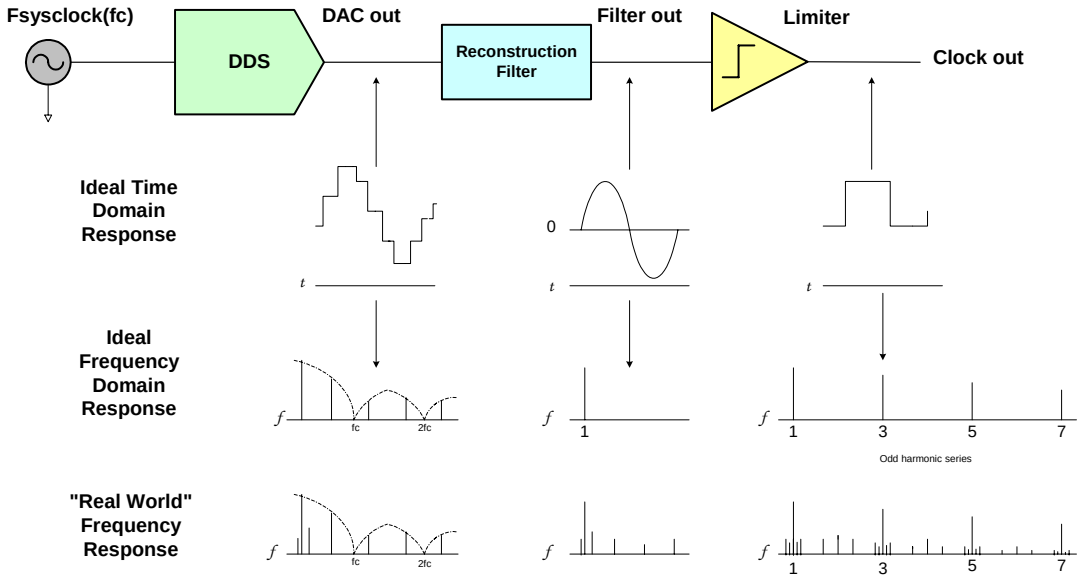
The relative timing of all the clocks associated with a particular clock IC is available in the "timing" view as shown here.

Generating Low Jitter Clocks Using DDS Systems

Reference:

David Brandon, "Direct Digital Synthesizers in Clocking Applications," Application Note AN-823, Analog Devices, 2006

Generating Clocks from a DDS



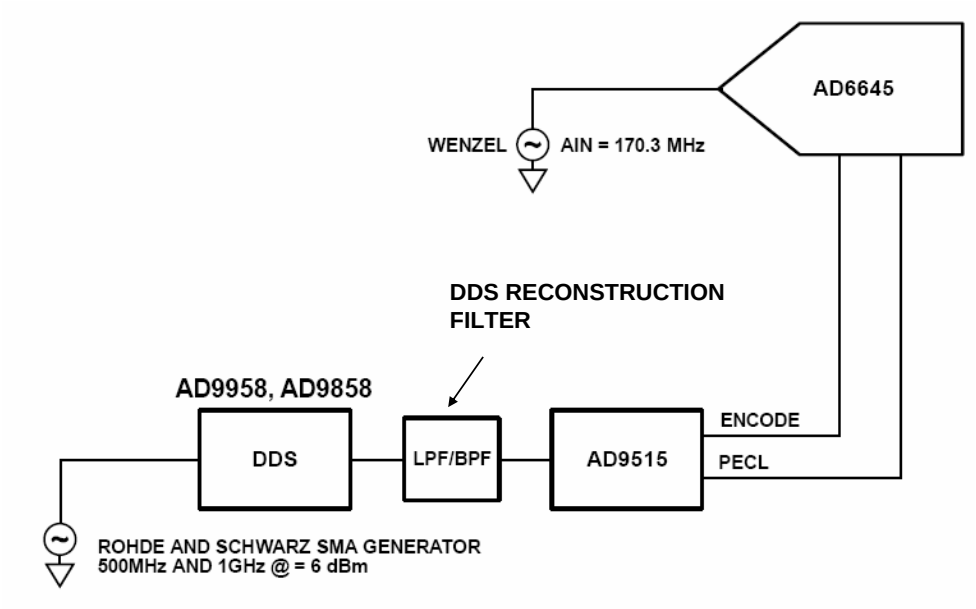
The DDS chip can synchronize to a user's reference. An on-chip clock multiplier can generate the fast clock needed to clock the NCO/DAC. A frequency tuning word may be written to set the output clock rate. External filtering removes unwanted images. A squaring function then converts sine wave to square wave.

The primary challenge in using DDS systems for clock generation is reducing the time jitter that is generated due to the discrete spurious components that are present on the DDS output signal. These spurious components are primarily due to the quantized nature of the DDS output signal and the phase noise produced because of phase truncation within the DDS.

This figure shows time and frequency domain representations at each point in the process. A real-world representation of the frequency domain is shown at the bottom of the figure. This response contains aliases of higher order harmonics of the output signal which fall close to the desired output signal, and filtering becomes difficult.

The overall quality of the final clock output of a DDS system is determined primarily by the filter and the limiter. AN-823 discusses the results of experiments conducted with a high performance DDS and clock distribution IC and shows the jitter associated with various filter configurations.

Test Set for Measuring Jitter of AD9958/AD9858 DDS Driving AD9515 Clock Distribution IC



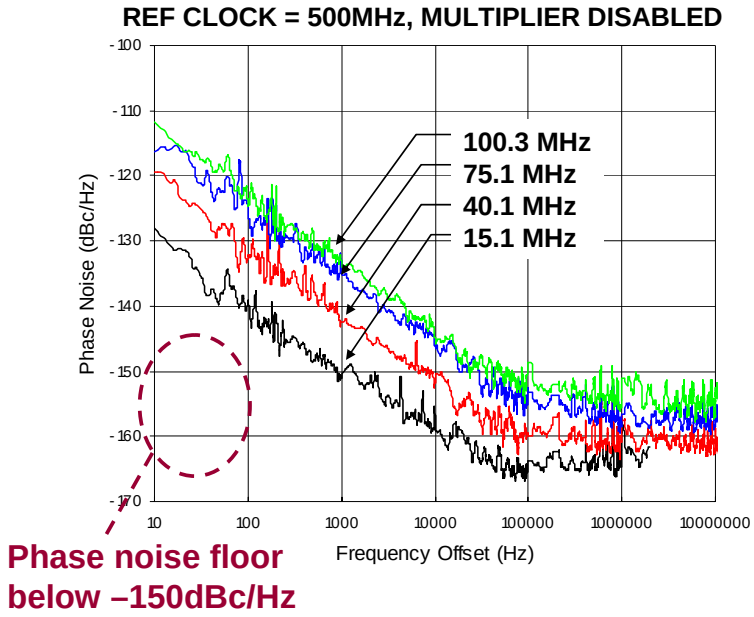
This is the basic test set used to measure the jitter performance of the AD9958/AD9858 DDS driving the AD9515 clock distribution IC. The jitter is calculated by FFT analysis of the AD6645 14-bit output data using the relationship between SNR and jitter,

$$SNR = 20\log_{10}[1/2\pi ft_j].$$

The DDS sampling clock is derived from a Rohde and Schwarz SMA signal generator. Data was taken on two different DDSs, the AD9958 and the AD9858. The jitter measurement was made by using the clock derived by the DDS and the AD9515 as the sampling clock to the AD6645, a 14-bit, 100MSPS ADC.

The analog input to the ADC was derived from a Wenzel crystal oscillator (www.wenzel.com) known for its low jitter.

New DDS Chips Like the AD9958 Dual Channel and AD9959 Quad Have Very Low Phase Noise



Power dissipation <200mW per channel

This shows the phase noise of the AD9958 DDS chip with a reference clock of 500MHz. Output frequencies of 15.1MHz, 40.1MHz, 75.1MHz, and 100.3MHz are shown.

Note that the broadband phase noise floor is below –150dBc/Hz in all cases.

Application Note AN-823 Details Performance of AD9958 Driving AD9515

AN-823 shows jitter < 1 ps rms possible with proper filtering

Table 1. Jitter Response AD9958 and AD9515 vs. Fout, Power, Frequency and Filter BW

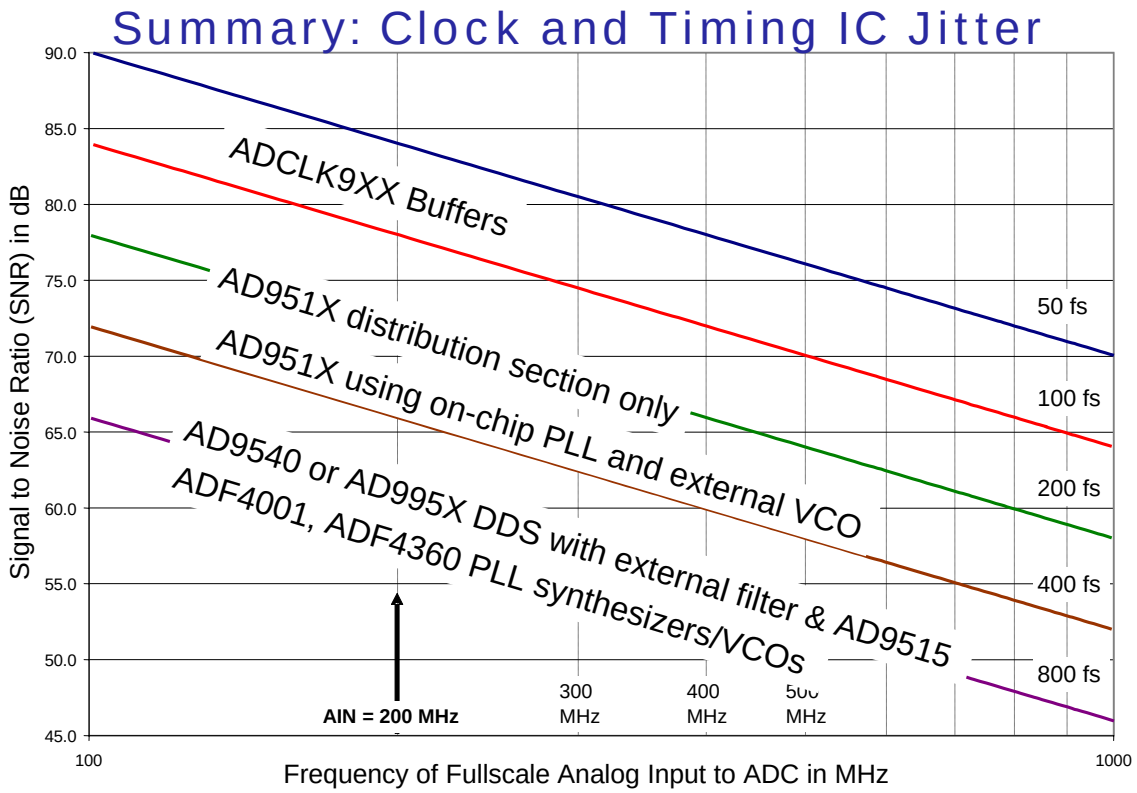
Product	DDS Sample Rate (MHz)	DDS Output Frequency (MHz)	DDS Output Power (dBm)	DDS Reconstruction Filter (MHz)	AD9515 Divider Output Setting	AD9515 Output Frequency (MHz)	Jitter (rms) (ps)
AD9958/AD9515	500	38.88	–3.6	200 LPF	1	38.88	4.1
AD9958/AD9515	500	38.88	–3.6	200 LPF	2	19.44	4.1
AD9958/AD9515	500	38.88	–4.7	47 LPF	1	38.88	2.4
AD9958/AD9515	500	38.88	–4.7	47 LPF	2	19.44	2.4
AD9958/AD9515	500	38.88	–3.3	5% BPF	1	38.88	1.5
AD9958/AD9515	500	38.88	–3.3	5% BPF	2	19.44	1.5
AD9958/AD9515	500	77.76	–3.8	200 LPF	1	77.76	2.5
AD9958/AD9515	500	77.76	–3.8	200 LPF	2, 4	38.88, 19.44	2.5
AD9958/AD9515	500	77.76	–4.9	85 LPF	1	77.76	1.5
AD9958/AD9515	500	77.76	–4.9	85 LPF	2, 4	38.88, 19.44	1.5
AD9958/AD9515	500	77.76	–3.8	5% BPF	1	77.76	1.1
AD9958/AD9515	500	77.76	–3.8	5% BPF	2, 4	38.88, 19.44	1.1
AD9958/AD9515	500	155.52	–5.5	200 LPF	2	77.76	1.5
AD9958/AD9515	500	155.52	–5.5	200 LPF	4, 8	38.88, 19.44	1.5
AD9958/AD9515	500	155.52	–5.6	5% BPF	2	77.76	0.68
AD9958/AD9515	500	155.52	–5.6	5% BPF	4, 8	38.88, 19.44	0.68

This table shows the jitter of the final output clock for various DDS output frequencies, AD9515 divider settings, and reconstruction filter characteristics.

Note that the lowest jitter is obtained when the reconstruction filter is a bandpass filter having a bandwidth equal to approximately 5% of the DDS output frequency. This obviously limits the tuning range of the DDS, however.

Wider filter bandwidths allow wider tuning ranges, at the expense of increased jitter. For further details of the results of these experiments, consult the application note.

David Brandon, "Direct Digital Synthesizers in Clocking Applications," Application Note AN-823, Analog Devices, 2006.



This figure summarizes the current jitter performance of the various IC solutions discussed in this section. The new ADCLK9xx family of clock buffers from Analog Devices are designed with additive jitter less than 100fs.