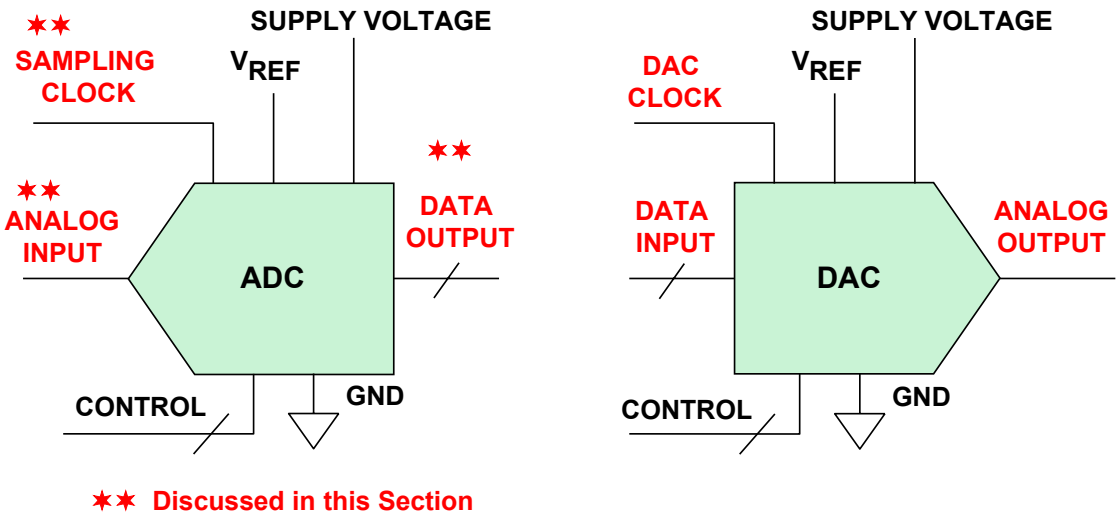
# High Speed System Applications





## SECTION 2
## OPTIMIZING DATA CONVERTER INTERFACES

# Data Converter Interface Overview




This figure shows the critical interfaces to an ADC or DAC:

Analog Input/Output
Sampling Clock/DAC Clock
Data Output/Input

The reference voltage, supply voltages, and ground are also important. Section 4 of this book will address the issues associated with grounding and decoupling, and this section discusses the ones listed above.

This section concentrates on ADCs; however, the same interface concepts apply equally to DACs, some of which are discussed in Section 3.

# General Trends in Data Converters Affecting Interface Design

- **Higher sampling rates, higher resolution**
- **Excellent ac performance**
- **Single-supply operation (e.g., +5V, +3V, +2.5V, +1.8V)**
- **Smaller input/output signal swings**
- **Differential inputs/outputs**
- **More sensitivity to noise**
- **Lower power, shutdown or sleep modes**
- **Maximize usage of low cost foundry CMOS processes**
- **Small surface mount packages**

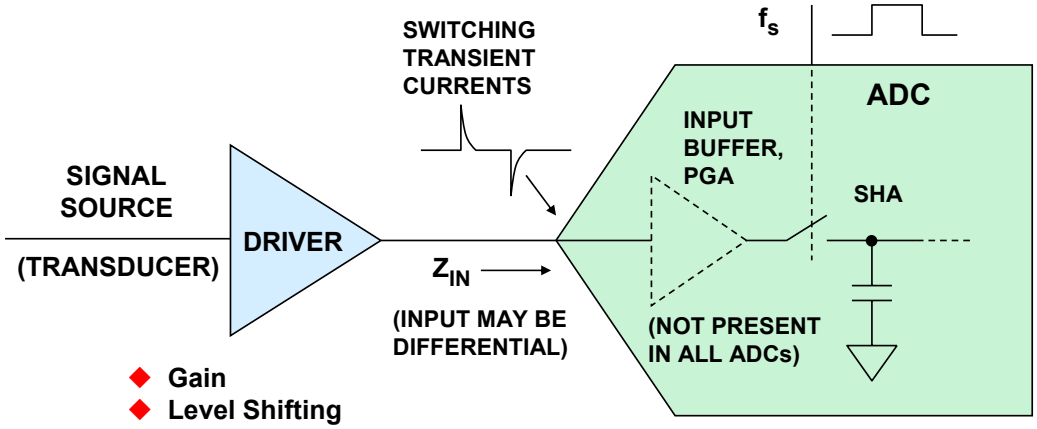
Several issues have complicated the design of data converter interfaces in recent years. The primary one is the trend to lower voltage, lower power, single-supply ICs which reduce signal swings proportionally. Smaller signal swings make modern data converters more sensitive to noise, grounding, and decoupling.

Many ADCs are now designed with differential inputs to reduce sensitivity to noise and also to get more signal swing for a given supply voltage. Selecting the proper drive amplifier is more complex because not only must it have differential outputs, but many times it must convert a single-ended signal to a differential one as well as perform a level shifting function to match the common-mode input voltage of the ADC.

These factors, added to the increased demand for higher sampling rates, resolutions, and excellent ac performance, make proper analog interface design critical to achieving the desired system performance.

# Driving the ADC Analog Input

# ADC Analog Inputs Are Not Ideal and Require Suitable Drivers




- Gain
- Level Shifting
- Isolation from Signal Source
- Impedance Transformation
- Single-Ended to Differential Conversion

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- Driver Should Not Degrade DC or AC Performance of ADC
- A Few ADCs Are Designed to Interface Directly with Transducers (Some Σ-Δ and SAR ADCs)

An ideal ADC analog input circuit would have a constant resistive input impedance (in most cases, the resistance is several kΩ, but a few ADCs are designed with lower impedances) and an input range compatible with the signal source. Practical ADCs, however, present a finite complex (real and reactive components) input impedance to the driver, and may have transient currents on the input which are due to the switching action of the sample-and-hold function in the converter.

The input of the ADC may be buffered internally to minimize these transients, but CMOS ADCs typically do not have the input buffer.

With no internal buffer, an external driver may be required to isolate the signal source from the ADC input. When subjected to the transient currents, the driver must settle to the required accuracy in an interval that is less than approximately equal to one-half the sampling clock period.

The external ADC driver may be required to perform other functions such as gain, level shifting, single-ended to differential conversion, as well as isolating the signal source from the ADC input.

The external driver should be selected so that it does not degrade either the ac or dc performance of the ADC.

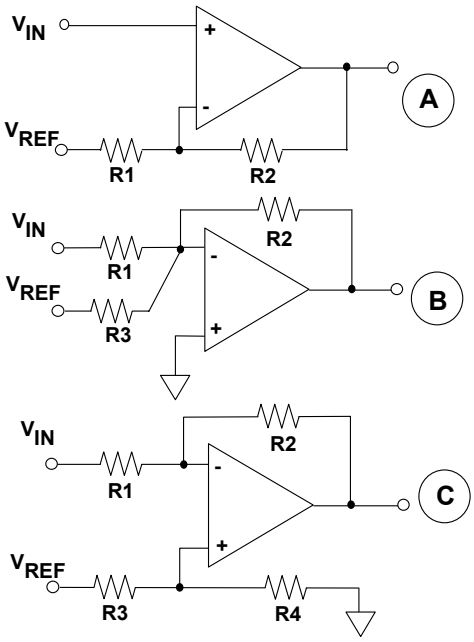
The bandwidth of the driver is generally very high in order to keep distortion low; therefore, some noise filtering between the driver and the ADC is generally desirable.

However, one should not automatically assume that an external driver is required because a few ADCs are designed to interface directly with transducers (primarily some sigma-delta and SAR ADCs).

In any event, the ADC data sheet must be carefully studied to understand what type of analog input driver is suitable if one is required.

# Single-Ended DC-Coupled Amplifier Drivers for ADCs

# Op Amp Gain and Level Shifting Circuits




$$V_{out} = \left(1 + \frac{R2}{R1}\right) V_{in} - \frac{R2}{R1} V_{ref}$$

$$\text{NOISE GAIN} = 1 + \frac{R2}{R1}$$

$$V_{out} = -\frac{R2}{R1} V_{in} - \frac{R2}{R3} V_{ref}$$

$$\text{NOISE GAIN} = 1 + \frac{R2}{R1||R3}$$

$$V_{out} = -\frac{R2}{R1} V_{in} + \left(\frac{R4}{R3 + R4}\right)\left(1 + \frac{R2}{R1}\right) V_{ref}$$

$$\text{NOISE GAIN} = 1 + \frac{R2}{R1}$$

In dc-coupled applications, the drive amplifier may be required to provide gain and offset voltage, to match the signal to the input voltage range of the ADC. This figure summarizes various op amp gain and level shifting options. The circuit of A operates in the non-inverting mode, and uses a low impedance reference voltage, $V_{REF}$, to offset the output. Gain and offset interact according to the equation:

$$V_{OUT} = [1 + (R2/R1)] \bullet V_{IN} - [(R2/R1) \bullet V_{REF}].$$

The circuit in B operates in the inverting mode, and the signal gain is independent of the offset. The disadvantage of this circuit is that the addition of R3 increases the noise gain, and hence the sensitivity to the op amp input offset voltage and noise. The input/output equation is given by:

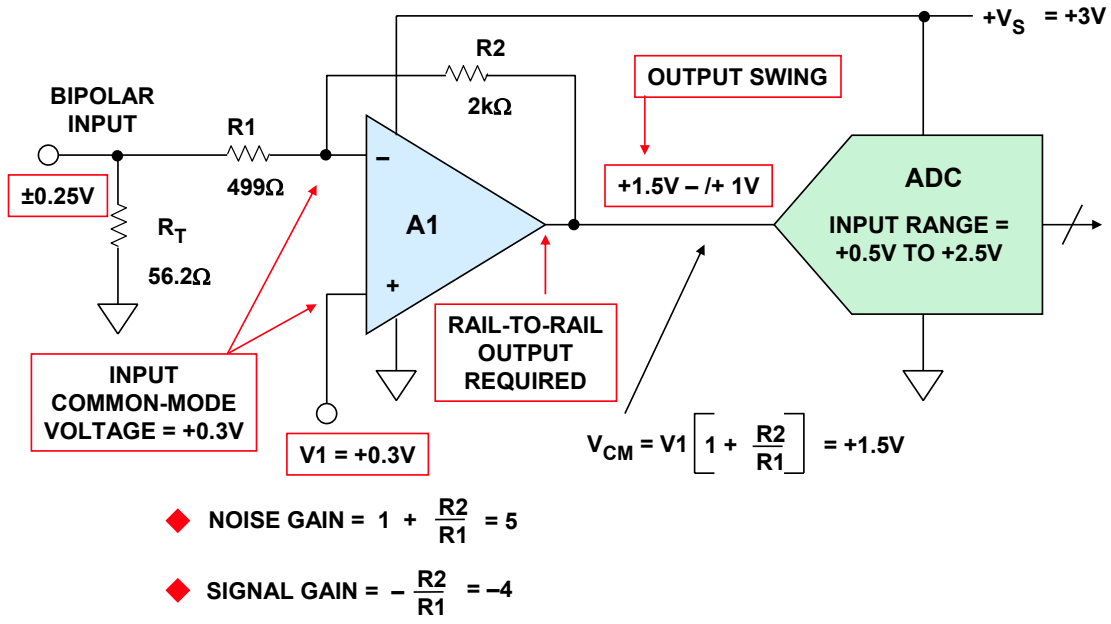
$$V_{OUT} = -(R2/R1) \bullet V_{IN} - (R2/R3) \bullet V_{REF}.$$

The circuit in C also operates in the inverting mode, and the offset voltage $V_{REF}$ is applied to the non-inverting input without noise gain penalty. This circuit is also attractive for single-supply applications ($V_{REF} > 0$). The input/output equation is given by:

$$V_{OUT} = -(R2/R1) \bullet V_{IN} + [R4/(R3+R4)][\,1 + (R2/R1)] \bullet V_{REF}.$$

Note that the circuit of A is sensitive to the impedance of $V_{REF}$, unlike the counterparts in B and C. This is because the signal current flows into/from $V_{REF}$, due to $V_{IN}$ operating the op amp over its common-mode range. In the other two circuits the common-mode voltages are fixed, and no signal current flows in $V_{REF}$. However, a dc current flows from the reference in B and C, so the output impedance of the reference must be added to R3 in performing the calculations.

# Single-Ended Level Shifter with Gain Requires Rail-to-Rail Op Amp




This circuit represents a typical single-supply ADC driver interface example. The is ideally suited to a single-supply level shifter and is similar to C shown in the previous figure. It will now be examined further in light of single-supply and common-mode issues. This figure shows the amplifier driving an ADC with an input range of +0.5V to +2.5V. Note that the entire circuit must operate on a single +3V supply.

The input range of the ADC (+0.5V to +2.5V) determines the output range of the A1 op amp. In order to drive the signal to within 0.5V of each rail, a rail-to-rail output stage is required. The signal gain of the op amp is set to 4, thereby amplifying the 0.5V p-p input signal to 2V p-p.

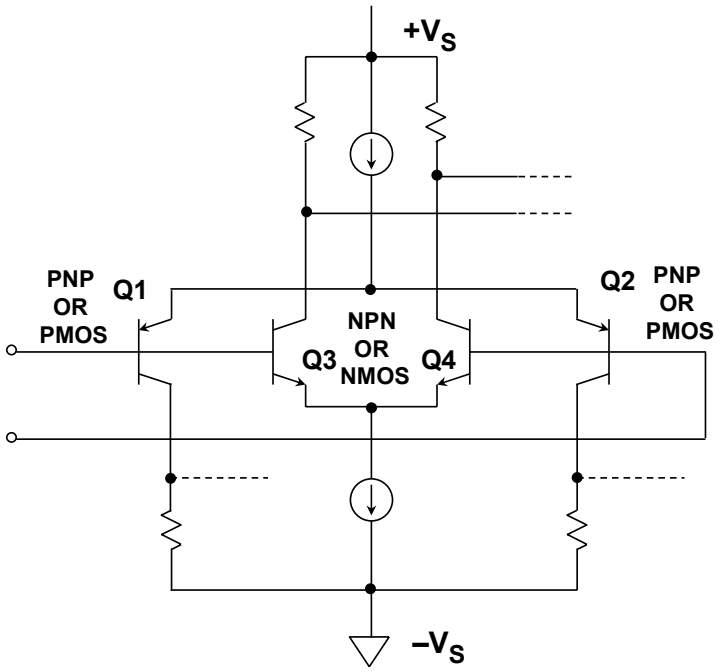
The input common-mode voltage of A1 is set at +0.3V which generates the required output offset of +1.5V. This produces the +1.5V offset when the bipolar input signal is at 0V. Note that some non rail-to-rail single-supply op amps can accommodate this input common-mode voltage when operating on a single +3V supply; however, the amplifier data sheet must be consulted.

This relatively simple circuit is an excellent example of where careful analysis of dc voltages is invaluable to the amplifier selection process.

Note that there will usually be some noise filtering between the amplifier output and the ADC input, but this will be discussed in more detail later.

An understanding of rail-to-rail input and output structures is needed to select the proper drive amplifier, and this discussion follows.

# A True Rail-to-Rail Input Stage




A simplified diagram of what has become known as a true rail-to-rail input stage is shown in this figure. Note that this requires use of two long tailed pairs, one of PNP bipolar transistors Q1-Q2, the other of NPN transistors Q3-Q4. Similar input stages can also be made with CMOS or JFET differential pairs.

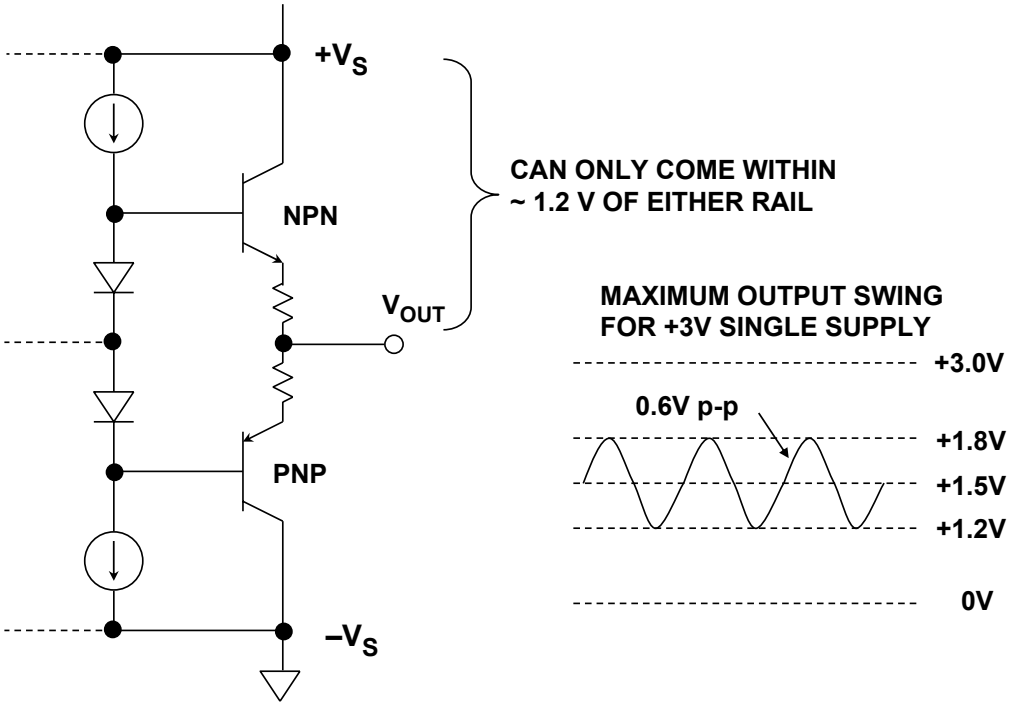
The NPN pair is operational when the input common-mode voltage is at or near the positive rail, and the PNP pair is operational when the input common-mode voltage is at or near the negative rail.

Rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair, somewhere along the input common-mode voltage range. Where this transition region occurs depends upon the particular amplifier design under consideration. Some have it set near the positive rail, some near mid-supply, and some near the negative rail. Some have an externally programmable transition region.

When the common-mode voltage is in the transition region, the input bias current will most likely change value and direction, and the common-mode rejection may be degraded. Other specifications may also be affected (such as the offset voltage), so the data sheet of the amplifier must be carefully studied to ensure that this is not a problem for the required system common-mode operating voltage.

At this point it should be noted that not all single-supply op amps are rail-to-rail.

# Popular Op Amp Output Stage

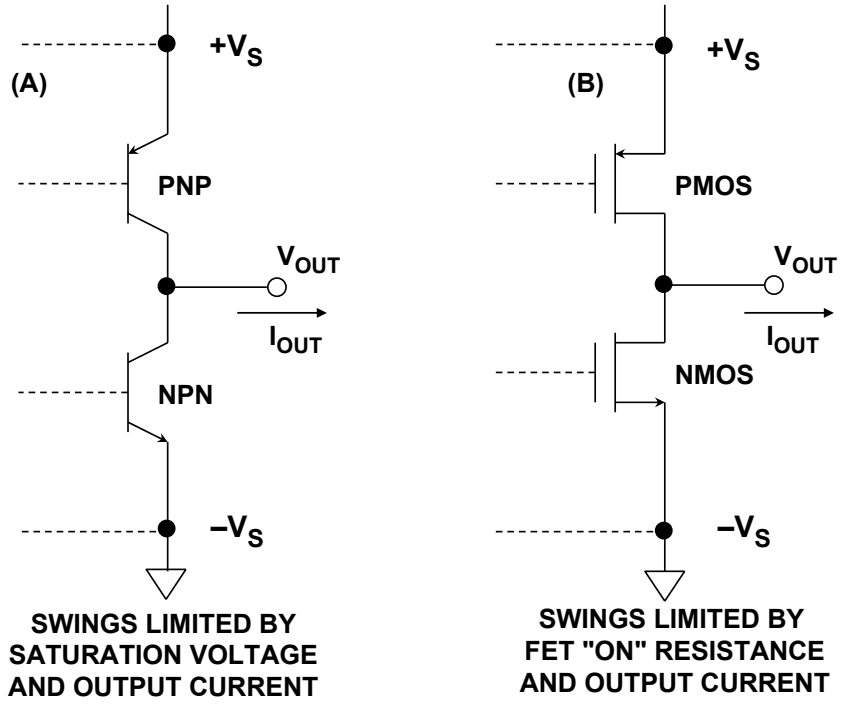



We will now examine output stages of op amps. This is a standard emitter-follower (common collector) output used in complementary bipolar processes. It has low output impedance and is relatively insensitive to capacitive loading.

However, the output can go no closer than about 1.2V to each supply rail. The headroom requirement can be even greater than 1.2V for some op amps which use this output structure, depending on the design.

On low supply voltages, such as 3V, this stage has only 0.6V peak-to-peak output voltage swing, centered on a common-mode voltage of +1.5V. In a very few applications (especially in differential output amplifiers) this swing may be adequate. In most single-ended applications, however, more signal swing is required.

## "Almost" Rail-to-Rail Output Stages




The complementary common-emitter/common-source output stages shown in A and B allow the op amp output voltage to swing much closer to the rails, but these stages have much higher open-loop output impedance than do the emitter follower-based stages previously discussed.

In practice, however, the amplifier's high open-loop gain and the applied feedback can still produce an application with low output impedance (particularly at frequencies below 10Hz). What should be carefully evaluated with this type of output stage is the loop gain within the application, with the load in place. Typically, the op amp will be specified for a minimum gain with a load resistance of 10kΩ (or more). Care should be taken that the application loading doesn't drop lower than the rated load, or gain accuracy may be lost.

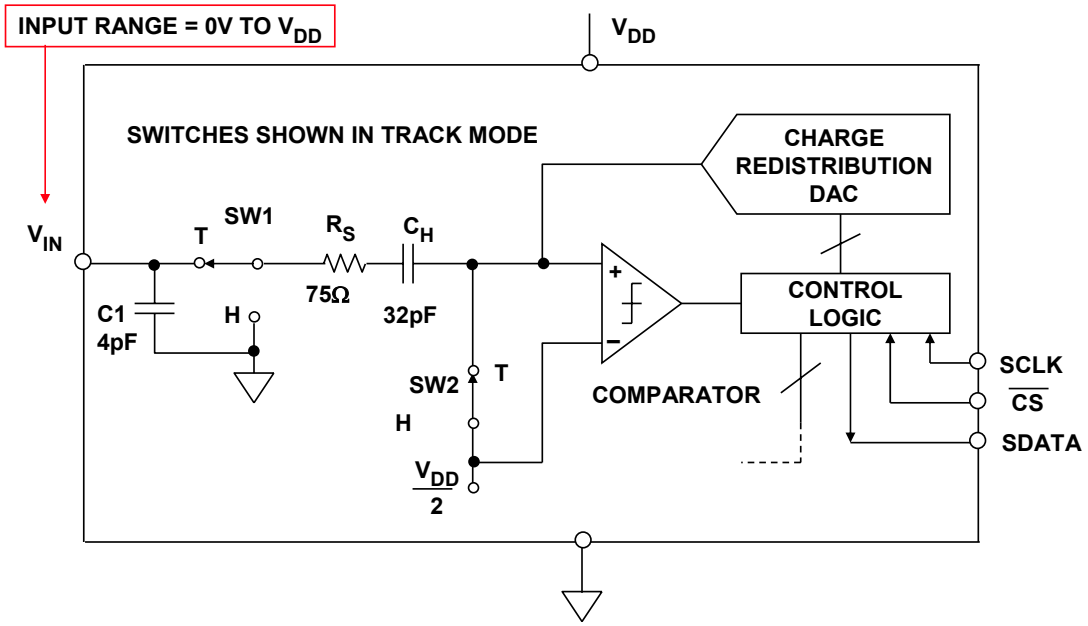
It should also be noted that these output stages will cause the op amp to be more sensitive to capacitive loading than the emitter-follower type. Again, this will be noted on the device data sheet, which will indicate a maximum of capacitive loading before overshoot or instability will be noted.

The complementary common emitter output stage using BJTs in A cannot swing completely to the rails, but only to within the transistor saturation voltage (VCESAT) of the rails. For small amounts of load current (less than 100μA), the saturation voltage may be as low as 5 to 10mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500mV at 50mA).

On the other hand, an output stage constructed of CMOS FETs as in B can provide nearly true rail-to-rail performance, but only under no-load conditions. If the op amp output must source or sink substantial current, the output voltage swing will be reduced by the I·R drop across the FET's internal "on" resistance. Typically this resistance will be on the order of 100Ω for precision amplifiers, but it can be less than 10Ω for high current drive CMOS amplifiers.

For the above basic reasons, it should be apparent that there is no such thing as a true rail-to-rail output stage, hence the title "Almost" Rail-to-Rail Output Stages. The best any op amp output stage can do is an "almost" rail-to-rail swing, when it is lightly loaded.

# Input Circuit of AD7276 2.35V-3.6V, 12-Bit, 3MSPS 6-Lead TSOT ADC

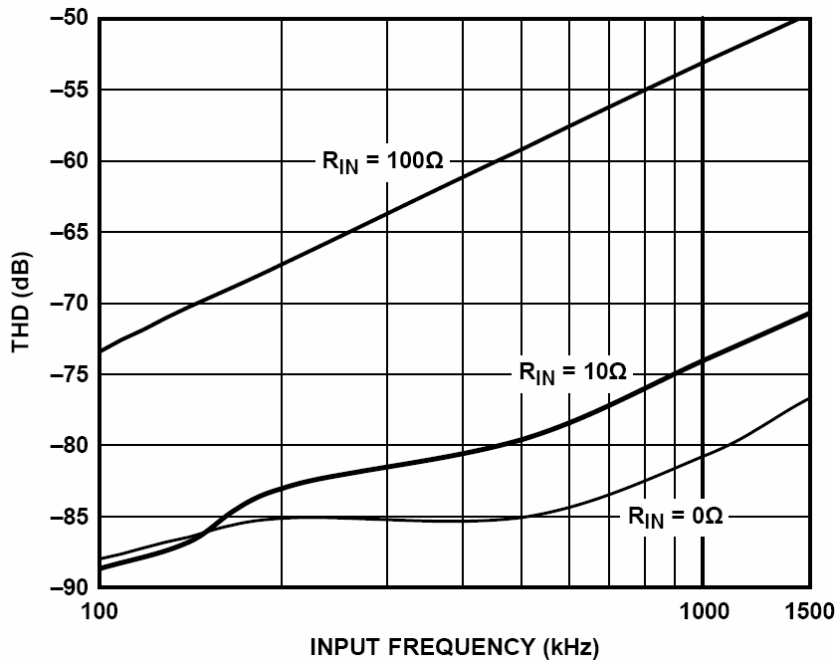



The AD7276/AD7277/AD7278 are 12-/10-/8-bit, low power (12.6mW), successive approximation ADCs, respectively. The parts operate from a single 2.35V to 3.6V power supply and feature throughput rates of up to 3MSPS. The parts contain a low noise, wide bandwidth track-and-hold circuit that can handle input frequencies in excess of 55MHz. The conversion process and data acquisition are controlled using the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of CS (bar), and the conversion is also initiated at this point. There are no pipeline delays associated with the part. The reference for the part is taken internally from $V_{DD}$. This allows the widest dynamic input range to the ADC; therefore, the analog input range for the part is 0 to $V_{DD}$. The conversion rate is determined by the SCLK. For 3MSPS operation, SCLK is 48MHz. The CS (bar) signal does not have to be synchronized to SCLK.

A simplified block diagram of the series is shown in this figure. This ADC utilizes a standard successive approximation architecture based on a switched capacitor CMOS charge redistribution DAC. The input CMOS switches, SW1 and SW2, comprise the sample-and-hold function, and are shown in the track mode in the diagram. Capacitor C1 represents the equivalent parasitic input capacitance, $C_H$ is the hold capacitor, and $R_S$ is the equivalent on-resistance of SW2. In the track mode, SW1 is connected to the input, and SW2 is closed. In this condition, the comparator is balanced, and the hold capacitor $C_H$ is charged to the value of the input signal. Note that the drive circuit must be capable of driving this capacitance, and the series resistance must not be high enough to limit the bandwidth. Assertion of convert start CS (bar) starts the conversion process: SW2 opens, and SW1 is connected to ground, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the hold capacitor to bring the comparator back into balance. At the end of the appropriate number of clock pulses, the conversion is complete.

Under certain conditions, the AD7276-family can be directly connected to the source as described in the next figure.

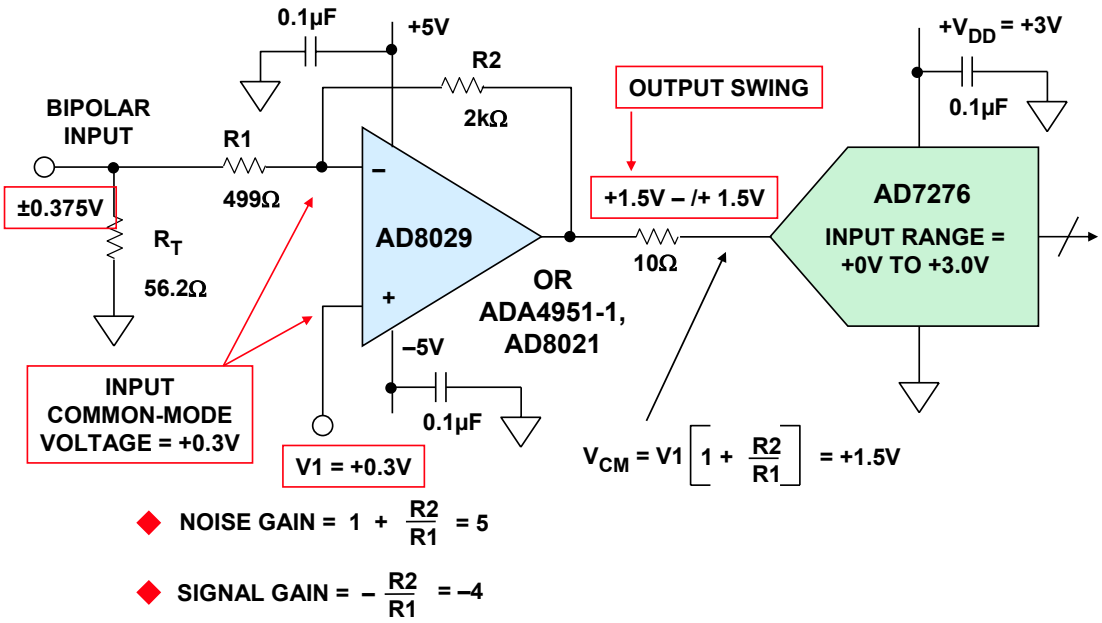
## Low Source Resistances Can Drive the AD7276 Input Directly




This figure shows the AD7276 THD as a function of the analog input frequency and the source resistance. This allows the user to determine if an external buffer amplifier is required, based on the system THD requirement and the source resistance.

The reason for the strong dependence of THD on source resistance is because of the highly nonlinear nature of the input circuit. Larger source resistances increase the effects of the nonlinearity caused by the changing capacitance as the sample-and-hold switches.

# Op Amp Driver for AD7276 Requires Dual Supply Op Amp




If an external buffer amplifier is needed to drive the AD7276, it must operate on separate supplies, because the output stage must drive the signal between 0V and +3V. A rail-to-rail output amplifier operating on a single +3V supply would cause the signal to be clipped when it approached either 0V or +3V.

This shows the AD8029 operating on dual 5V supplies acting as a level shifter and a negative gain-of-4. The +0.3V dc level on the non-inverting input is amplified by the noise gain (5) to provide the +1.5V common-mode output level.

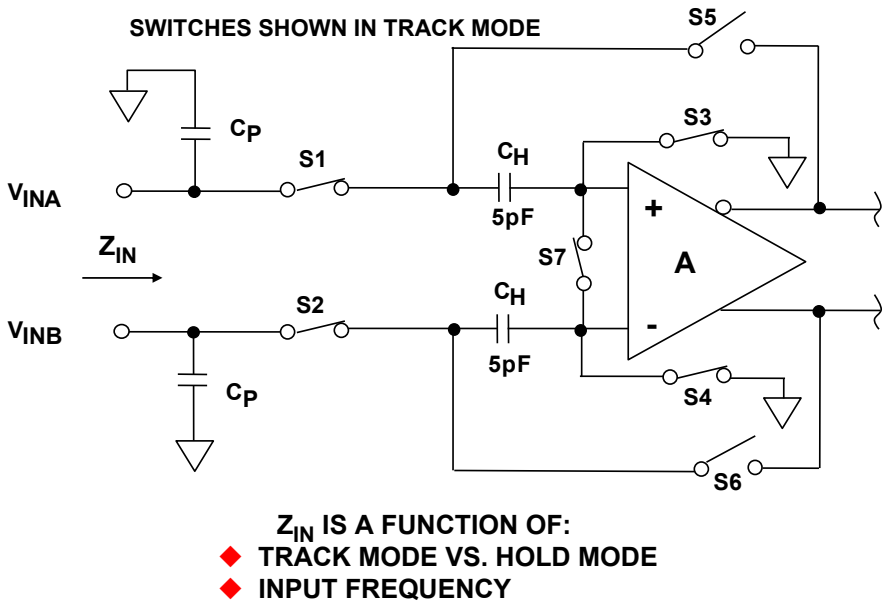
The design procedure starts by determining the signal gain required. The output swing is 3V p-p, and the input swing is 0.75V p-p, so the signal gain must be –4. This sets the ratio of R2 to R1.

The noise gain is 5, therefore a common-mode voltage of +0.3V is required to develop the output offset of +1.5V.

Note that since the drive amplifier operates on ±5V supplies, and the ADC on a +3V supply, care must be taken that the amplifier does not overdrive the ADC, especially under power-up conditions. A suitable clamping network may therefore be required to protect the ADC from overdrive.

# Differential Amplifier Drivers for ADCs

# Simplified Input Circuit for a Typical Unbuffered Switched Capacitor CMOS Sample-and-Hold




This figure shows a simplified input circuit for an unbuffered CMOS switched capacitor ADC. Most high performance CMOS switched capacitor pipelined ADCs have differential inputs. The differential structure is typically carried through most of the ADC. This makes matching requirements easier as well as reduces second-order products. In addition, the differential structure helps in common-mode noise rejection.

Note that the SHA switches are connected directly to each of the inputs. Switching transients can be significant, because there is no isolation buffer. The drive amplifier settling time to the transients must be fast enough so that the amplifier settles to the required accuracy in less than one-half the sampling period (this settling time must include the effects of any external series resistance).

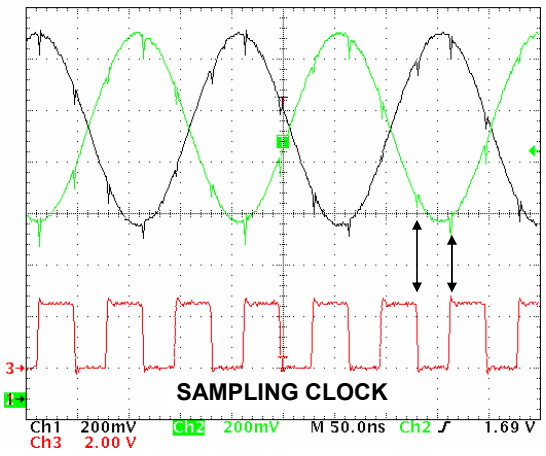
The differential input impedance of this structure is dynamic and changes when the SHA switches between the sample mode and the hold mode. In addition, the impedance is a function of the analog input frequency.

In the track mode (shown in the figure), the input signal charges and discharges the hold capacitors, $C_H$. When the circuit switches to the hold mode the switches reverse their positions, and the voltage across the hold capacitors is transferred to the outputs.

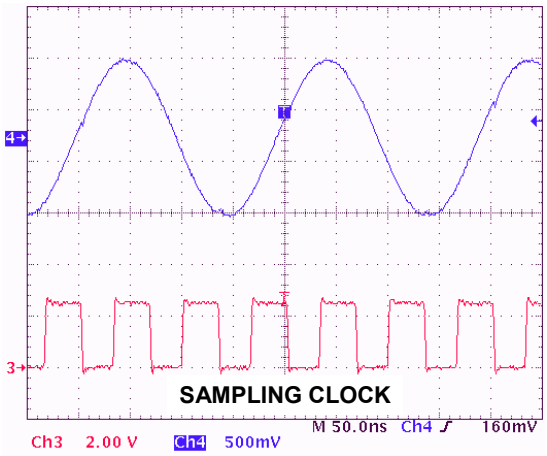
It is highly recommended that this type of input be driven differentially for common-mode rejection of the switching transients. While it is possible to drive them single-ended (with one input connected to the appropriate common-mode voltage), degradation in SFDR will occur because the even-order distortion products are no longer rejected.

# Typical Single-Ended (A) and Differential (B) Input Transients of CMOS Switched Capacitor ADC

**(A) SINGLE ENDED**




**(B) DIFFERENTIAL**




- **Differential charge transient is symmetrical around mid-scale and dominated by linear component**
- **Common-mode transients cancel with equal source impedance**

**Note: Data Taken with 50Ω Source Resistances**

Figure (A) shows each of the differential inputs of a typical unbuffered CMOS ADC as well as the sampling clock. The inputs were driven with a 50Ω source resistance. Note that a transient occurs on each edge of the sampling clock because of the switching action previously described.

Figure (B) shows the differential input signal to the ADC under the same conditions as (A). Note that most of the transient current glitches are cancelled because they are common-mode signals.

Note that for cancellation to be optimum the two inputs must be driven from a balanced source impedance (the real and reactive components of the impedance must be matched).

# Advantages of Differential Analog Input Interfaces for Data Converters

- **Differential inputs give twice the signal swing vs. single-ended (Especially important for low voltage single-supply operation)**
- **Differential inputs help suppress even order distortion products**
- **Many IF/RF components such as SAW filters and mixers are differential**
- **Differential inputs suppress common-mode ADC switching noise including LO feed-through from mixer and filter stages**
- **Differential ADC designs allow better internal component matching and tracking than single-ended. Less need for trimming**

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- **If you drive them single-ended, you will have degradation in distortion and noise performance**
- **However, many signal sources are single-ended, so the differential amplifier is useful as a single-ended to differential converter**

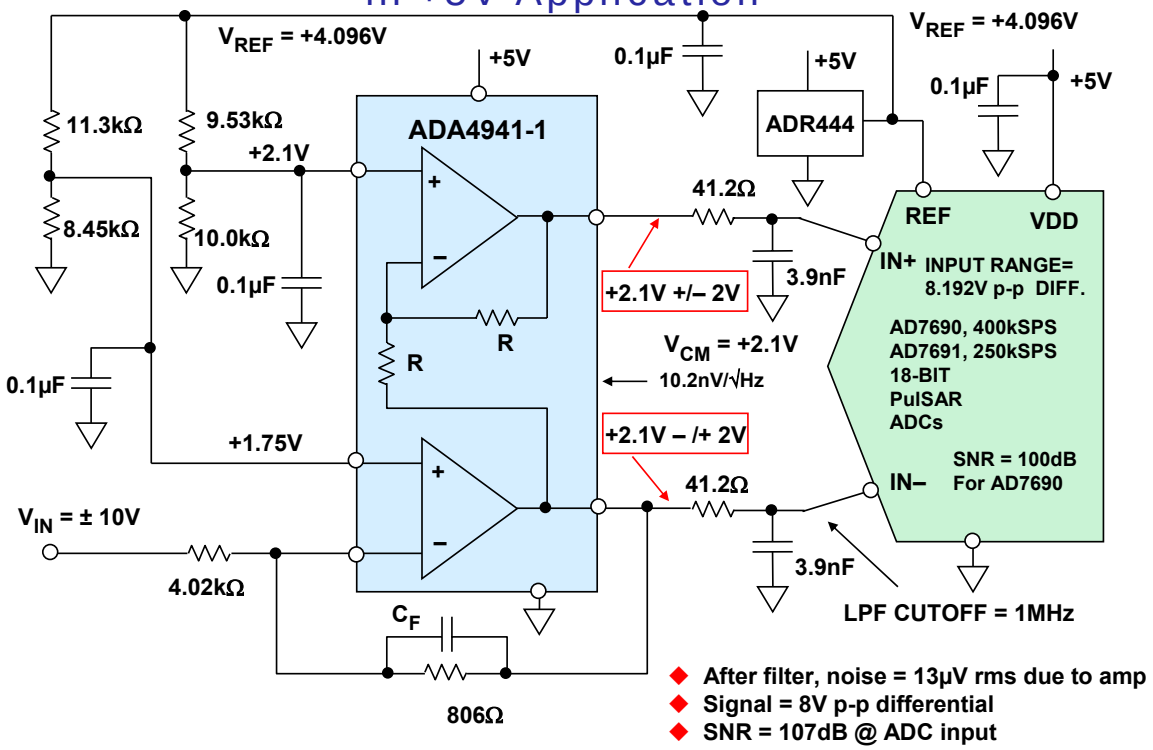
This list summarizes the advantages of using differential analog inputs for ADCs. In the real world, however, many signals are single-ended, and a convenient method is required to convert them to differential signals with minimum degradation in noise and distortion.

A family of differential amplifiers has been developed specifically for this purpose and are described in the next few pages.

The first two differential amplifiers discussed are the ADA4941 and the ADA4922. These amplifiers are optimum drivers for the 16- and 18-bit family of PulSAR successive approximation ADCs.

Another class of differential amplifiers is designed specifically for higher speed ADCs.

## ADA4941 Driving AD7690 18-Bit PulSAR® ADC in +5V Application




This figure shows the ADA4941-1 driving the 18-bit PulSAR family of ADCs which have switched capacitor inputs. The ADA4941-1 is a low power, low noise differential driver for ADCs up to 18 bits in systems that are sensitive to power. Small signal bandwidth is 31MHz. A resistive feedback network can be added to achieve gains greater or less than 2. The ADA4941-1 provides essential benefits, such as low distortion and high SNR that are required for driving high resolution ADCs. With a wide input voltage range (0V to 3.9V on a single 5V supply), rail-to-rail output, high input impedance, and a user-adjustable gain, the ADA4941-1 is designed to drive single-supply ADCs with differential inputs found in a variety of low power applications, including battery-operated devices and single-supply data acquisition systems.

In this application, the two resistor dividers set the output common-mode voltage of the ADA4941-1 to +2.1V so that the output only has to go to within 100mV of ground. This allows sufficient headroom for the rail-to-rail output stages of the amplifier and allows the entire circuit to operate on a single +5V supply.

The input range of the AD7690 and AD7691 is $2V_{REF}$ p-p differential. The reference used is the ADR444 which is a 4.096V reference. The 41.2Ω resistors and the 3.9nF capacitors for a lowpass filter with a cutoff frequency of 1MHz, suitable for use with the AD7690 which has an input bandwidth of 9MHz. A lower frequency cutoff frequency would be used with the 250kSPS AD7692 PulSAR ADC.

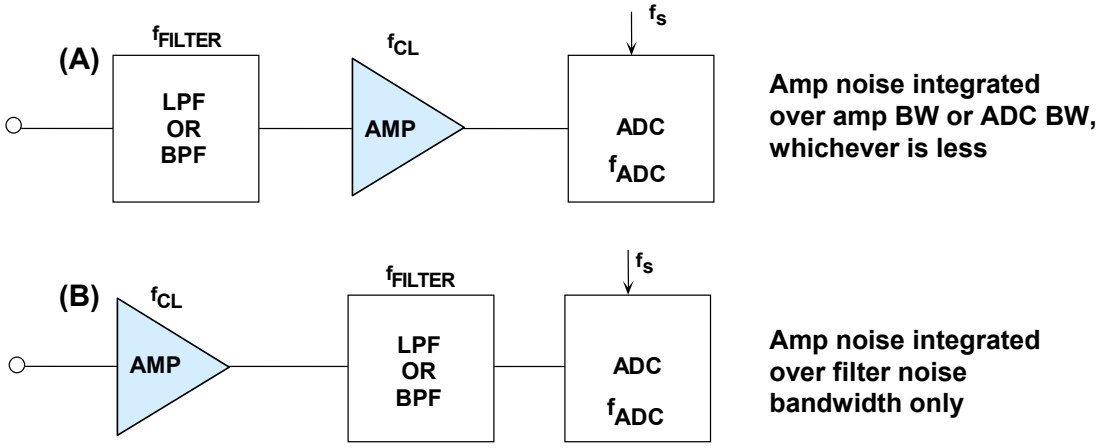
The output noise spectral density of the ADA4941-1 is 10.2nV/√Hz. Integration over the noise bandwidth of the filter yields:

$$v_{rms} = v_n\sqrt{BW} = 10.2\times10^{-9}\sqrt{(1.57\times1\times10^{6})} = 13\mu V.$$

The peak-to-peak signal is 8V, and the rms value of the signal is therefore 2.83V.

The SNR due to the op amp is therefore SNR = $20\log(2.83 \div 13\times10^{-6})$ = 107dB, which is 7dB better than the 100dB SNR of the ADC.

# Positioning the Noise Reduction Filter to Reduce the Effects of the Op Amp Noise




- **ADCs typically have very high input bandwidths, usually much greater than $f_s/2$**
- **Low distortion drive amplifiers typically have high bandwidths**
- **Placing a simple LPF or BPF placed between the AMP and the ADC is an excellent noise reduction technique**
- **The output capacitor of the filter absorbs some of the ADC input transient currents.**

ADCs typically have input bandwidths much greater than their maximum sampling rates. For instance, a 100MSPS ADC may have an input bandwidth of 700MHz.

A good drive amplifier also has a bandwidth which is much greater than the sampling rate in order to give good distortion performance over the bandwidth of interest.

The wideband noise from an op amp will therefore be integrated over the full input bandwidth of the ADC if the filter is placed ahead of the op amp as in (A).

The most desirable location for the noise reduction filter is between the amplifier and the ADC as shown in (B). However, the amplifier must be capable of driving the net impedance presented by the filter and the ADC.

The rms noise at the output of the filter is easily calculated from the following equation:

$$v_{rms} = v_n\sqrt{BW},$$

where $v_n$ is the wideband voltage noise spectral density of the op amp (expressed in nV/√Hz), and BW is the equivalent noise bandwidth of the filter (see next slide). The SNR of the output of the filter due to the op amp noise can then be calculated knowing the peak-to-peak value of the input signal to the ADC. This SNR can then be compared to the SNR of the ADC.

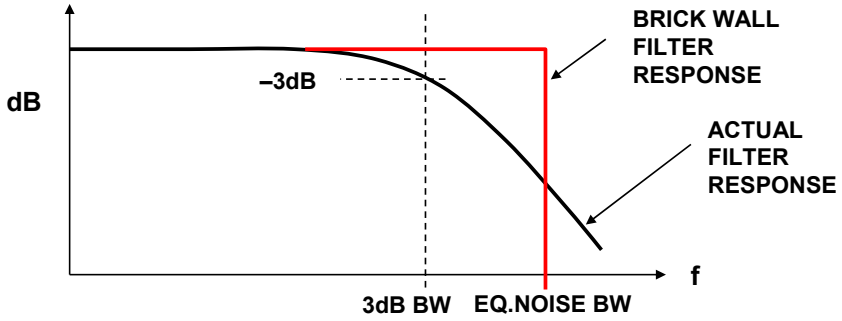
The input noise of the ADC (not including the op amp) can be calculated based on the ADC SNR by using the equation SNR = 20log(Vsignal/Vnoise) and solving for Vnoise. Vsignal is simply the rms value of the ADC fullscale input signal.

The total input noise from both the ADC and the op amp can be calculated by combining the two noise sources on a root-sum-square basis because they are uncorrelated.

Good reductions in noise can be achieved with just a simple 1- or 2-pole filter as will be shown in the next figure.

## Relationship Between Equivalent Noise Bandwidth and 3-dB Bandwidth for Butterworth Filter

| NUMBER OF POLES | EQ. NOISE BW / 3dB BW |
|---|---|
| 1 | 1.57 |
| 2 | 1.11 |
| 3 | 1.05 |
| 4 | 1.03 |
| 5 | 1.02 |

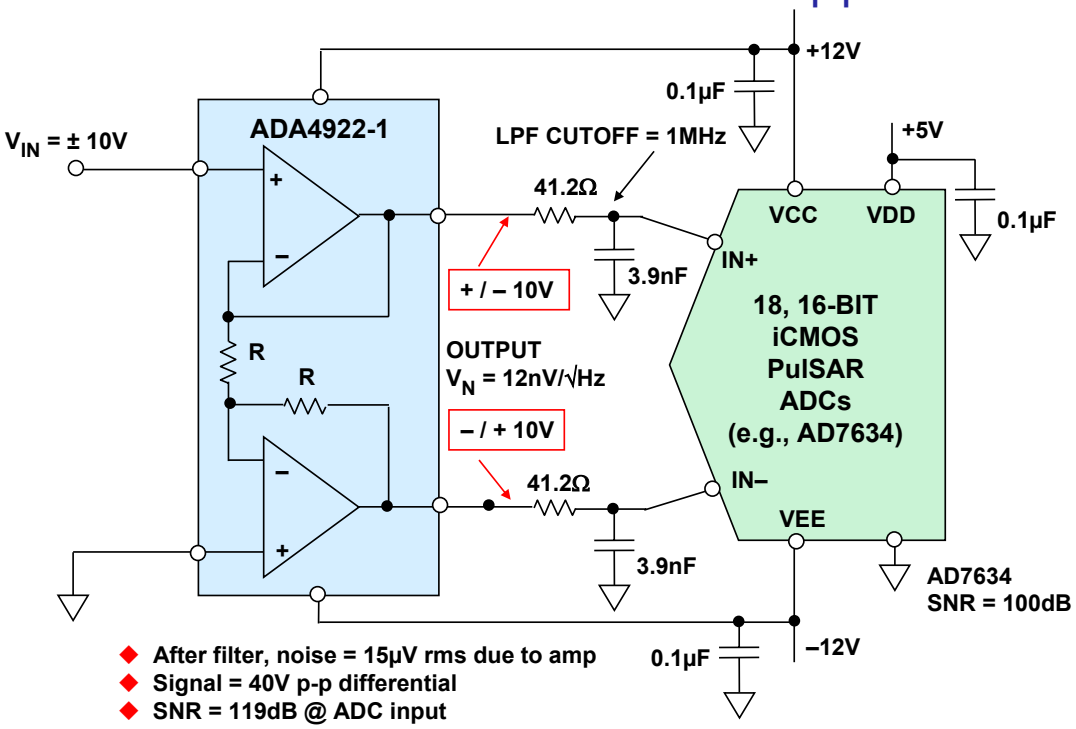



The equivalent noise bandwidth of a filter is the bandwidth of a "brick wall" filter which has the same effect on broadband Gaussian noise as an actual filter which has a finite transition region.

This figure shows the ratio of the equivalent noise bandwidth to the 3dB bandwidth for Butterworth filters with one to five poles. For a single-pole filter, the ratio is $\pi/2 = 1.57$. Notice that since the ratio is only 1.11 for a 2-pole filter, adding additional poles offers very little improvement in noise reduction.

Most of the driver circuits shown in the following figures in this section contain at least a single-pole RC noise reduction filter between the drive amplifier and the ADC. In many cases, the R and C values are optimized based on empirical data because of the transient nature of the CMOS ADC inputs.

# ADA4922-1 Driving AD7634 18-Bit *i*CMOS PulSAR ADC in ±12V Industrial Application



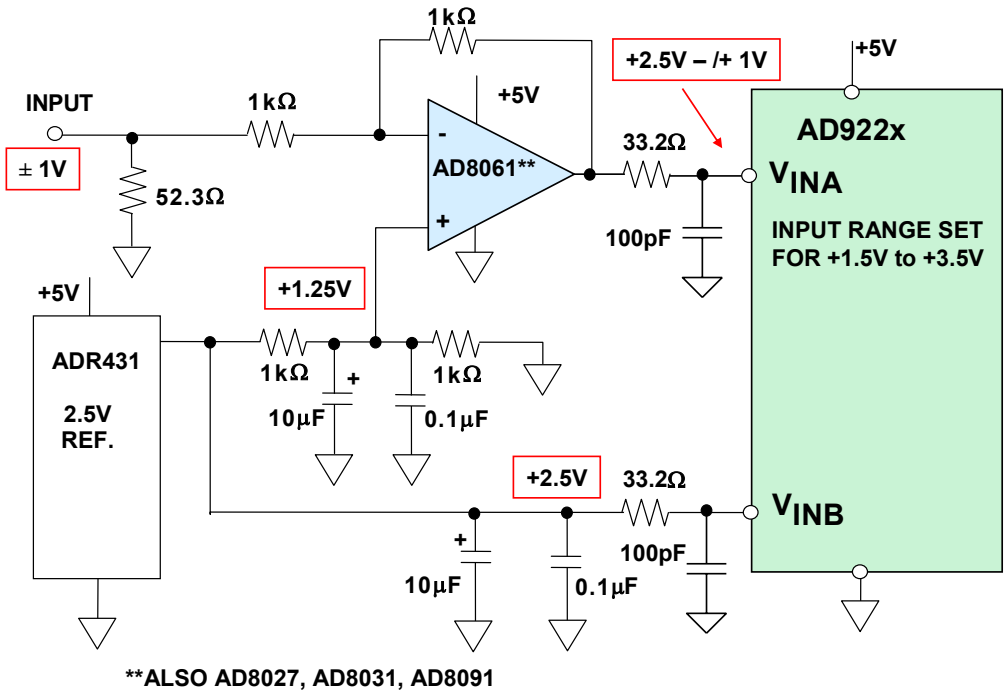

There are many industrial applications where signals as great as ±10V are standard. This figure shows a simple method for performing a single-ended to differential conversion using the ADA4922-1 driving a 16-bit or 18-bit *i*CMOS PulSAR ADC. The *i*CMOS family of PulSAR ADCs has a low power front end which operates high voltage supplies up to ±12V. The rest of the ADC operates on a low voltage power supply which is typically 5V.

The ADA4922-1 is a differential driver for 16-bit to 18-bit ADCs that have differential input ranges up to 40V p-p. Small signal bandwidth is 38MHz. Configured as an easy-to-use, single-ended-to-differential amplifier, the ADA4922-1 requires no external components to drive ADCs. The ADA4922-1 provides essential benefits such as low distortion and high SNR that are required for driving ADCs with resolutions up to 18 bits. With a wide supply voltage range (5V to 26V), high input impedance, and fixed differential gain of 2, the ADA4922-1 is designed to drive ADCs found in a variety of applications, including industrial instrumentation.

The ADA4922-1 is manufactured on ADI's proprietary second-generation XFCB process that enables the amplifier to achieve excellent noise and distortion performance on high supply voltages. The ADA4922-1 is available in an 8-lead 3mm × 3mm LFCSP as well as an 8-lead SOIC package. Both packages are equipped with an exposed paddle for more efficient heat transfer. The ADA4922-1 is rated to work over the extended industrial temperature range, −40°C to +85°C.

Noise calculations using the 1MHz lowpass filter yield 15µV rms for the op amp. The signal range of the ADC is 40V p-p, which is 14.14V rms. This yields an SNR of 119dB due to the op amp alone. Using the AD7634 SNR of 100dB, the rms ADC input noise contribution is calculated to be 141µV rms. The combined input ADC noise is therefore 142µV rms, and the contribution due to the op amp is almost negligible.

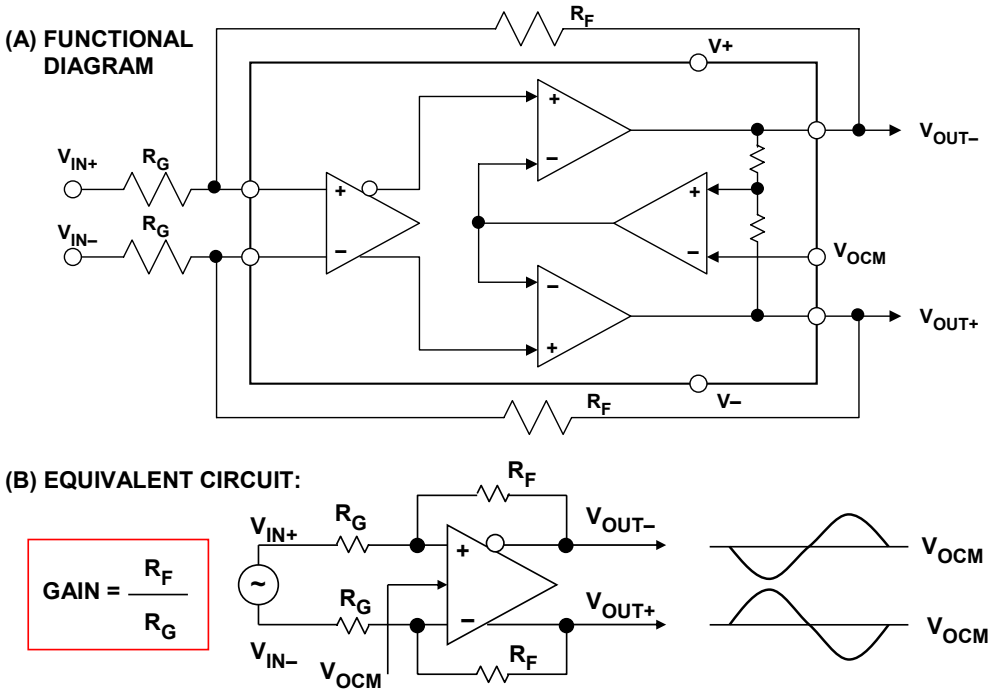
# DC-Coupled Single-Supply Level Shifter for Driving AD922x ADC Input




Distortion performance will most likely be compromised if a differential input ADC is driven single-ended. However, if single-ended drivers must be used, care should be taken that the source impedance is balanced as shown here. Balancing the source impedance (both R and C) allows some cancellation of the common-mode current transients produced by the ADC input SHA.

This circuit is designed to operate on a single +5V supply. It accepts a bipolar ±1V input signal and interfaces it to the input of the ADC whose range is set for 2V p-p with a 2.5V common-mode voltage. The AD8061 rail-to-rail output op amp is used, although others are suitable depending upon bandwidth and distortion requirements (for example, the AD8027, AD8031, or AD8091). The +1.25V input common-mode voltage for the AD8061 is developed by a voltage divider from the external ADR431 2.5V reference.

# AD813x and ADA493x Differential ADC Drivers Functional Diagram and Equivalent Circuit



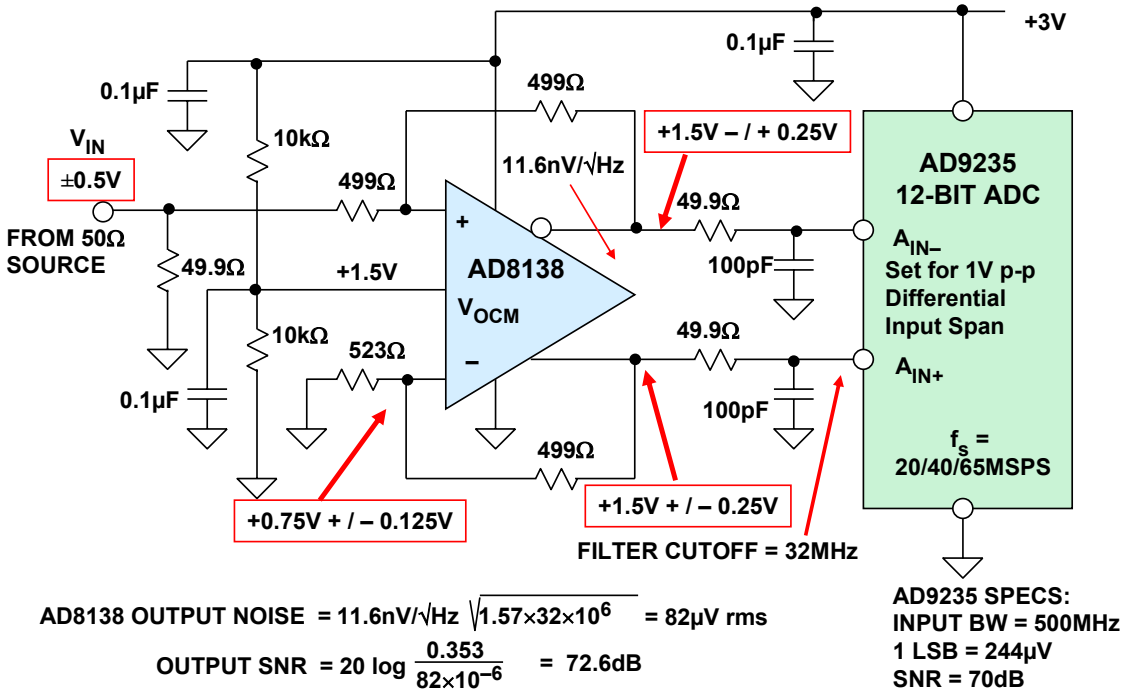

A block diagram of the AD813x and ADA493x family of fully differential amplifiers optimized for higher speed ADC driving is shown in this figure. The (A) diagram shows the details of the internal circuit, and (B) shows the equivalent circuit. The gain is set by the external resistors $R_F$ and $R_G$, and the common-mode voltage is set by the voltage on the $V_{OCM}$ pin. The internal common-mode feedback forces the $V_{OUT+}$ and $V_{OUT-}$ outputs to be balanced, i.e., the signals at the two outputs are always equal in amplitude but 180° out of phase per the equation,

$$V_{OCM} = ( V_{OUT+} + V_{OUT-} ) / 2.$$

The amplifier uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level in level shifting applications. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the $V_{OCM}$ input, without affecting the differential output voltage. The result is nearly perfectly balanced differential outputs of identical amplitude and exactly 180° apart in phase over a wide frequency range. The circuit can be used with either a differential or a single-ended input, and the voltage gain is equal to the ratio of $R_F$ to $R_G$.

The $V_{OCM}$ pin is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on V+ and V−). Relying on this internal bias results in an output common-mode voltage that is within about 100mV of the expected value. In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (made up of 10kΩ resistors or less), be used. In addition, the $V_{OCM}$ pin should be decoupled to ground using a ceramic capacitor (0.01µF to 0.1µF).

# DC-Coupled AD8138 Driving AD9235 12-Bit, 20/40/65MSPS CMOS ADC, Baseband Signal




AD8138 OUTPUT NOISE = $11.6\text{nV}/\sqrt{\text{Hz}} \sqrt{1.57 \times 32 \times 10^6} = 82\mu\text{V rms}$

OUTPUT SNR = $20 \log \frac{0.353}{82 \times 10^{-6}} = 72.6\text{dB}$

This figure represents a typical application of the AD8138 differential amplifier as a single-ended to differential ADC driver for the AD9235 12-bit, 65MSPS CMOS ADC.

The AD8138 has a 3dB bandwidth of 320MHz and delivers a differential signal with 85dBc SFDR for a 20MHz signal.

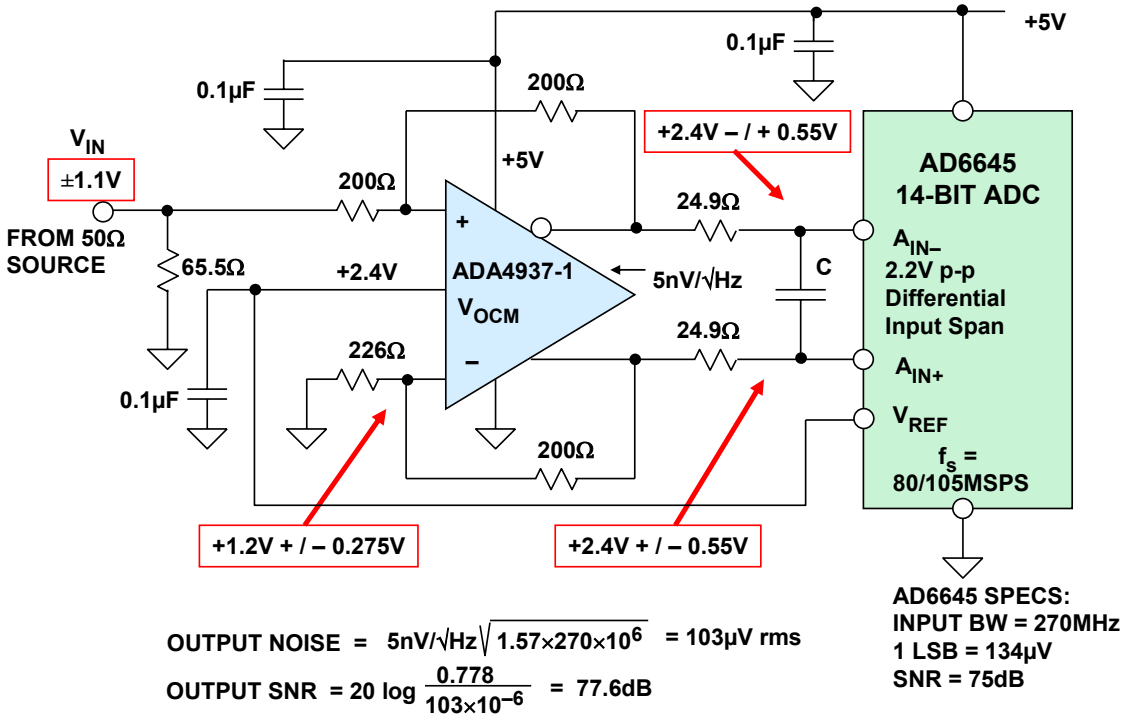
The input range of the AD9235 is set for 1V p-p differential; therefore, each input of the AD8138 only swings between +1.25V and +1.75V. This is within the output drive capability of the AD8138 even though it does not have a "rail-to-rail" output stage. This allows the AD8138 to be operated on the same +3V supply as the AD9235 ADC.

The 523Ω resistor matches the net drive impedance seen by the noninverting input (499Ω + 50Ω||49.9Ω ≈ 523Ω).

Note the simple RC input filtering circuit which reduces the effects of the transient currents as well as the amplifier noise. The cutoff frequency of the RC combination is 32MHz. The output voltage noise spectral density of the AD8138 is 11.6nV/√Hz, resulting in 82µV rms noise in the 32MHz bandwidth. The corresponding SNR is 72.6dB, which is 2.6dB better than the 70dB SNR of the AD9235.

A Differential Amplifier Gain Calculator design tool is available at www.analog.com/DesignCenter, which can be used to check the input and output common-mode voltage ranges of the differential amplifier series for different power supplies, gain settings, and input signal ranges.

## ADA4937-1 Driving AD6645 in +5V DC-Coupled Application




$$\text{OUTPUT NOISE} = 5\text{nV}/\sqrt{\text{Hz}}\sqrt{1.57\times270\times10^{6}} = 103\mu\text{V rms}$$

$$\text{OUTPUT SNR} = 20\log\frac{0.778}{103\times10^{-6}} = 77.6\text{dB}$$

This figure as well as the following three figures illustrate very similar circuits. However, each circuit illustrates how subtle differences in ADC common-mode voltage, signal swing, and supply voltage affect the choice of differential drive amplifier.

The ADA4937-1 is one of the latest in the series of differential amplifiers and is optimized for operation on a single +5V supply. In this figure, it is used as a level shifter to drive the AD6645 14-bit 80/105MSPS ADC. The AD6645 operates on a 2.2V p-p differential signal with a common-mode voltage of +2.4V. This means that each output of the ADA4937 must swing between 1.85V and 2.95V which is within the output drive capability of the ADA4937-1 operating on a single +5V supply.

The input signals must swing between 0.925V and 1.475V which falls within the allowable input range of the ADA4937-1 operating on a single +5V supply.

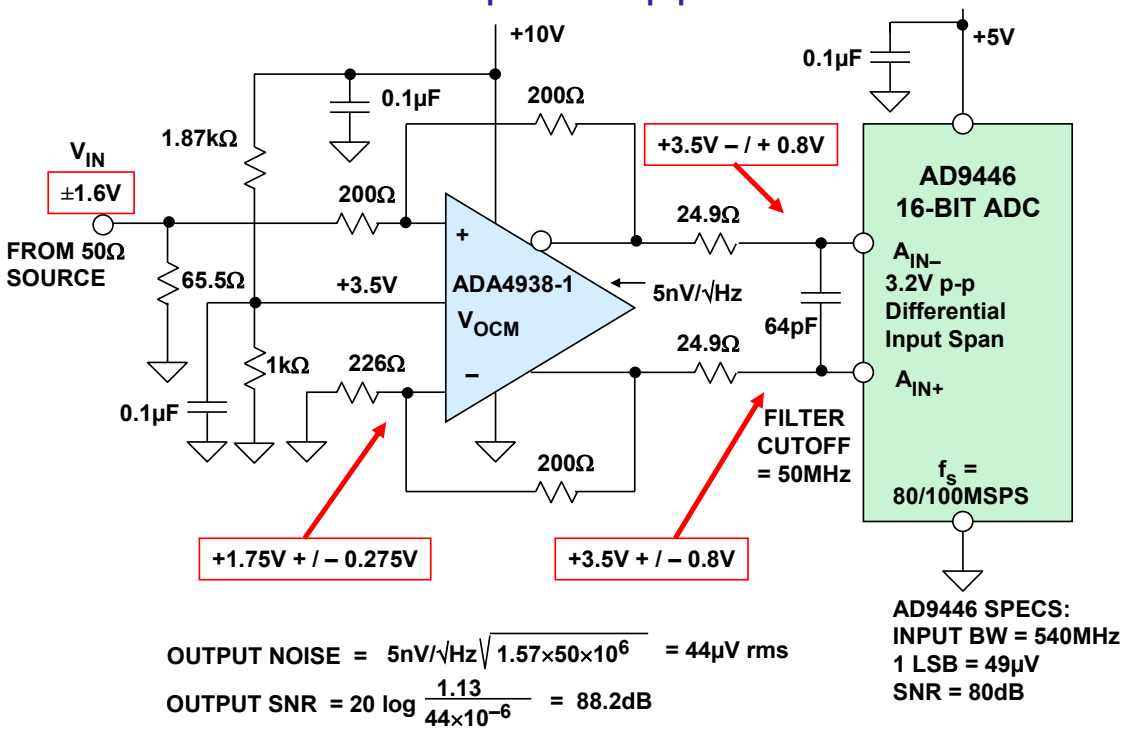
The 65.5Ω input termination resistor in parallel with the 200Ω gain setting resistor makes the overall impedance approximately 50Ω. Note that a 226Ω resistor is inserted in series with the inverting input. This is to match the net impedance seen by the noninverting input (200Ω + 65.5Ω||50Ω ≈ 226Ω).

The output noise voltage spectral density of the ADA4937-1 is only 5nV/√Hz. This value includes the contributions of the feedback and gain resistors and is for G = 1. Integrated over the input bandwidth of the AD6645 (270MHz), this yields an output noise of 103µV rms. This corresponds to an SNR of 77.6dB due to the amplifier. Note that the integration must be over the full input bandwidth of the ADC since there is no external noise filter.

The SNR of the AD6645 is 75dB which corresponds to an input noise of 138µV rms. The combined noise due to the op amp (103µV) and the ADC (138µV) is 172µV, yielding an overall SNR of 73dB.

If the full bandwidth of the AD6645 is not required, a single-pole noise reduction filter can be added by selecting an appropriate value for C.

# ADA4938-1 (0V, 10V) Driving AD9446 in DC-Coupled Application

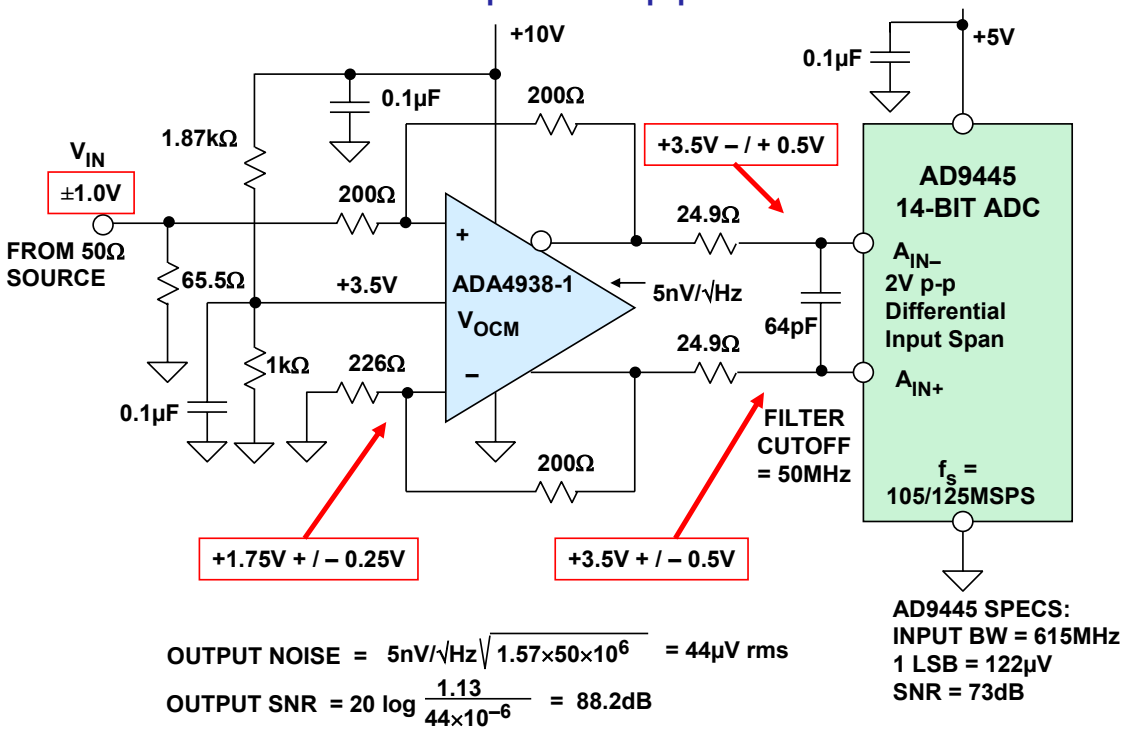



This circuit is very similar to the previous figure, but the AD9446 ADC requires an input voltage of +3.5V ±0.8V on each differential input. This means that each output of the differential amplifier must swing between +2.7V and +4.3V. The +4.3V requirement is outside the capability of the AD4937-1 driver operating on a +5V supply, so the ADA4938-1 driver operating on a +10V supply must be used.

The noise filter has a cutoff of 50MHz. The output noise of the driver (5nV/√Hz) integrated over this bandwidth is 44µV rms. This yields an SNR of 88.2dB for the driver which is 8.2dB better than the SNR of the AD9446.

Note that since the drive amplifier operates on +10V and the ADC on +5V, care must be taken that the amplifier does not overdrive the ADC input and cause damage. Power supply sequencing can also be an issue if power is applied to the amplifier before power is applied to the ADC. Suitable protection circuitry may therefore be required.

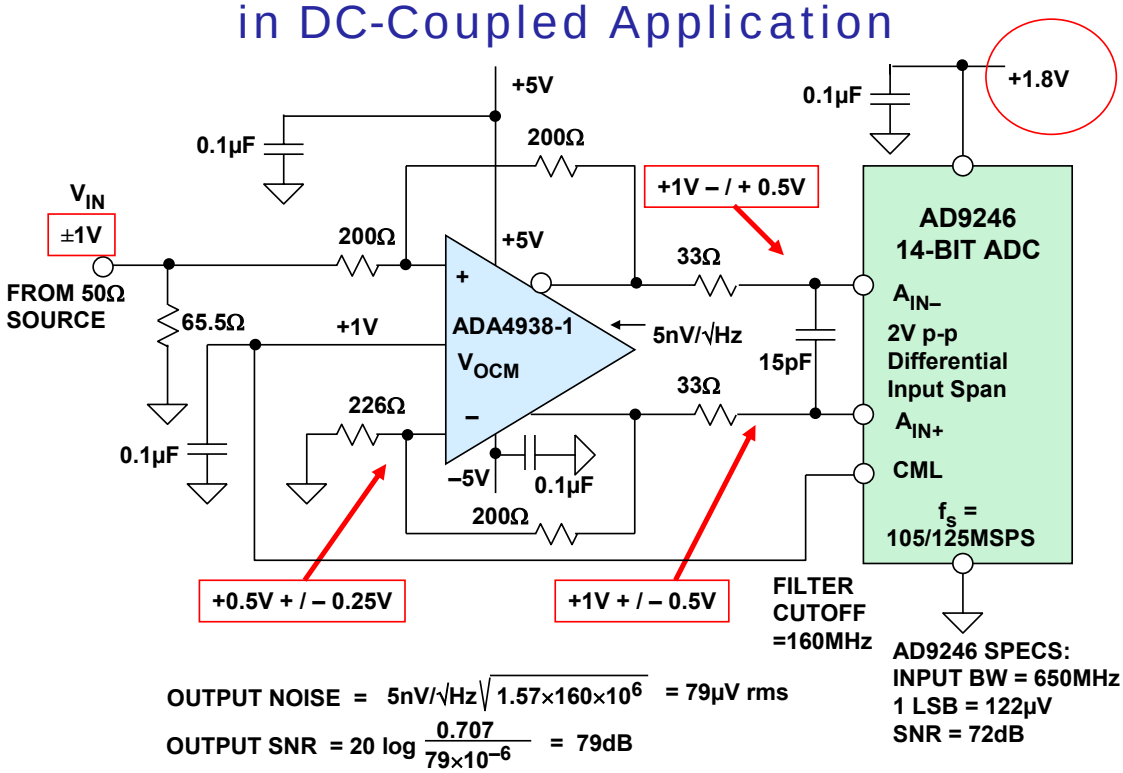
## ADA4938-1 (0V,+10V) Driving AD9445 in DC-Coupled Application




This figure shows the ADA4938-1 driving the AD9445 14-bit 105/125MSPS ADC. The circuit is very similar to the previous circuit with the exception of signal amplitude. Again, the ADA4938-1 amplifier operating on a +10V supply is required because each input of the AD9445 must be driven to +4V, which would not be possible with a drive amplifier operating on a +5V supply.

As in the previous example, suitable precautions against ADC overdrive must be taken since the amplifier operates on a +10V supply and the ADC on a +5V supply.

# ADA4938-1 (±5V) Driving AD9246 1.8V ADC in DC-Coupled Application



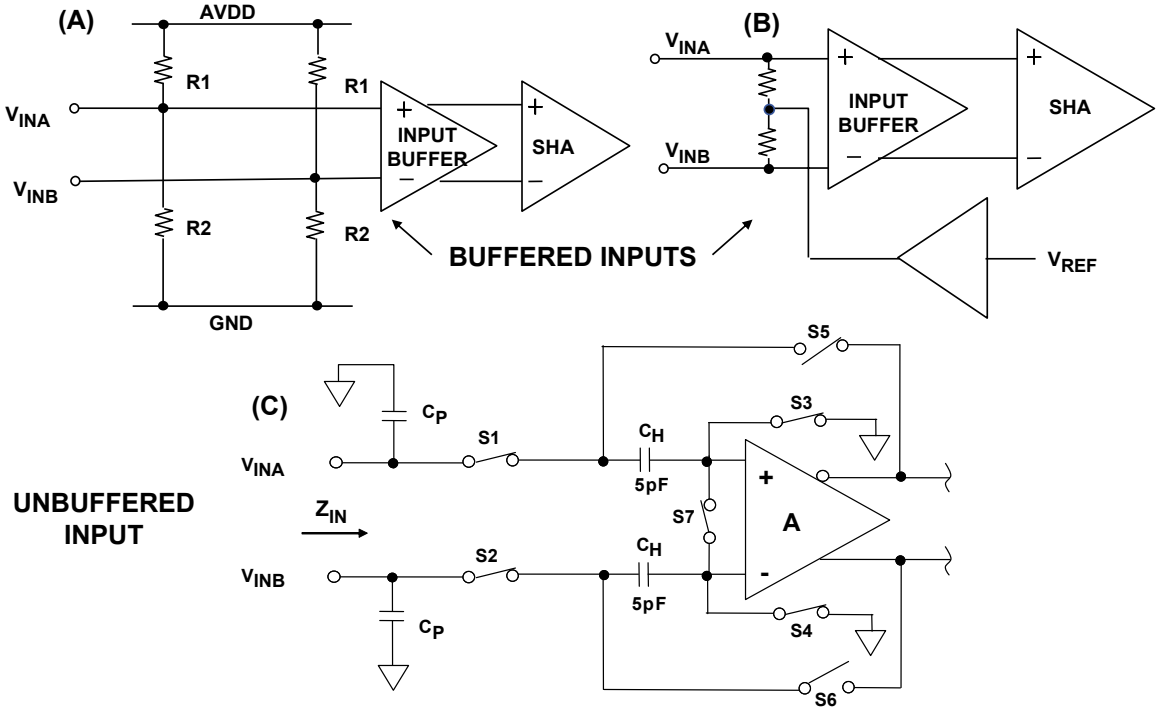

The AD9246 is a low power (395mW) 14-bit, 105/125MSPS ADC which operates on an analog supply of +1.8V.

The input signal to the AD9246 is 2V p-p differential with a common-mode voltage of +1V; therefore, each output of the drive amplifier must swing between +0.5V and +1.5V. This requires a dual supply differential driver such as the ADA4938-1 operating on ±5V supplies as shown in the figure.

As in the previous circuits, suitable precautions must be taken against ADC overdrive because the drive amplifier operates on ±5V supplies, while the ADC operates on a single +1.8V supply.

# Equivalent Input Circuit Models for Buffered (BiCMOS) and Unbuffered (CMOS) Pipelined ADCs

# Buffered and Unbuffered Differential ADC Inputs Structures



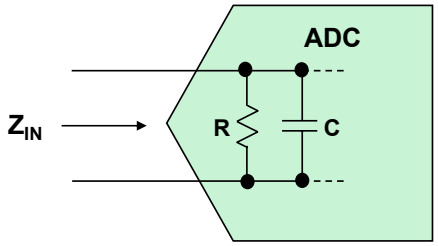

In designing the input interface circuit, it is important to know whether or not there is an input buffer present to isolate the input from the sample-and-hold circuit.

High performance pipelined BiCMOS ADCs (such as the AD6645, AD9445, and AD9446 generally have the input buffer on-chip. Two popular input structures for buffered input BiCMOS ADCs are shown in (A) and (B) in the figure.

CMOS pipelined ADCs typically dissipate less power and have slightly lower performance than BiCMOS ones, and generally don't have the input buffer, and as shown in (C), the input is connected directly to the sample-and-hold switches. The unbuffered input structure typically generates more transient currents than the buffered structure and is more difficult to drive.

When choosing an ADC, it is important to know if the input structure is buffered or unbuffered. In many cases, the input buffer is actually shown in the functional block diagram of the ADC which appears on the first page of the data sheet. In some cases, the input structure can be determined from the applications section of the data sheet where the description of the converter's operation is contained. As mentioned above, most CMOS ADCs have an unbuffered input, while BiCMOS ADCs have a buffered input—however, there can be exceptions.

# Input Impedance Model for Buffered and Unbuffered Input ADCs




**BUFFERED INPUT**

- **R and C are constant over frequency**
- **Typically:**

  **R: 1kΩ - 2kΩ**
  **C: 1.5pF - 3pF**

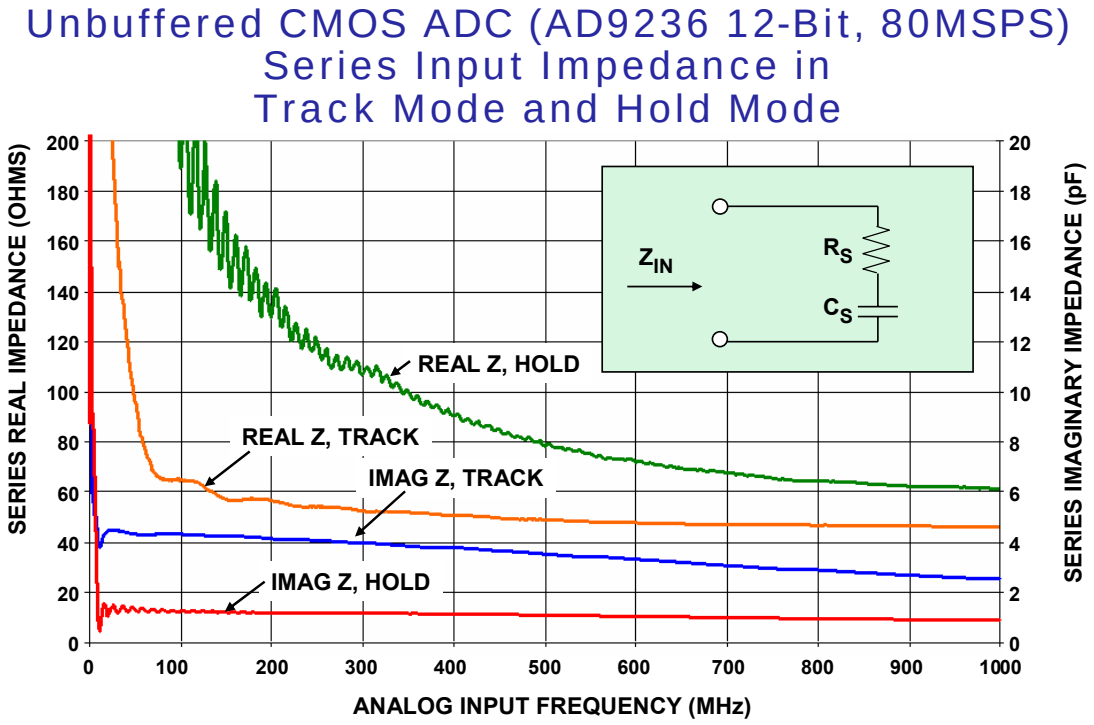
**UNBUFFERED INPUT**

- **R and C vary with both frequency and mode (track/hold)**
- **Use Track mode R and C at the input frequency of interest**

We can model the input impedance of both the buffered and unbuffered input structures as a resistance in parallel with a capacitance. In the case of the buffered input ADC, the R and C values are constant over input frequency. Typical values of R range from 1kΩ to 2kΩ, and typical values of C range from 1.5pF to 3pF, depending on the particular part. However, the data sheet for the ADC should always be consulted because there are some exceptions.

The unbuffered input structure is much more difficult to model because the R and C values change dynamically with both analog input frequency and whether the ADC is in the track mode or the hold mode.

For purposes of modeling the unbuffered input, it is the track mode impedance that is of most interest in designing the interface.




A sampling network analyzer can be used to measure the track mode and hold mode input impedance as a function of analog input frequency. See reference below.

This figure shows the real and imaginary part of the input impedance for the AD9236 12-bit, 80MSPS CMOS ADC, which is typical of other members of the family.

The figure shows the series mode input impedance, however, the parallel mode input impedance is of more interest.

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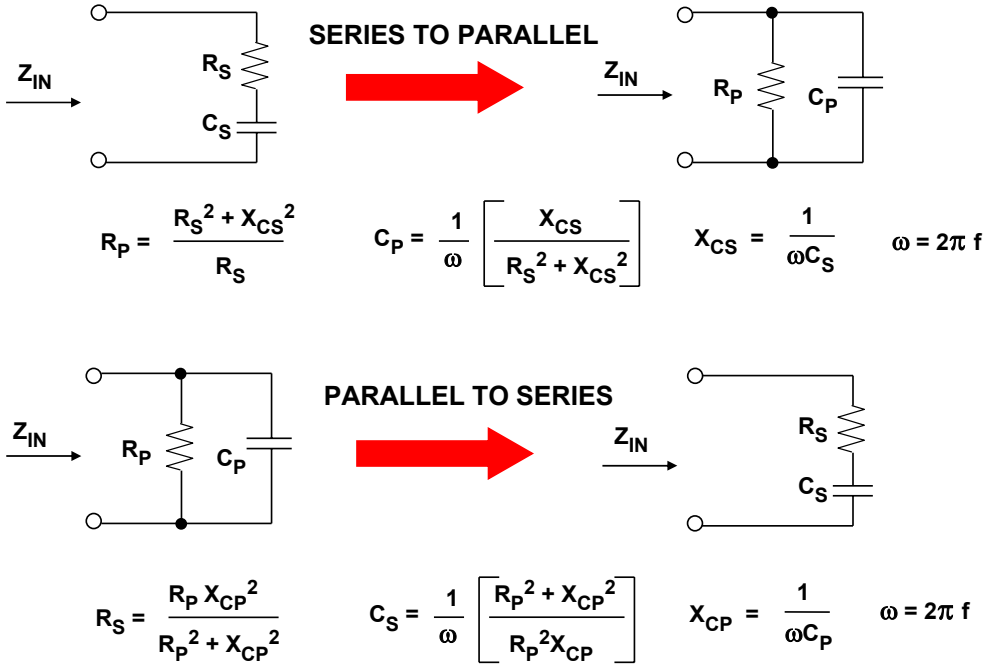
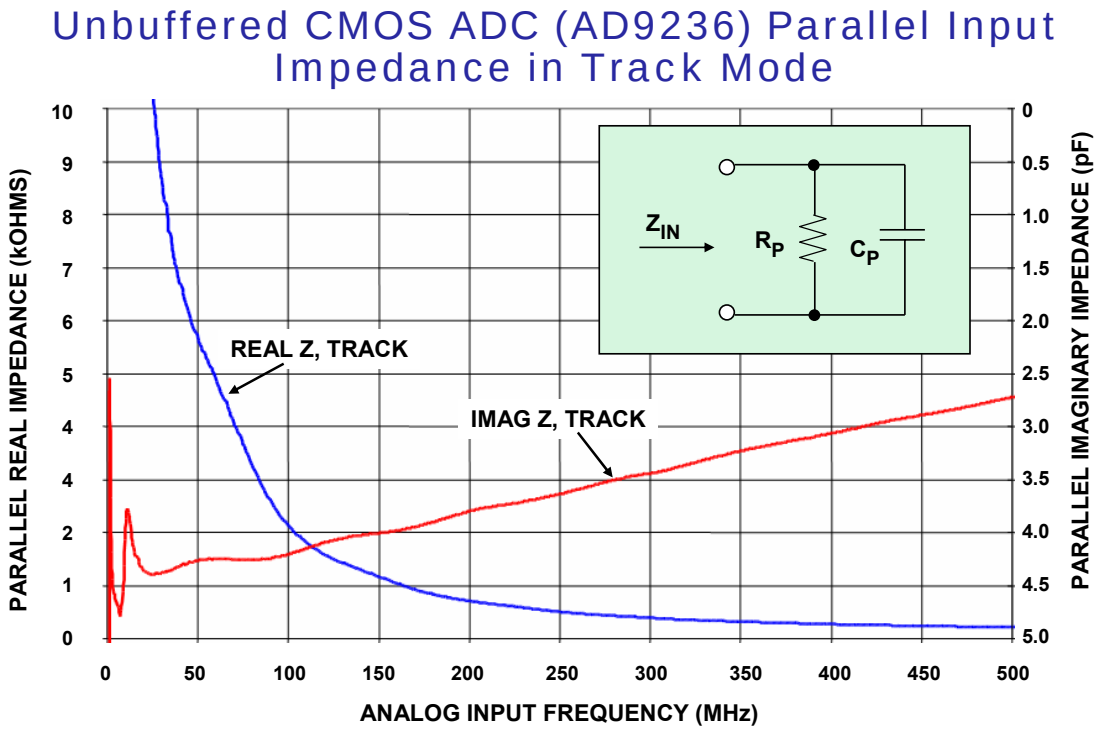
Rob Reeder, "Frequency Domain Response of Switched-Capacitor ADCs," Application Note *AN-742*, Analog Devices., www.analog.com/DesignCenter.

# Converting Between Series and Parallel Equivalent Circuits




The formulas shown in this figure can be used to convert between the series and parallel equivalent circuits if required.



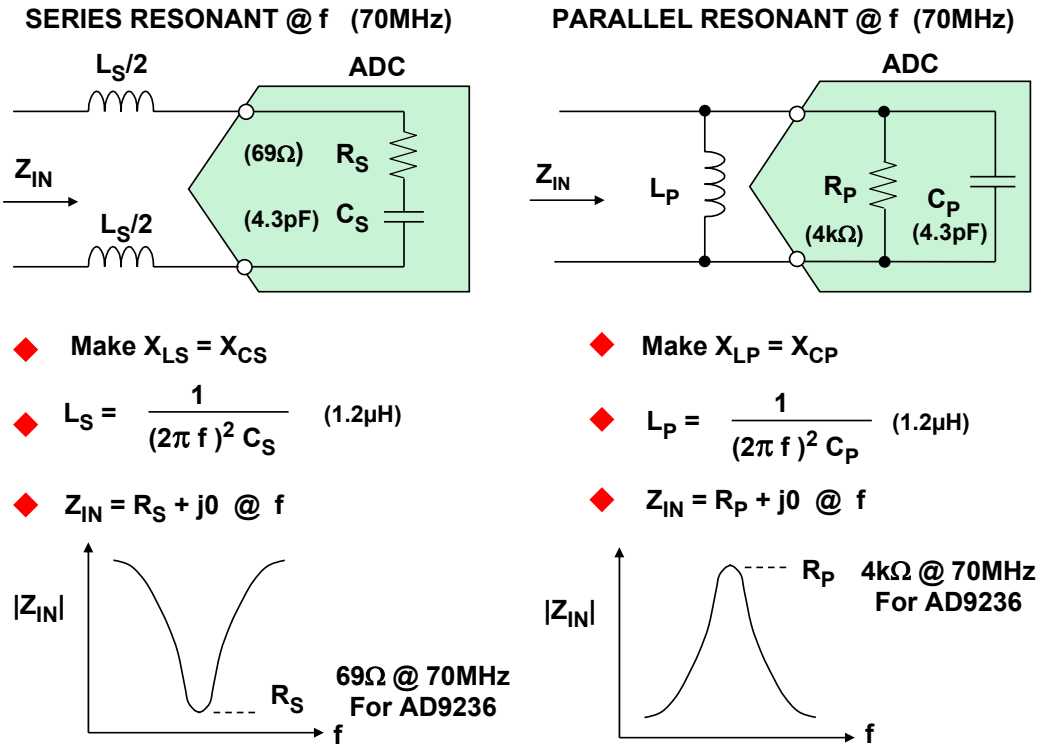

This shows only the parallel equivalent circuit for the track mode impedance as a function of analog input frequency. In general, parallel equivalent circuit is more useful.

The real (resistive) part of the input impedance is very high at lower frequencies (baseband) and to less than 2kΩ above 100MHz.

The imaginary (capacitive) part of the input impedance starts out at approximately 4.5pF at low frequencies and drops gradually as the frequency is increased.

Real and imaginary impedances are available as S-parameter in spreadsheet format on the Analog Devices' website in the evaluation board section of the product information.

# Basic Principles of Resonant Matching




Now that we have a method of determining the impedance of the input of the ADCs, it is useful to consider the principle of resonant matching when the input signal is an IF signal with a limited bandwidth.

Resonant matching is achieved by simply adding the appropriate external series or parallel inductance to cancel the effects of the series or parallel capacitance of the input circuit of the ADC. This presents a resistive load to the driver at the IF frequency of interest.

The first diagram shows the series approach. At a 70MHz IF frequency, the reactance of the 1.2µH inductor matches that of the 4.3pF capacitor, and the net impedance $Z_{IN}$ is resistive and equal to 69Ω. Note that the inductor value in each leg is equal to the calculated value divided by two.

The second diagram shows the parallel equivalent circuit for the same ADC. At the resonant IF frequency (70MHz), the input impedance is resistive and equal to 4kΩ.

The parallel resonant approach is preferable because at resonance it yields a much higher input impedance than the series approach. The high impedance is easier to drive with low distortion amplifiers. The reference below describes the technique of resonant matching in more detail.

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Chris Bowick, *RF Circuit Design*, Newnes/Elsevier, 1982, ISBN 0-7506-9946-9.

# Resonant Matched Design Example:

# AD8370 Variable Gain Amplifier Driving AD9236 12-Bit, 80MSPS ADC with 70MHz IF

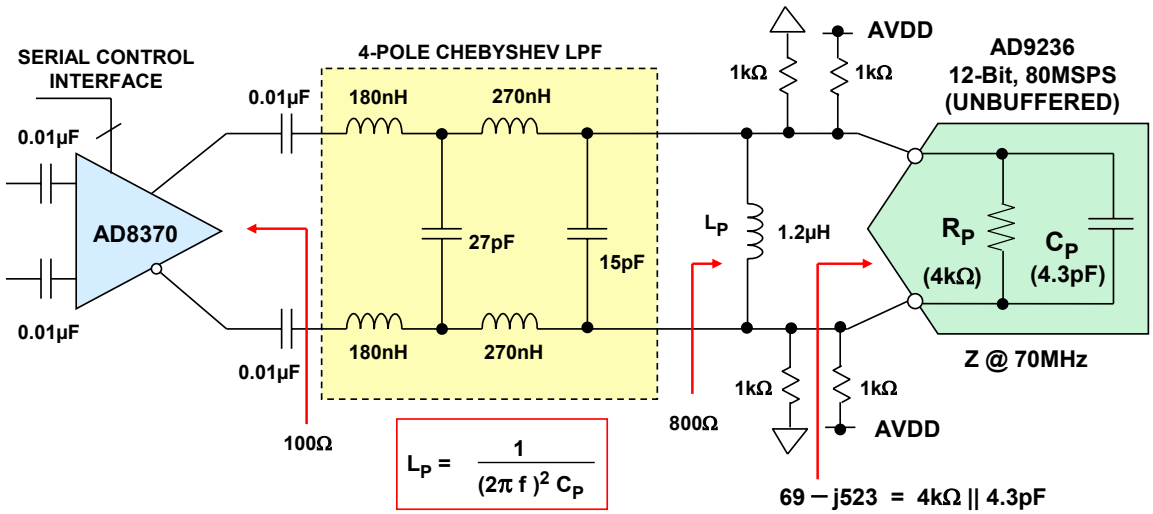
This design example is for a 70MHz IF frequency sampled at 76.8MHz (customer specified frequency). The sampling process downconverts the IF frequency to 6.8MHz. The AD9236 12-bit, 80MSPS ADC is driven with the AD8370 variable gain amplifier (VGA) followed by a 4-pole noise reduction lowpass filter.

The input impedance of the ADC at 70MHz is used to determine the value of the appropriate parallel resonant inductor, $L_P$. This transforms the input impedance of the ADC to a resistance at the IF frequency.

The lowpass filter is then designed based on the resistive source impedance of the amplifier, the equivalent resistive load of the ADC, and the desired filter transfer function.

The AD8370 is a programmable gain amplifier that has two ranges: −11dB to +17dB and +6dB to +34dB. The differential input impedance is 200Ω, and the differential output impedance is 100Ω. The AD8370 has 7dB noise figure at maximum gain, two-tone IP3 of +35dBm at 70MHz, 3dB bandwidth of 750MHz, and a 40dB precision gain range. It is controlled via a serial 8-bit digital interface and operates on a +3V to +5V power supply.

# AD8370/AD9236 Matching and Antialias Filter Interface Design for 70MHz IF




- **The resonant shunt inductor in combination with the 1kΩ bias resistors presents an ~ 800Ω differential load.**
- **The anti-aliasing filter is designed to be sourced from 100Ω and loaded into 800Ω and was optimized using a filter design program to use standard values and includes the effects of inductor parasitics.**

The final design for the 70MHz IF digitizer is shown in this figure. The first step is to determine the input impedance of the AD9236 at 70MHz. This data is available from an on-line spreadsheet and is 4kΩ in parallel with 4.3pF. The 1.2µH external parallel inductor resonates with the 4.3pF ADC capacitance at 70MHz and is calculated using the formula in the figure.

The four 1kΩ resistors are required to set the common-mode voltage for the differential inputs to the ADC. The four resistors form a 1kΩ differential resistance. The equivalent resistive load to the filter output is therefore 1kΩ||4kΩ = 800Ω.

The filter design is a fourth-order Chebyshev with 0.5dB ripple, 100Ω source, and 800Ω load. The cutoff frequency is set to 83MHz, and the filter is designed to give greater than 10dB attenuation at 100MHz. The values were adjusted to obtain standard value components and account for inductor parasitics. Other filter response types could be used here if desired, such as Butterworth.

Details of this type of resonant design using amplifier drivers can be found in Reference 1. The filters can be easily designed using a number of filter design programs as in Reference 2.

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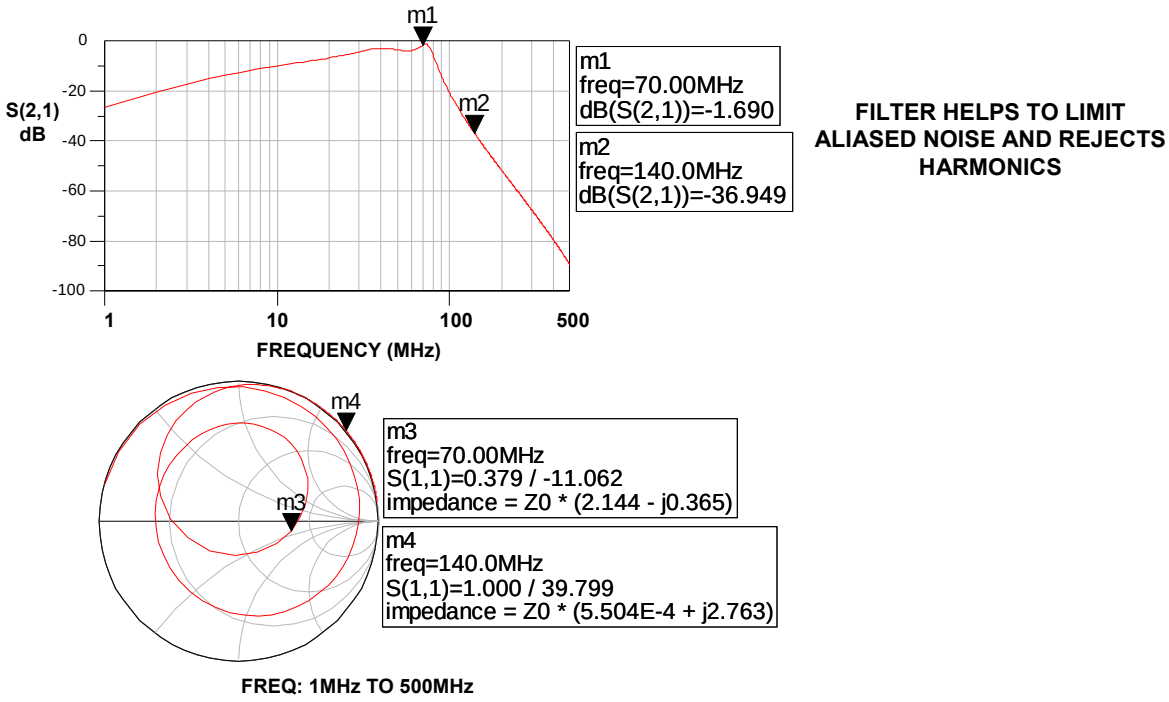
1. Eric Newman and Rob Reeder, "A Resonant Approach to Interfacing Amplifiers to Switch-Capacitor ADCs," *Application Note AN-827*, Analog Devices, www.analog.com.

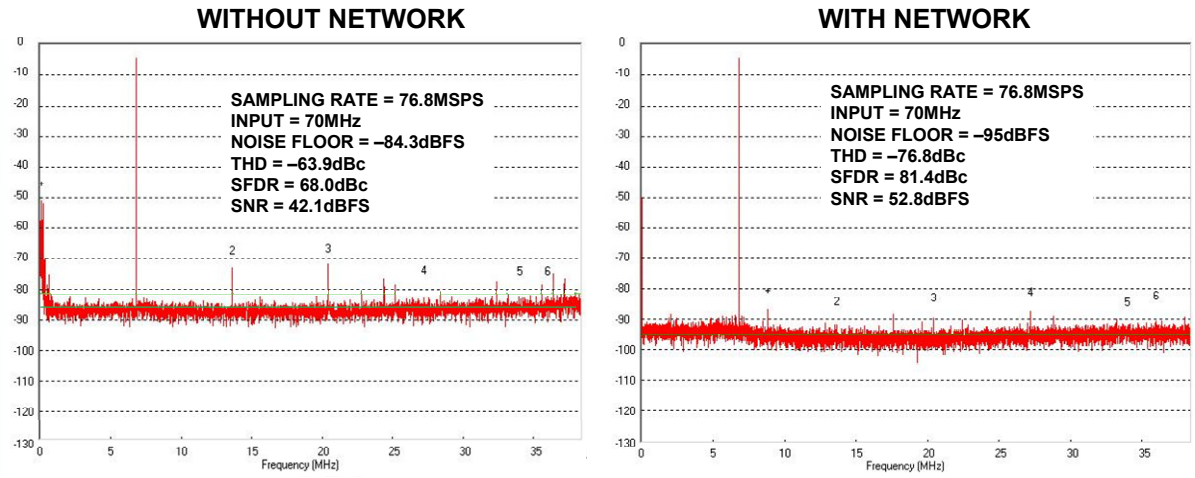
2. Filter design programs such as Filter Lite 5.0 from Nuhertz Technologies, or Agilent Technologies Advanced Design System (ADS).

# Simulated Response of Interface




This figure shows the simulated response of the entire interface, including the resonant inductor and the ADC input impedance. Also shown is a Smith chart of the input impedance to the filter.

# Before and After Adding Matching Analog Antialiasing Filter Network




- **SFDR Improved by 13.4dB, SNR improved by 10.7dB**
- **Note: Measured at maximum gain of 35dB (gain code 255, high gain mode) using 76.8MHz sampling clock**

This figure shows that adding the matching filter network improves the SFDR of the system by 13.4dB and the SNR by 10.7dB.

The improvement in SFDR is primarily because the load presented to the driving amplifier at 70MHz IF is resistive due to the resonant matching and is also a higher impedance than would be the case without the matching circuit. (The 4pF input capacitance has a reactance of 568Ω at 70MHz).

The improvement in SNR is primarily due to the filter bandlimiting the broadband noise to 80MHz. Otherwise the amplifier output noise would be integrated over the full 500MHz input bandwidth of the ADC.

# Wideband Design Example:

# AD8352 Variable Gain Amplifier Driving AD9445 14-Bit, 125MSPS Buffered Input ADC

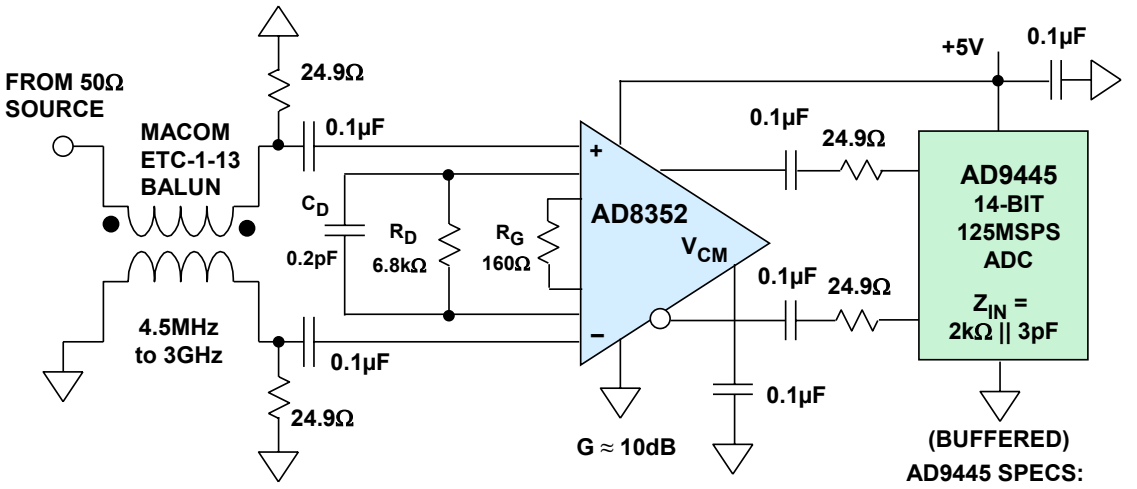
In this example, we are digitizing a wideband signal with the AD9445 14-bit, 125MSPS ADC and desire to preserve as much of the ADC input bandwidth as possible.

The AD9445 has 615MHz input bandwidth and an SFDR of 95dBc for a 100MHz input.

For the driver, we have chosen the AD8352 2GHz bandwidth differential amplifier because it has a resistor programmable gain range of 3db to 21dB. The amplifier also has low noise (2.7nV/√Hz referred to the input for a gain setting of 10dB) and low distortion (82dBc HD3 at 100MHz).

The lower end of the bandwidth requirement is approximately 10MHz.

# AD8352 2GHz Differential Amplifier Driving AD9445 14-Bit, 125MSPS ADC




- OUTPUT NOISE OF AD8352 FOR 10dB GAIN = 8.5nV/√Hz
- INTEGRATED OVER 615MHz INPUT BW OF AD9445 = 264µV rms
- INPUT REFERRED NOISE OF AD9445 = 158µV rms
- TOTAL NOISE = 307µV rms
- SNR = 67dB FOR 2V P-P INPUT

This shows the optimum circuit configuration for driving the AD9445 with the 2GHz AD8352 in a wideband application. The balun converts the single-ended input to differential to drive the AD8352. Although it is possible to configure the AD8352 to accept a single-ended input (see AD8352 data sheet), optimum distortion performance is obtained if it is driven differentially as shown.

The $C_D/R_D$ network is chosen to optimize the third-order intermodulation performance of the AD8352. The values are selected based on the desired gain and are given in the data sheet.

The performance of the circuit is shown in the next figure. Note that SFDR is 83dBc for a 98.9MHz input signal sampled at 105MSPS.

Noise performance can be predicted as follows:

The output noise spectral density of the AD8352 for G = 10 is 8.5nV/√Hz. Since there is no input filter, this must be integrated over the entire input bandwidth of the AD9445, 615MHz:

$$V_{NAMP} = 8.5nV/Hz\sqrt{(1.57\times615\times10^{6})} = 264\mu V \text{ rms.}$$

The input noise of the ADC is calculated from the SNR or 73dB:

$$V_{NADC} = 0.707\div10^{SNR/20} = 158\mu V \text{ rms.}$$

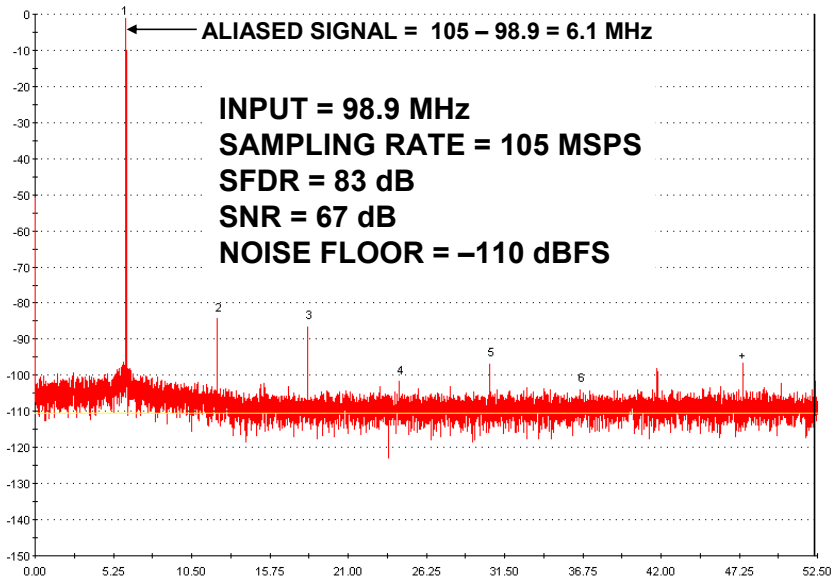
The total noise is calculated by:

$$V_{TOTAL} = \sqrt{(V_{NAMP}^{2} + V_{NADC}^{2})} = 307\mu V \text{ rms.}$$

This results in a combined system SNR of:

$$SNR = 20\log(0.707\div307\times10^{-6}) = 67dB$$

# FFT Data for AD8352 Driving AD9445
# Input = 98.9MHz, Sampling Rate = 105MSPS




This figure shows the FFT output for the AD8352 driving the AD9445 with an input signal of 98.9MHz and a sample rate of 105MSPS. The circuit is identical to the one in the previous figure.

SFDR is 83dBc, and SNR is 67dB, representing exceptional performance for this IF input frequency.

# Transformer Drivers

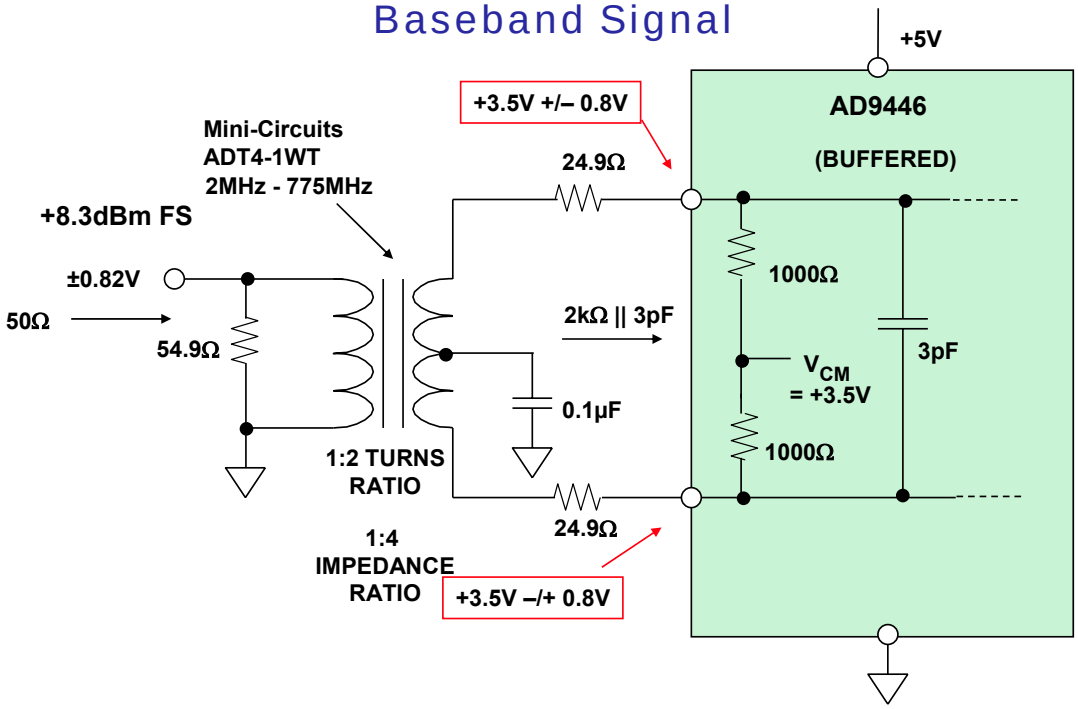
Transformers are popular ADC drivers in IF/RF applications. However, they are somewhat more difficult than amplifiers to analyze and apply as ADC drivers, and cannot pass dc or low frequency signals.

Transformers do not add additional noise to the system, but cannot generally be used for voltage gains more than two. In addition, they are somewhat difficult to analyze, and manufacturers do not typically provide detailed models on the data sheets.

The entire load on the transformer's secondary winding (including a noise filter if used) is reflected back to the primary winding. The resulting input load is therefore more difficult to control than that of an amplifier driver because output load of an amplifier is well isolated from its input.

The transformer is used as a single-ended to differential converter in many applications. At frequencies above about 100MHz, the parasitic capacitance between the primary and secondary windings can cause phase and amplitude unbalance which, in turn, can increase the distortion of the ADC. This may be remedied by either using a two-transformer configuration or using a higher performance transformer.

## Transformer Coupling into the AD9446 16-Bit, 80/100MSPS BiCMOS Buffered Input ADC, Baseband Signal




This figure shows a typical baseband transformer driver used as a single-ended to differential converter. The AD9446 16-bit, 80/100MSPS ADC is fabricated on a BiCMOS process, and has buffered inputs. Therefore, input transient currents are minimal.

The 24.9Ω resistors in series with the input isolate the transformer from the input capacitance of the ADC. The common-mode voltage of +3.5V is generated internally in the ADC.

This circuit uses a 1:2 turns ratio transformer for voltage gain. The total resistive load seen by the secondary of the transformer is 2000Ω + 24.9Ω + 24.9Ω = 2050Ω. This resistance is divided by 4 to reflect it to the primary winding as 512Ω. Therefore, in order for the input of the transformer to be a 50Ω termination for the signal, a 54.9Ω resistor is added in parallel with the equivalent 512Ω resistance.

For additional information regarding optimizing a transformer-coupled ADC input interface, refer to the following reference:

---

Rob Reeder,"Transformer-Coupled Front-End for Wideband A/D Converters," *Analog Dialogue*, Vol. 39, Number 2, 2005, www.analog.com.

# Differential Amplifiers vs. RF Transformer/Balun Drivers

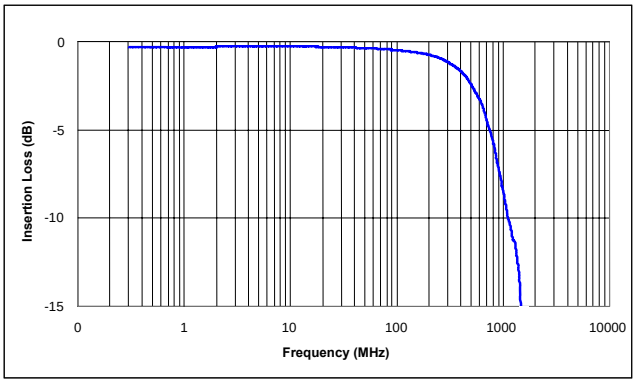
| DIFFERENTIAL AMPLIFIERS | RF TRANSFORMERS/BALUNS |
|---|---|
| Allow dc coupling, gain, offset adj. | Only work in ac-coupled apps. |
| Provide single-ended to differential conversion | Provide single-ended to differential conversion |
| Add noise | No additional noise added |
| Add distortion | Add less distortion |
| I/O Impedances well defined | I/O Impedance analysis difficult |
| Input isolated from output | Input and output interact |
| Add power to system | No additional power added |
| Can provide voltage gain | Gain > 2 difficult at IF frequencies |
| Good for baseband and medium IF frequency (up to 100MHz) | Good for baseband, medium, and high IF frequency |

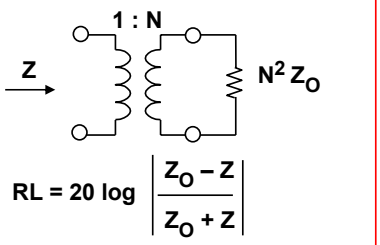
This figure compares differential amplifier drivers with transformer, or balun drivers. Note that a *balun* is a transformer with a bifilar winding and stands for "balanced-unbalanced." Baluns typically have higher bandwidth and lower parasitics than traditional RF transformers.

Transformers become difficult to use in low distortion applications requiring voltage gains greater than 2. On the other hand, differential amplifiers are capable of providing 10dB to 30dB voltage gain, depending on the device. The downside of differential amplifiers, of course, is the additional noise they add to the system.

# Transformer Insertion Loss and Return Loss

**Insertion Loss (Gain)**

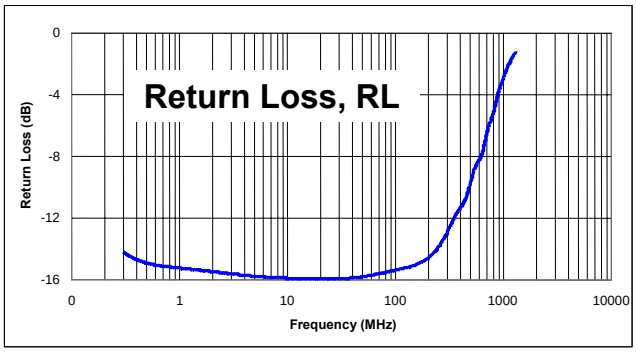



$$RL = 20 \log \left| \frac{Z_O - Z}{Z_O + Z} \right|$$

$Z_O$ = Ideal Input Impedance

$Z$ = Measured Input Impedance with Secondary Terminated in Ideal Value $N^2Z_O$




A transformer can be viewed simplistically as a bandpass filter. The transformer *insertion loss* is essentially a bandwidth specification, but it should not be the only consideration when designing with a transformer.

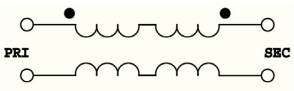
*Return Loss* is the effective impedance as seen by the primary when the secondary is terminated. For example, if you have an ideal 1:2 turns ratio (1:4 impedance ratio), transformer you would expect a 50Ω impedance reflected to the primary when the secondary is terminated with 200Ω. However, this is not always true. The impedance reflected to the primary varies with frequency. In general, as the turns ratio increases, so does the variability of the return loss. An example is shown on the next page.

The figure shows how to calculate the return loss. The secondary is terminated in a resistor equal to $N^2Z_O$, where N is the turns ratio, and $Z_O$ is the ideal transformer impedance. The actual input impedance is then measured, and this value is Z. The return loss, RL, is then calculated from the formula $RL = 20\log|[(Z_O - Z) / (Z_O + Z)]|$. The bottom graph in the figure shows the return loss plotted as a function of input frequency for a typical RF transformer.

It is important to know the return loss at the IF frequency of interest so that adjustments can be made in the terminations to make the actual input impedance reflected to the primary the correct value. This ensures a good match to the source and minimizes reflections due to impedance mismatch.

# Data for Mini-Circuits TC1-1-13M Balun

**Data Used by Permission of Mini-Circuits,**
**P.O. Box 350166, Brooklyn, New York 11235-0003**
**http://www.minicircuits.com**




## Transformer Electrical Specifications ($T_{AMB}$=25°C)

| Ω RATIO | FREQUENCY (MHz) | INSERTION LOSS* | | | PHASE UNBALANCE (Deg.) Typ. | | AMPLITUDE UNBALANCE (dB) Typ. | |
|---|---|---|---|---|---|---|---|---|
| | | 3 dB MHz | 2 dB MHz | 1 dB MHz | 1 dB bandwidth | 2 dB bandwidth | 1 dB bandwidth | 2 dB bandwidth |
| 1 | 4.5-3000 | 2000-3000 | 1000-2000 | 4.5-1000 | 2 | 3 | 0.5 | 0.5 |

* Insertion Loss is referenced to mid-band loss, 0.5 dB typ.

## Typical Performance Data

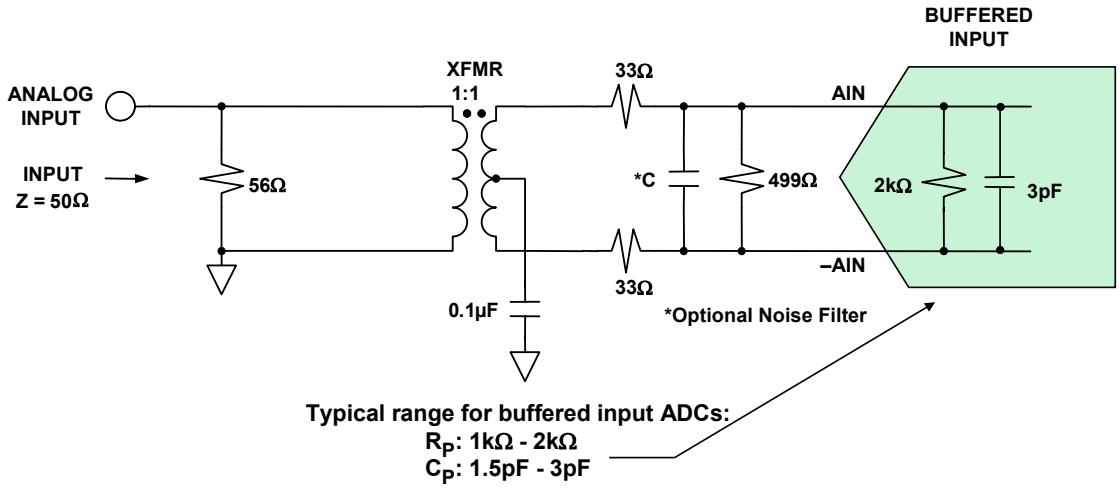
| FREQUENCY (MHz) | INSERTION LOSS (dB) | INPUT R. LOSS (dB) | AMPLITUDE UNBALANCE (dB) | PHASE UNBALANCE (Deg.) |
|---|---|---|---|---|
| 4.50 | 0.18 | 31.52 | 0.69 | 176.19 |
| 10.00 | 0.18 | 34.60 | 0.56 | 178.22 |
| 50.00 | 0.19 | 33.50 | 0.56 | 180.11 |
| 100.00 | 0.24 | 29.68 | 0.55 | 179.81 |
| 500.00 | 0.46 | 19.52 | 0.45 | 179.19 |
| 1000.00 | 0.68 | 16.22 | 0.14 | 178.41 |
| 1500.00 | 0.90 | 15.89 | 0.29 | 179.11 |
| 2000.00 | 1.11 | 16.97 | 0.71 | 181.28 |
| 2500.00 | 1.62 | 12.88 | 0.78 | 185.79 |
| 3000.00 | 3.02 | 6.79 | 0.49 | 167.68 |

Turns ratio, insertion loss (gain), and return loss are three commonly specified transformer parameters as shown in this figure. Amplitude and phase unbalance may also be specified.

However, the parasitic inductances and capacitances associated with the transformer are rarely specified on the manufacturer's data sheet. In some cases these parameters can be obtained by contacting the manufacturer directly. Otherwise, estimates or actual measured values can be used. In most cases some optimization in the actual circuit is required regardless of the simulation results.

# Baseband Sampling Applications for Buffered Input ADCs

- The input interface for buffered ADCs is fairly simple to design
- When IFs are ≥ 100MHz, 2nd-order distortions begin to rise because the of transformer's amplitude and phase imbalance
- To solve this problem two transformers may be needed (see next page)




This figure shows a generic buffered input ADC driven by a transformer in a baseband application, where the input signal has a bandwidth up to $f_S/2$. The buffered ADC input impedance is 2kΩ in parallel with 3pF. The secondary termination is split between the 499Ω parallel resistor and the two 33Ω series resistors. The 33Ω series resistors isolate the secondary winding from the ADC input capacitance and the 499Ω resistor reduces the effects of the 3pF input ADC input capacitance.

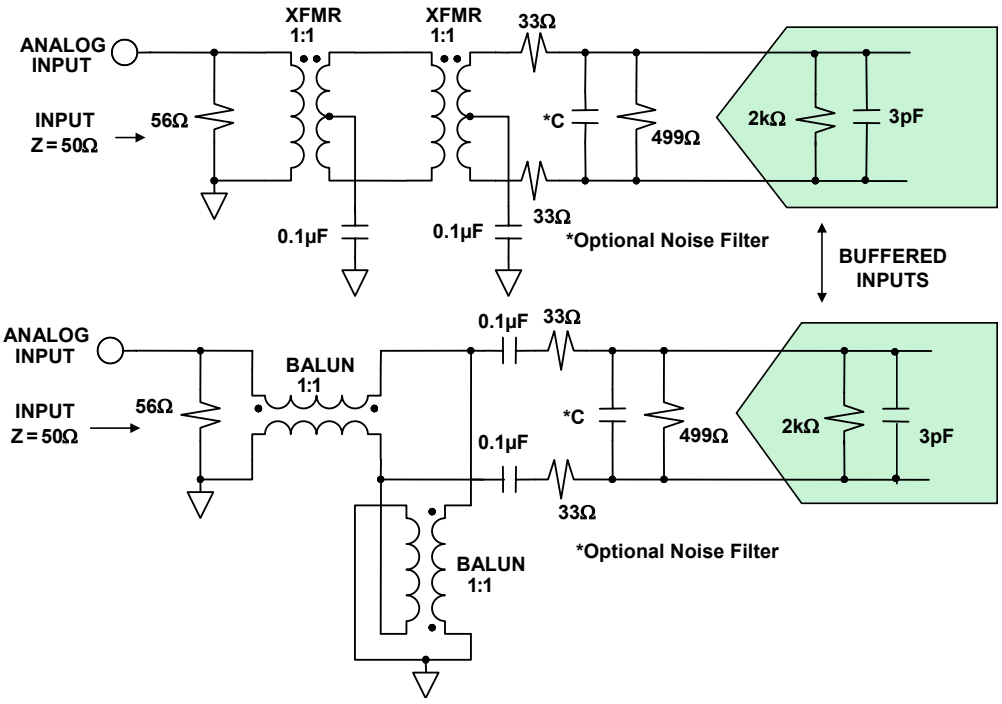
The 499Ω resistor in parallel with the 2kΩ ADC resistor forms a 400Ω equivalent resistor. This makes the net secondary resistive load equal to 33Ω + 33Ω + 400Ω = 466Ω. This is reflected to the primary as 466Ω, since the transformer is 1:1. The 56Ω input resistor in parallel with 466Ω gives a net input termination resistance of 50Ω.

Most buffered input ADCs provide an internal dc common-mode bias voltage on the two inputs, so there is no need for an external bias network, as in the case of unbuffered input ADCs.

The center tap of the secondary winding is decoupled to ground to ensure that the input to the ADC is balanced.

A small capacitor, C, can be added to filter high frequency noise if desired.

# Double Transformers/Baluns May Improve Performance of Buffered ADCs for IF Frequencies > 100MHz




For IF frequencies above about 100MHz, the parasitic capacitance between the primary and secondary windings of the transformer may cause enough amplitude and phase unbalance to affect second-order distortion performance. The major reason for this unbalance is because one side of the primary winding is grounded and has no signal while the other side of the winding is driven by the signal and can couple into the secondary through the parasitic capacitance.

This problem can be addressed in two ways. One solution is to select a higher performance transformer (at additional cost) with better phase and amplitude balance.

Another solution is to add a second transformer (or balun) as shown in the figure. The second transformer serves to "distribute" the unbalance between the two transformers, thereby reducing the overall unbalance.

Regardless of the approach selected, some experimentation is required in order to achieve the optimum performance.

Details of the double transformer approach can be found in the reference.

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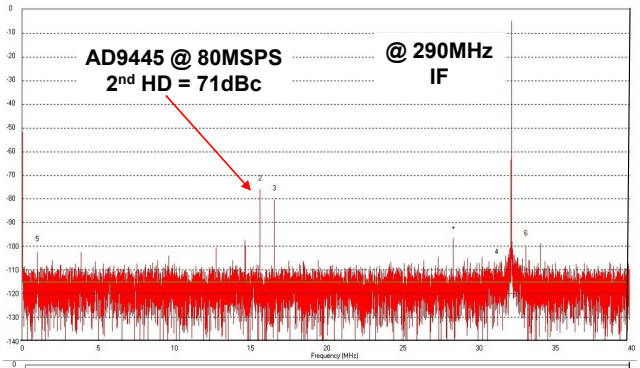
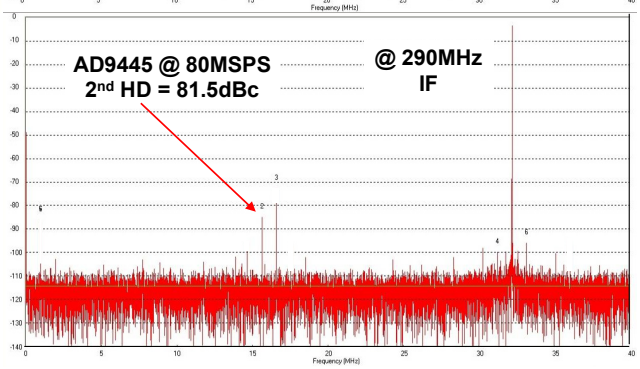
Rob Reeder and Ramya Ramachandran, "Wideband A/D Converter Front-End Design Considerations – When to Use a Double Transformer Configuration," *Analog Dialogue* Vol. 40, Number 3, 2006, Analog Devices, www.analog.com.

# Double Transformer Improves 2nd Harmonic Distortion by 10.5dB at 290MHz IF

SINGLE



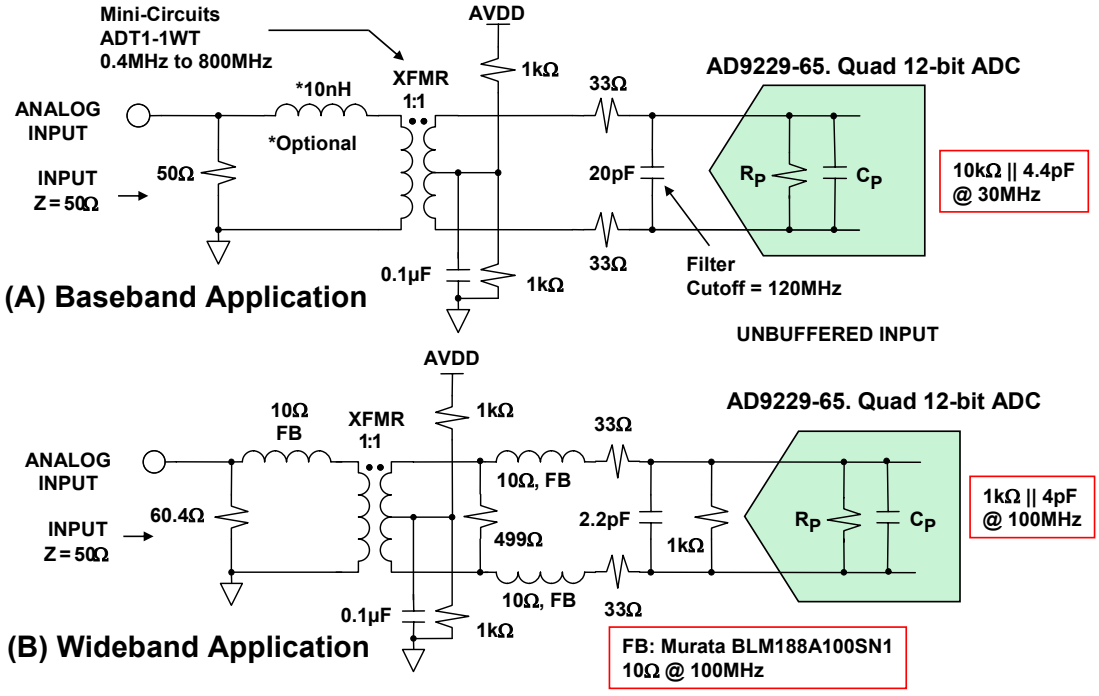

DOUBLE




Here is an example using the AD9445-125MSPS ADC sampling at 80MSPS with an input frequency of 290MHz. Note the second harmonic is 71dBc. This data was gathered using a single 1:1 impedance ratio transformer on the front end.

Adding a second transformer reduces the second harmonic to 81.5dBc, an improvement of 10.5dB.

# Switched-Capacitor ADC Input Configurations for Wideband Signals




This figure shows two examples of unbuffered ADC input configurations: baseband and wideband.

In baseband applications (A), the analog input frequency to the ADC is less than $f_S/2$, and the resistive component of the ADC input impedance is high. This makes the input circuit easier to design. The two 33Ω resistors isolate the transformer from the ADC input transient currents as well as form a simple noise filter with the 20pF differential capacitor. The cutoff frequency is approximately 120MHz.

For baseband applications an inductor in series with the transformer's primary can be used to alter the bandwidth response of the transformer by peaking the gain in the passband and providing a steeper rolloff outside the passband. The inductor has the effect of adding a pole in the transfer function. The value of inductance depends on the desired amount of peaking and bandwidth requirement. However, the designer should note that this peaking can be undesirable where flatness of response and well-behaved phase response are important criteria.

For wideband signals which extend well beyond $f_S/2$, the design becomes more critical. In (B) the secondary resistive termination is split between $R_p$, the 1kΩ resistor, the 499Ω resistor, and the 33Ω series resistors. The net secondary termination is 265Ω. The 60.4Ω input resistor in parallel with the 265Ω equivalent resistance yields the desired 50Ω input termination.

The two series ferrite beads have been added to minimize gain peaking at the higher IF input frequencies. The part selected has a resistance of 10Ω at 100MHz. Determining the optimum ferrite bead generally involves some empirical work.

---

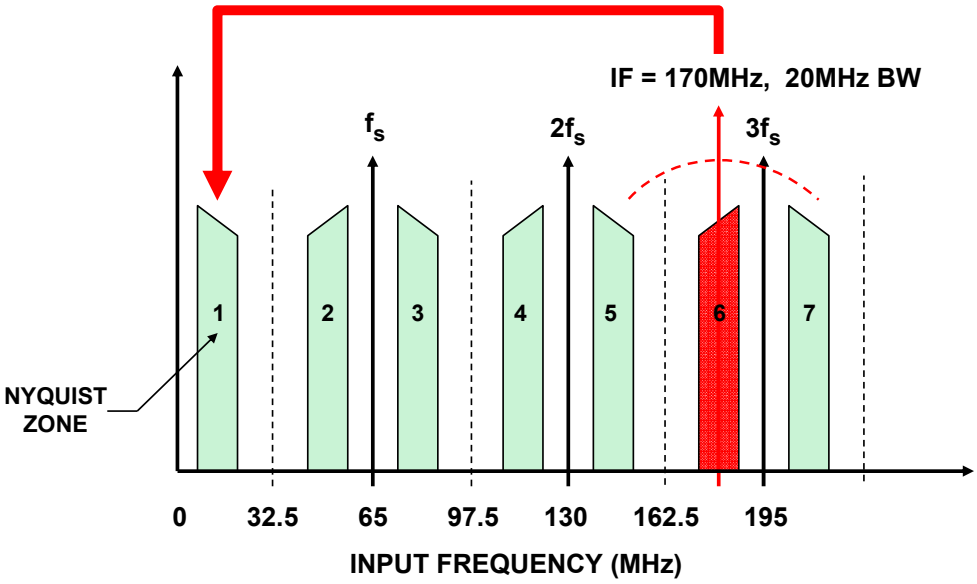
Rob Reeder, "Transformer-Coupled Front-End for Wideband A/D Converters," *Analog Dialogue*, Vol. 39, Number 2, 2005, Analog Devices, www.analog.com.

# Transformer Driver Resonant Matched Design Example: Unbuffered CMOS ADC, IF = 170MHz, Sampling Rate = 65MSPS

This design example is typical of the process required to optimize a transformer driven unbuffered CMOS ADC operating on an IF frequency. Resonant matching is used to optimize the response at the desired IF frequency. The system specifications represent those of an actual customer.

In this design, a 170MHz IF is digitized at a 65MSPS sampling rate. The bandwidth of the IF signal is 20MHz.

## Design Example: 170MHz IF Signal Sampled at 65MSPS




This figure shows the frequency spectrum of the 170MHz IF signal sampled at 65MSPS. The IF signal lies in the sixth Nyquist zone. The sampling process downconverts it to the first Nyquist zone as shown.

The actual bandwidth of the signal is 20MHz and, therefore, a sampling rate of at least 40MSPS is required. In this example, the sampling rate was selected to be 65MSPS.

# Design Example: Design Requirements and ADC Requirements

## Design Requirements

| | Input Impedance (Ohm) | VSWR | Passband Flatness (dB) | –3dB IF BW (MHz) | SNR (dBc) | SFDR (dBc) | Input Drive Level (dBm) |
|---|---|---|---|---|---|---|---|
| Ideal Value | 50 | 1 | 0.5 | 100 | 74 | 90 | 5 |
| Design Limit | 20 | 2 | 3 | 200 | 65 | 70 | 12 |

## ADC Requirements

**Sample Rate = 65MSPS**
**SNR = ≥ 65dB**
**IF = 170MHz**
**Band = 20MHz (160-180MHz)**

**AD9238, 12-bit, 65MSPS, 3V, Dual ADC**
**Input Bandwidth = 500MHz**
**Unbuffered CMOS Switched Capacitor Input Structure**

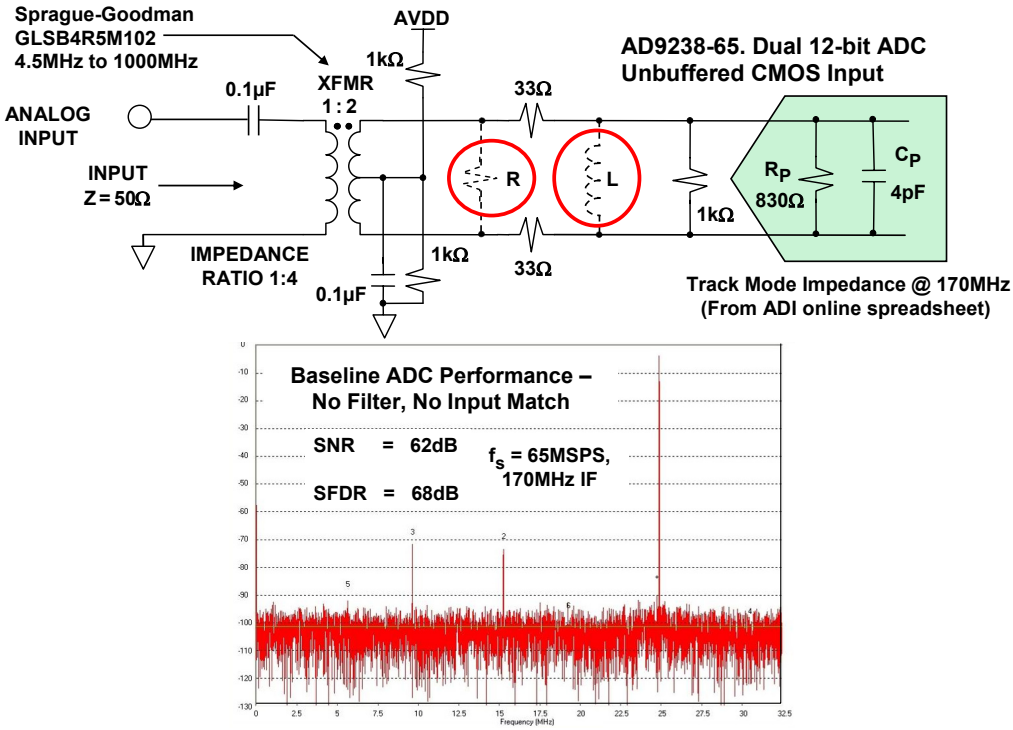
The basic design requirements and ADC requirements are presented in these tables. The IF frequency is 170MHz, and the bandwidth is 20MHz (160-180MHz). Input impedance is important in IF systems because mismatches reduce the amount of power transferred. Attention to input impedance is especially important in transformer drivers, because all of the load on the secondary is reflected back to the primary. The input impedance should not only be the proper value but should be primarily resistive at the IF frequencies of interest. This is quite different from an amplifier driver, where the output is relatively isolated from the input.

The desired passband flatness in the IF bandwidth (160-180MHz) is 0.5dB with a 3dB upper limit. The desired 3dB IF bandwidth is 100MHz, but 200MHz is acceptable. SNR should be between 65dB and 74dB, and SFDR between 70dB and 90dB. Input drive level should be no greater than +12dBm.

The system sampling rate was selected to be 65MSPS based on the 20MHz IF bandwidth. In order to achieve greater than 65dB SNR, a 12-bit ADC is required. The AD9238 12-bit, 65MSPS CMOS ADC was selected. This ADC has an unbuffered switched capacitor input structure as previously discussed. The input bandwidth of the AD9238 is 500MHz which is sufficient to handle the 170MHz IF input.

The AD9238 is a dual ADC and operates on a single +3V power supply.

# Design Example: AD9238 Switched Cap ADC Baseline Performance Without R and L




This figure shows the basic circuit without resonant matching as well as its performance when sampling a 170MHz IF signal at 65MSPS. SNR is 62dB, and SFDR is 68dB.

From the Analog Devices' online spreadsheets, the track mode impedance of the AD9238 is $R_P$ = 830Ω in parallel with $C_P$ = 4pF for an IF input frequency of 170MHz.

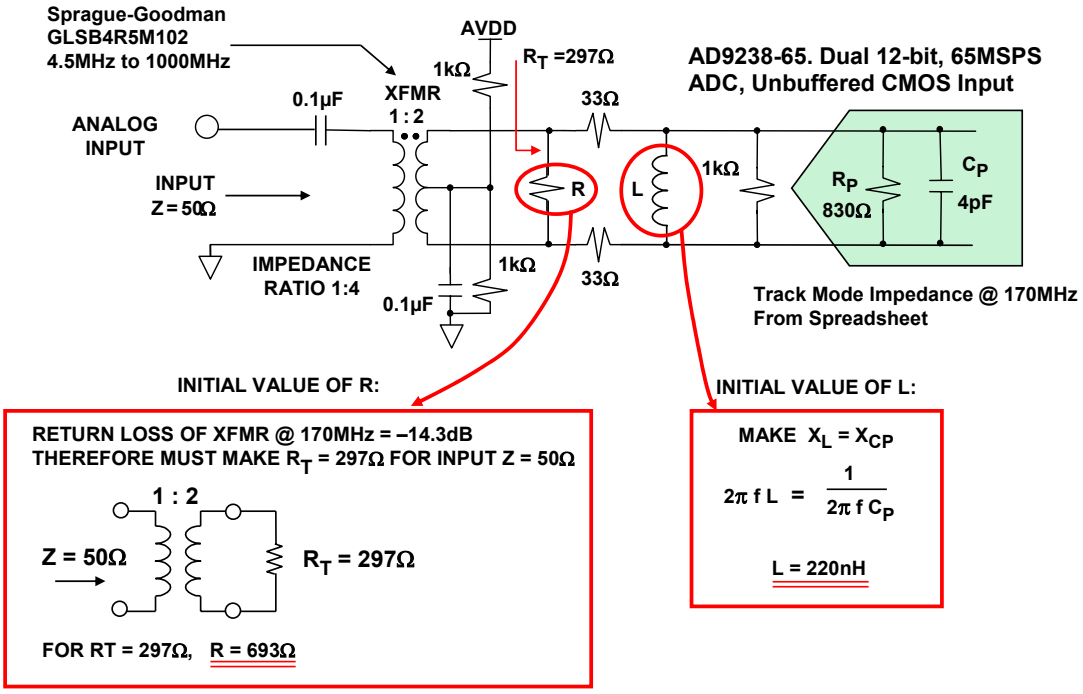
The 1kΩ differential resistor is to de-Q the parasitic $C_P$ on the ADC. The 33Ω series resistors inserted in series with each analog input aid in reducing the charge injection kickback into the transformer.

The transformer selected is a Sprague-Goodman, part number GLSB4R5M102 which has a turns ratio of 1:2 and an impedance ratio of 1:4.

The objective is to select the values of the parallel L to resonate with the 4pF capacitor at 170MHz and to select the value of R to make the overall input impedance 50Ω.

It should be emphasized that the process requires some experimental optimization, primarily because an exact model for the transformer parasitic inductances, resistances, and capacitances is not available. PC board parasitics also affect the optimum values.

# Design Example: Determining Initial Values of Shunt R and L




Selecting the initial value of L is a simple process of setting $X_L = X_{CP}$ and solving for L with f = 170MHz as shown in the figure. The value obtained is L = 220nH.

The return loss of the transformer at 170MHz is –14.3dB. This means that a net termination resistance of 297Ω (rather than the expected value of 200Ω) is required to make the effective input impedance 50Ω. The proper value for $R_T$ is calculated as follows.

The equation for return loss is: $RL = 20\log|(Z_O - Z)/(Z_O + Z)|$. Substitute RL = –14.3dB, and solve the equation for Z. The result is $Z = 0.673Z_O$. This says that if the secondary is terminated in the theoretically ideal value of 200Ω, the input impedance is actually 0.673×50Ω = 33.65Ω. Therefore, the secondary must be terminated in 297Ω in order to make the actual input impedance 50Ω.

Without the resistor R, the net resistive termination on the secondary of the transformer is equal to:

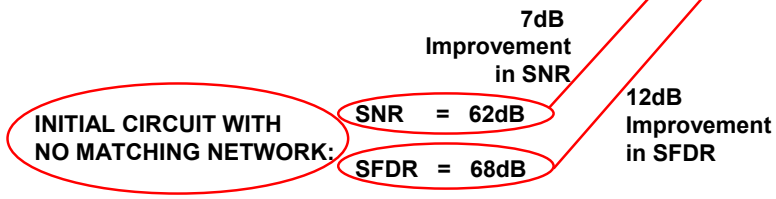
$$830\Omega||1000\Omega + 33\Omega + 33\Omega + \ = 519.5\Omega.$$

Therefore, R must be 693Ω in order to make the net termination resistance 297Ω. This is the starting point of the design.

# Design Example: AD9238 Switched Cap ADC – Iterate to Achieve Performance

**IF = 170MHz, $f_s$ = 65MSPS**

| DESIGN REQUIREMENTS | REV 1 | REV 2 | REV 3 | REV 4 - Final |
|---|---|---|---|---|
| R \|\| L | 693Ω \|\| 220nH | 400Ω \|\| 120nH | 560Ω \|\| 240nH | 620Ω \|\| 120nH |
| Input Impedance (50Ω) | 47 | 23 | 32 | 48 |
| VSWR (1-2) | 1.06 | 2.17 | 1.56 | 1.04 |
| Passband Flatness (0-3dB) | 4.04 | 1.5 | 2.8 | 0.17 |
| IF –3dB Bandwidth (100-200MHz) | 174 | 174 | 214 | 150 |
| SNR (65-74dB) | 69 | 69 | 69 | 69 |
| SFDR (70-90dB) | 73.5 | 77 | 78 | 80 |
| Input Drive Level (5-12dBm) | 9.06 | 7.6 | 5.8 | 5.9 |

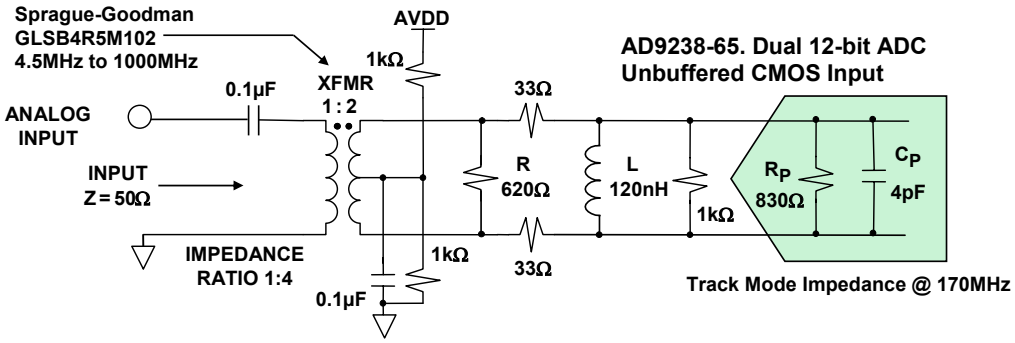



This shows the results of four interations of the design, starting with the calculated values of R and L. The final values (REV 4) yield performance within the required limits.

The primary reason for the interative design process is the lack of a good model for the transformer.

Note that the addition of the proper resonant matching network improves the SNR by 7dB and the SFDR by 12dB.

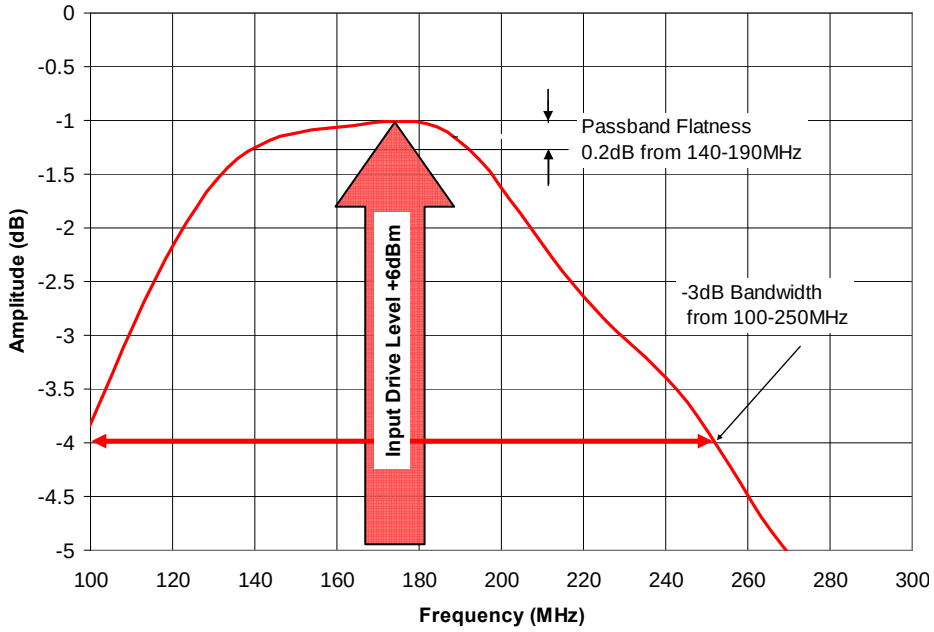
# Design Example: Final Configuration for Input Resonant Match



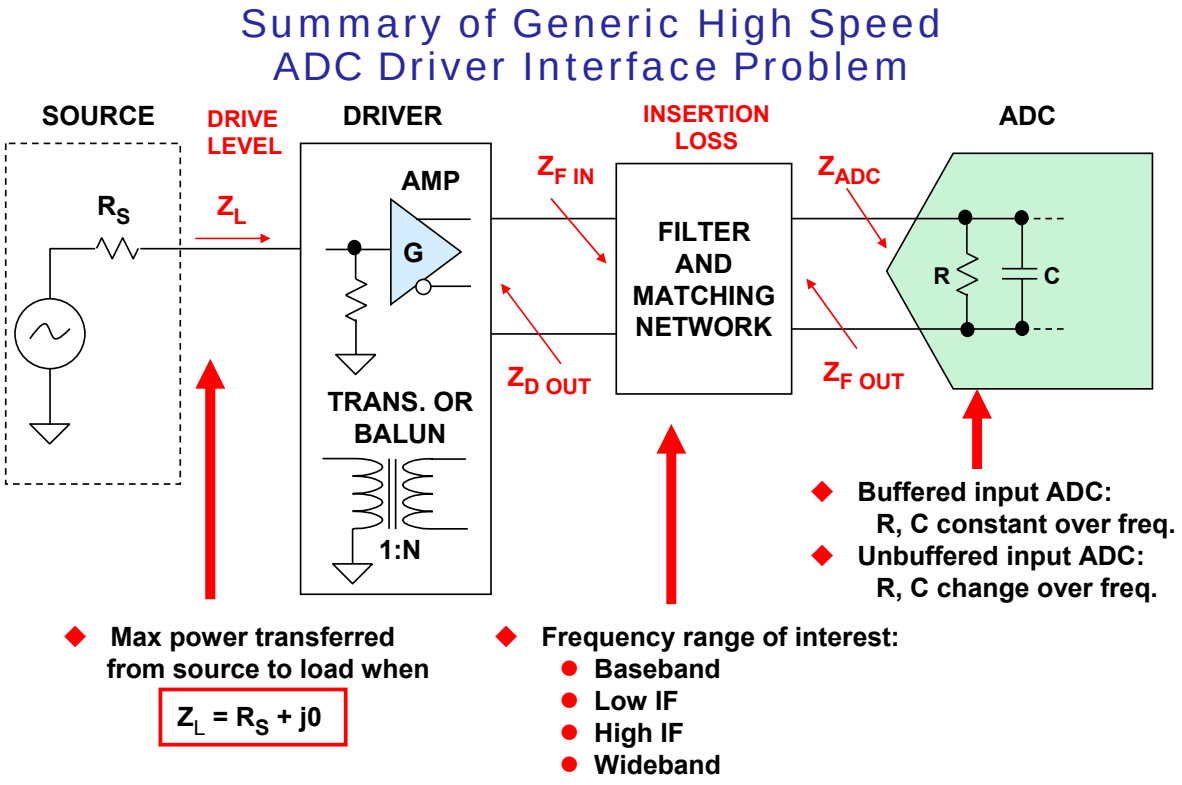

| | BEFORE MATCH | AFTER MATCH | CHANGE |
|---|---|---|---|
| SNR | 62dB | 69dB | +7dB |
| SFDR | 68dB | 80dB | +12dB |

This figure shows the final design and the improvement achieved by resonant matching.

# Design Example: AD9238 Switched Cap ADC - Final Results – Bandwidth & Passband Flatness




This figure shows the response of the interface. Note that the passband flatness is 0.2dB from 140MHz to 190MHz, and the 3dB bandwidth is 150MHz.




This figure summarizes the various considerations involved in designing the ADC analog input interface.

Amplifier drivers provide good isolation between the ADC input circuit and the signal source, and also provide signal gain if required. Current state-of-the-art differential amplifier output noise performance is approximately 5nV/√Hz.

Transformer drivers present more of a design problem because the secondary load is always reflected to the primary. In addition, good models containing transformer parasitics are not always available. However, transformers do not add additional noise to the system.

In this section we have also shown how resonant matching improves the dynamic performance in IF sampling applications. Dynamic ADC input impedance values are available which allow the design to be optimized at the desired IF frequency.

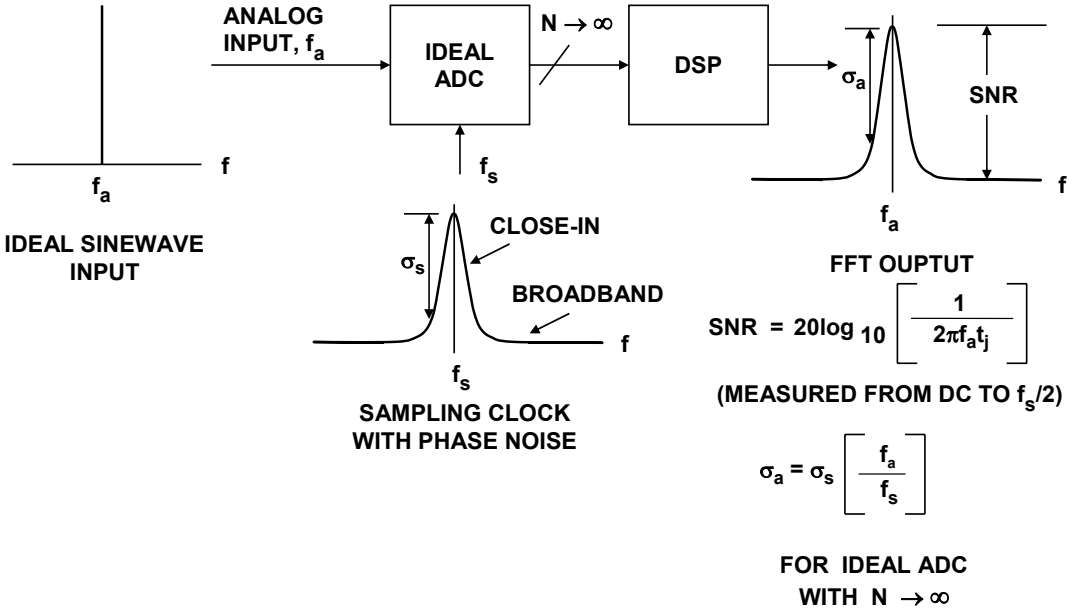
The filter and matching network requirements for baseband and broadband applications have also been discussed in this section.

# References

1. Rob Reeder, "Frequency Domain Response of Switched-Capacitor ADCs," *Application Note AN-742*, Analog Devices, www.analog.com.
2. Eric Newman and Rob Reeder, "A Resonant Approach to Interfacing Amplifiers to Switch-Capacitor ADCs," *Application Note AN-827*, Analog Devices, www.analog.com.
3. Rob Reeder, "Transformer-Coupled Front-End for Wideband A/D Converters," *Analog Dialogue*, Vol. 39, Number 2, 2005, Analog Devices, www.analog.com.
4. Rob Reeder, Mark Looney, and Jim Hand, "Pushing the State of the Art with Multichannel A/D Converters," *Analog Dialogue,* Vol. 39, Number 2, 2005, Analog Devices, www.analog.com.
5. Rob Reeder and Ramya Ramachandran, "Wideband A/D Converter Front-EndDesign Considerations – When to Use a Double Transformer Configuration," July Issue, *Analog Dialogue*, Vol. 40, Number 3, 2006, Analog Devices, www.analog.com.
6. ADC Input S-parameter data:
   Go to product webpage, click on "Evaluation Boards," upload
   S-parameter data in a spreadsheet (where available).

# Sampling Clock Drivers

# Effect of Sampling Clock Phase Noise on Ideal Digitized Sinewave




This figure shows an ideal ADC digitizing an ideal sinewave where the only error is phase noise on the sampling clock. Note that the sampling clock phase noise appears on the reconstructed sinewave output of the FFT. This is because of the inherent mixing that occurs between the sampling clock and the input signal.

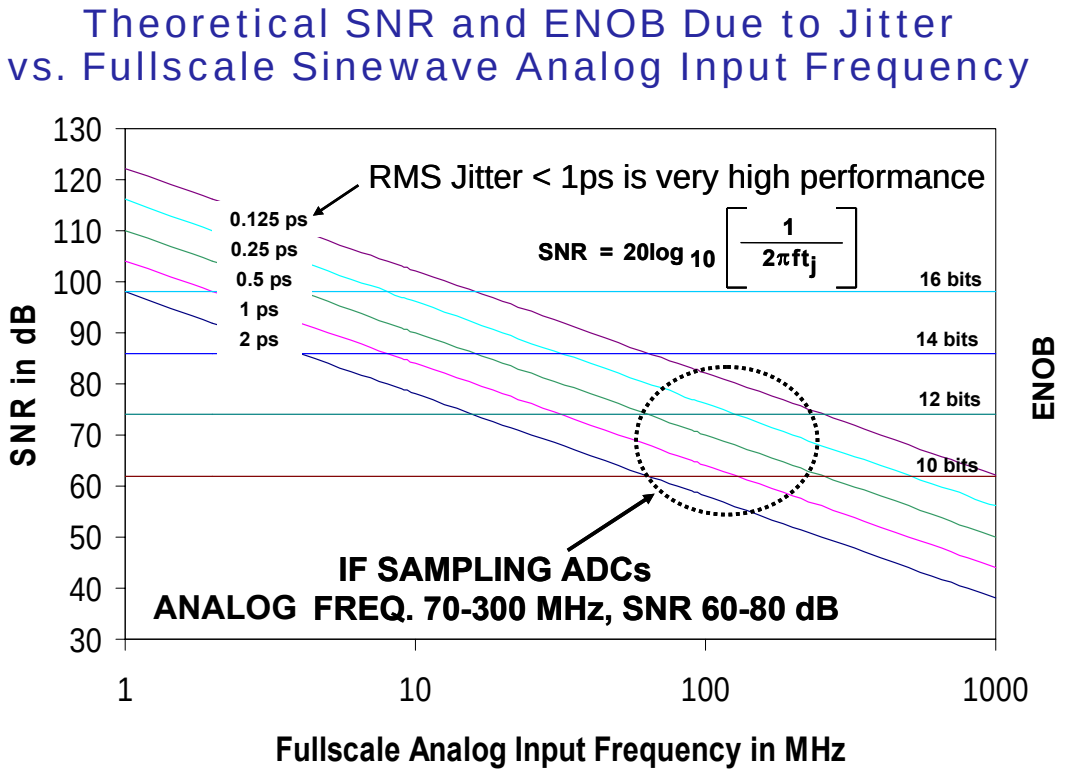
The figure also shows that the overall SNR (measured from dc to $f_S/2$) due to broadband sampling clock jitter for an ideal ADC ($N \rightarrow \infty$) is given by the familiar equation,

$$SNR = 20\log[1/2\pi f_a t_j],$$

where f is the input frequency and $t_j$ is the total broadband clock jitter.

The total broadband jitter is made up of the external clock jitter and the aperture jitter of the ADC itself. Although the two components combine on an rss basis, the external clock jitter is typically the dominant component and the most often neglected.

The figure also shows how the output phase noise is a scaled version of the clock phase noise and underscores the importance of phase noise in undersampling applications where $f_a > f_S$.




This figure plots the equation for jitter-based SNR and shows SNR on the left and ENOB (effective number of bits) on the right. They are related by the simple equation SNR = 6.02N + 1.76dB, where N = ENOB.

Note that for a fullscale 30MHz input, 14-bit ENOB requires that the rms jitter be no more than 0.3ps, or 300fs.

The equation assumes an ADC of infinite resolution, where the only error is the noise produced by the clock jitter.

IF sampling ADCs typically operate on IF frequencies between 70MHz 300MHz. The required SNR is typically between 60dB and 80dB.

Clock jitter less than 1ps rms represents a high performance clock.

# Additive RMS Jitter of Logic Gates/Drivers

| | |
|---|---|
| ◆ **FPGA (driver gates only, not including internal gates or dll/pll)** | **33-50 ps**** |
| ◆ **74LS00** | **4.94 ps *** |
| ◆ **74HCT00** | **2.20 ps *** |
| ◆ **74ACT00** | **0.99 ps *** |
| ◆ **MC100EL16 PECL** | **0.7 ps **** |
| ◆ **AD951x family** | **0.22 ps **** |
| ◆ **NBSG16, Reduced Swing ECL (0.4V)** | **0.2 ps **** |
| ◆ **ADCLK9xx, ECL Clock Driver Family** | **<0.1 ps**** |

*** Calculated values based on degradation in ADC SNR**
**** Manufacturers' specification**

To put jitter in perspective, this shows the typical rms jitter of several types of standard logic gates.

If several gates are put in series, the total rms jitter is the root-sum-square (rss) of the individual gate jitter. Four similar gates in series yields a jitter of $\sqrt{4} = 2$ times the jitter of each individual gate.

The data for the 74-series was obtained by measuring the degradation in an ADC SNR due to the addition of the gates in the sampling clock path. The 74-series is typically not specified for jitter.

The MC100EL16 and NBSG16 gates shown represent manufacturer's specifications.

The new Analog Devices' ADCLK9xx-series of drivers has less than 0.1ps rms jitter.

A high performance low jitter ADC test set can be used to measure the external clock jitter. This measurement technique is described further in the following reference:

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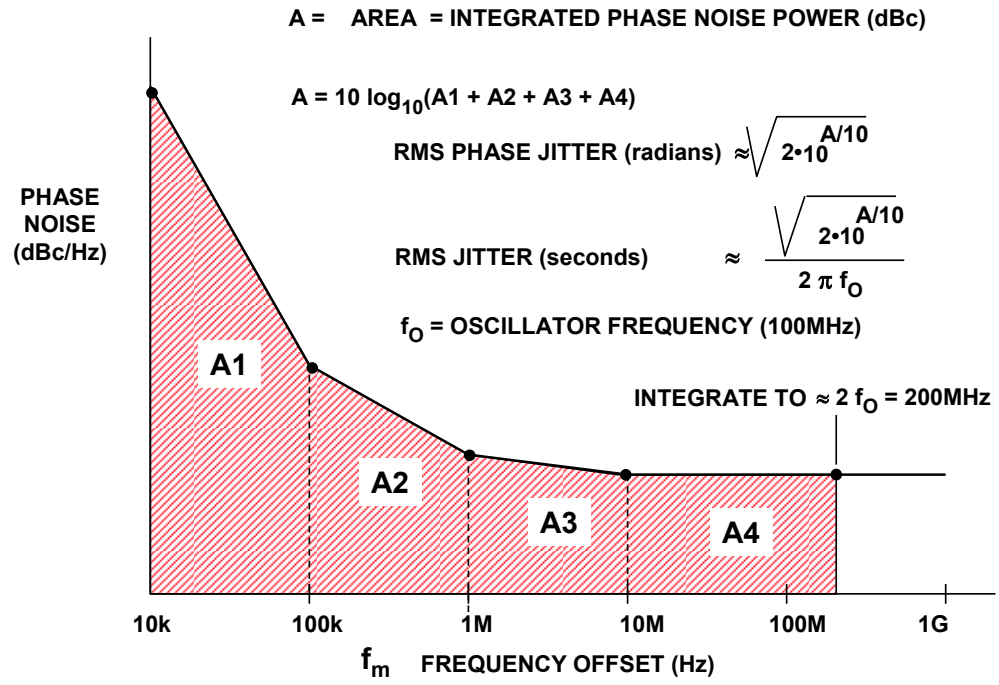
Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN-0916550273 Chapter 5. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410, Chapter 5.

# Calculating Jitter from Phase Noise




Most oscillators specify phase noise rather than jitter. Phase noise can be converted into jitter by integrating the phase noise over frequency as shown in this figure.

The process is quite similar to converting the voltage noise spectral density of an op amp into an rms voltage.

Note that the individual areas A1, A2, A3, and A4 are each expressed as ratios of phase noise power/carrier power. Therefore, they can be added directly.

The value for integrated phase noise power in dBc is obtained by A = 10log10(A1+A2+A3+A4).

The lower bandwidth of integration depends on the specified low frequency resolution of the system.

The upper limit for the integration should be approximately twice the oscillator frequency (or sampling clock frequency in the case of sampled data systems). This is a reasonable approximation to the bandwidth of the ADC clock input, and the actual number used is not that critical to the final result. This also assumes that there is no filter between the oscillator and the ADC sampling clock input.

Spreadsheet programs are available to make these calculations by simply inputting the various data points. The ADIsimPLL program will also convert phase noise into jitter.

More details on converting phase noise into jitter can be found in the following reference:

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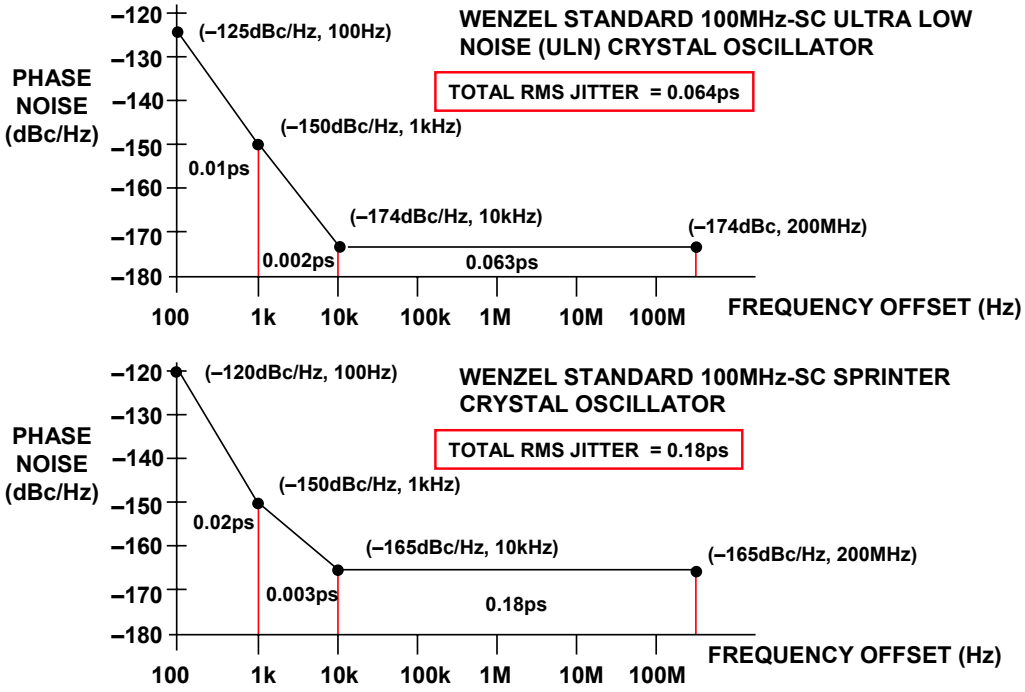
Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN-0916550273 Chapter 6. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410, Chapter 6.

## Jitter Calculations for Low Noise 100MHz Crystal Oscillators
(Phase Noise Data Used with Permission of Wenzel Associates)



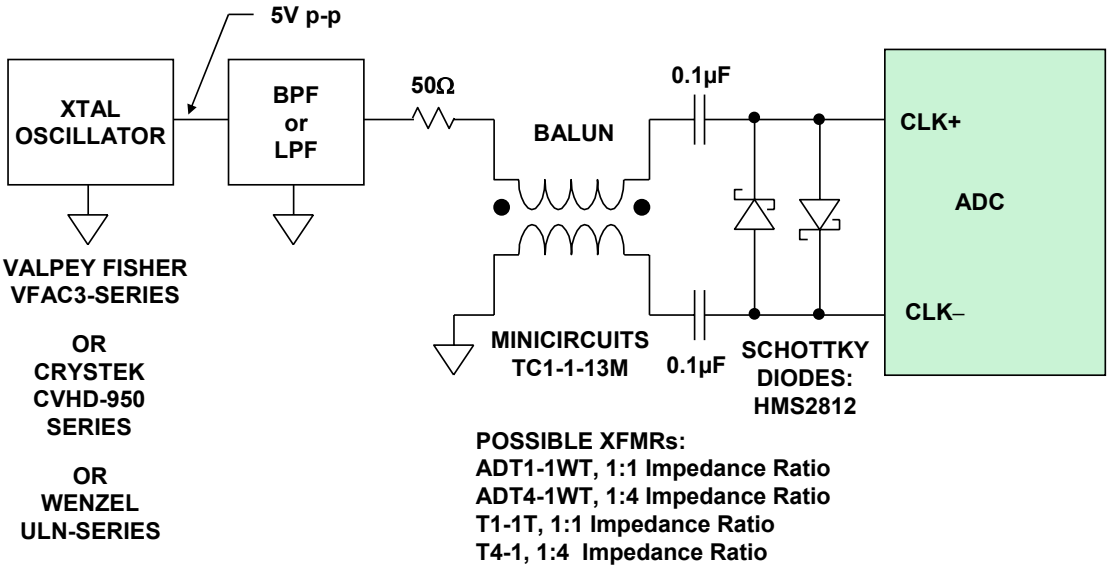

This figure shows the phase noise of two high quality crystal oscillators from Wenzel Associates. The graph is broken up into regions, and the jitter in each region is calculated along with the total jitter. The overall jitter is primarily determined by the "broadband" region.

The top graph is for the ULN-series and the calculations yield 64fs rms jitter.

The bottom graph is for the Sprinter-series oscillator and is about three times worse at 180fs.

In most cases the broadband component dominates the total jitter, and a reasonable approximation can be made by simply integrating the rectangular portion of the curve.

# Ultra Low Jitter (<100 fs) Differential Clock Source



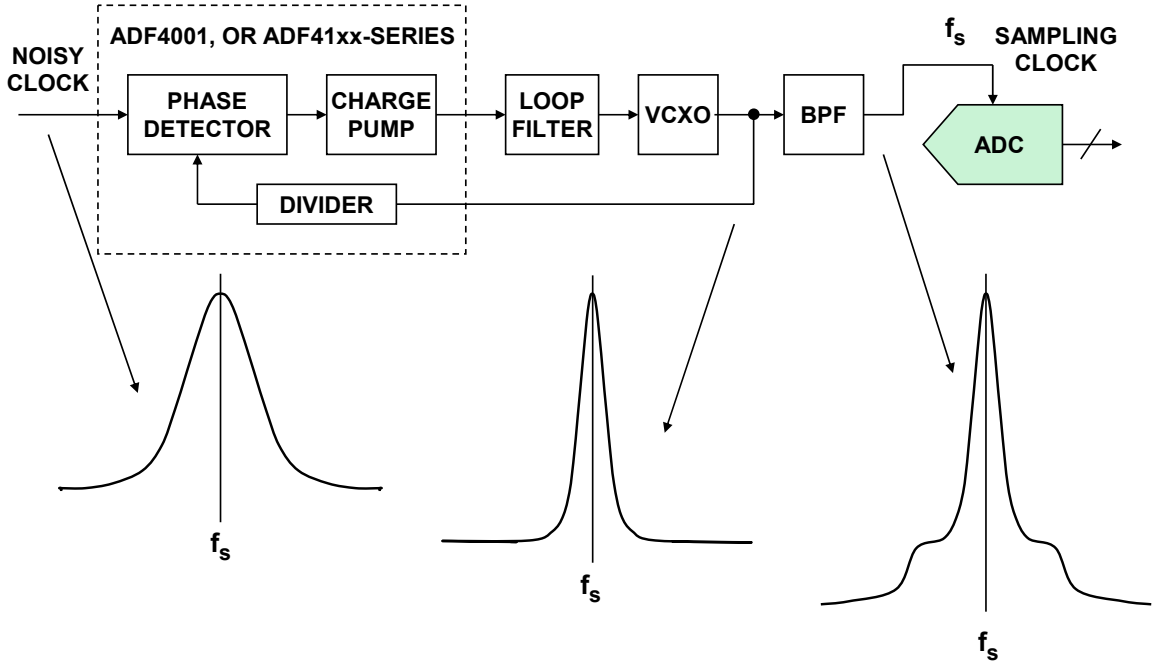

This figure shows a method for generating a sampling clock with less than 100fs jitter. The crystal oscillator is either a Valpey Fisher VFAC3-series (www.valpeyfisher.com), Crystek CVHD-950-series (www.crystek.com) or a Wenzel ULN-series (www.wenzel.com).

The output of the oscillator is filtered with either a lowpass or bandpass filter to remove harmonics and noise. A bandpass filter should be used for fixed frequency applications, but a lowpass filter allows some adjustment of the sampling clock frequency.

The single-ended filtered output must then be converted into a differential signal to drive the sampling clock input of the high speed ADC. This conversion can be performed using a balun or a transformer.

The output of the transformer is clamped with fast recovery Schottky diodes in order to present a high slew-rate differential square wave to the ADC sampling clock input. The diodes clamp at about 0.4V forward voltage, so the amplitude of the input square wave is about 0.8V p-p differential. This represents an optimum drive level for the CLK inputs.

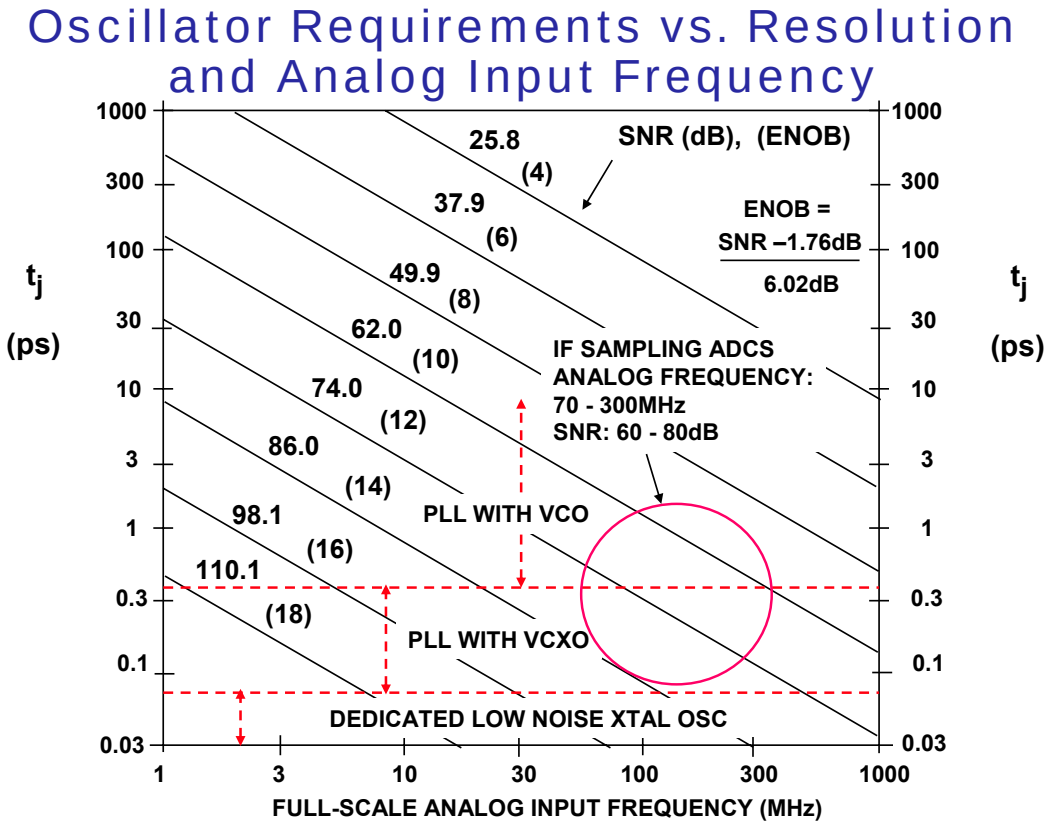
## Using a Phase-Locked Loop (PLL) and Bandpass Filter to Condition a Noisy Clock Source




Only the highest end systems can afford the dedicated crystal oscillators of the type previously discussed.

Many systems therefore use a low-cost combination of a phase-locked loop (PLL) and a VCXO (voltage-controlled crystal oscillator) followed by a bandpass filter to generate a low jitter sampling clock from a noisy system clock.

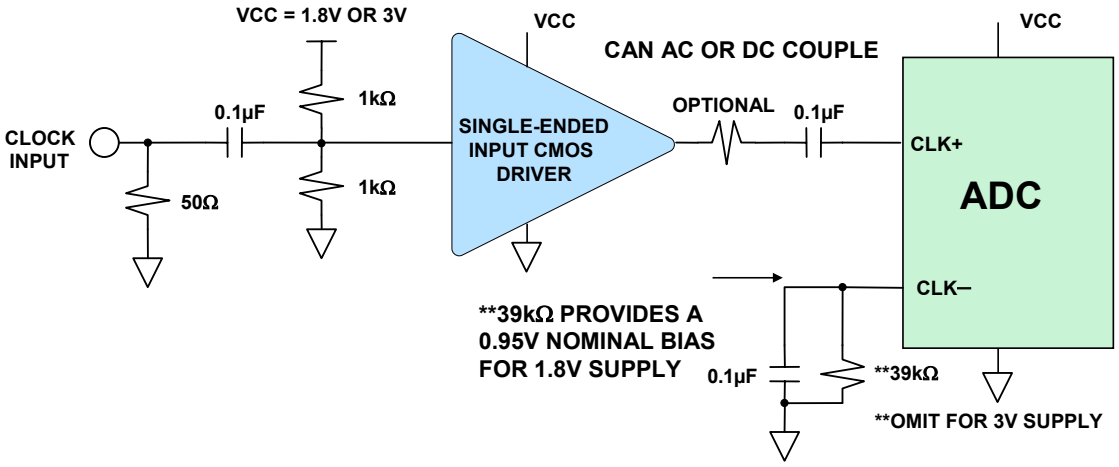
Analog Devices makes a number of PLLs and clock generation and distribution ICs suitable for this function, and these will be discussed in Section 3.




This figure shows that standard PLLs with VCOs can be used in many applications for generating clean sampling clocks.

PLLs with VCXOs can provide lower jitter solutions which are suitable for all but the most demanding applications where dedicated low-noise XTAL oscillators are required.

# Square or Sine Source Input using a 1.8V or 3V CMOS Single-Ended Clock Driver




**POSSIBLE 1.8V DRIVERS:**
**74VCX86 – LOW VOLTAGE VCX LOGIC**
**NC7NP04 – ULP TINY LOGIC SERIES**
**(FAIRCHILD)**

**POSSIBLE 3V DRIVERS:**
**74VCX86 – LOW VOLTAGE VCX LOGIC**
**NC75VC04 – TINY LOGIC SERIES**
**(FAIRCHILD)**

In order to achieve high performance, most pipelined ADCs are designed for differential sampling clock inputs. This provides good common-mode rejection and optimizes the signal for driving the internal sample-and-hold and minimizes the additive jitter at the sampling clock input.

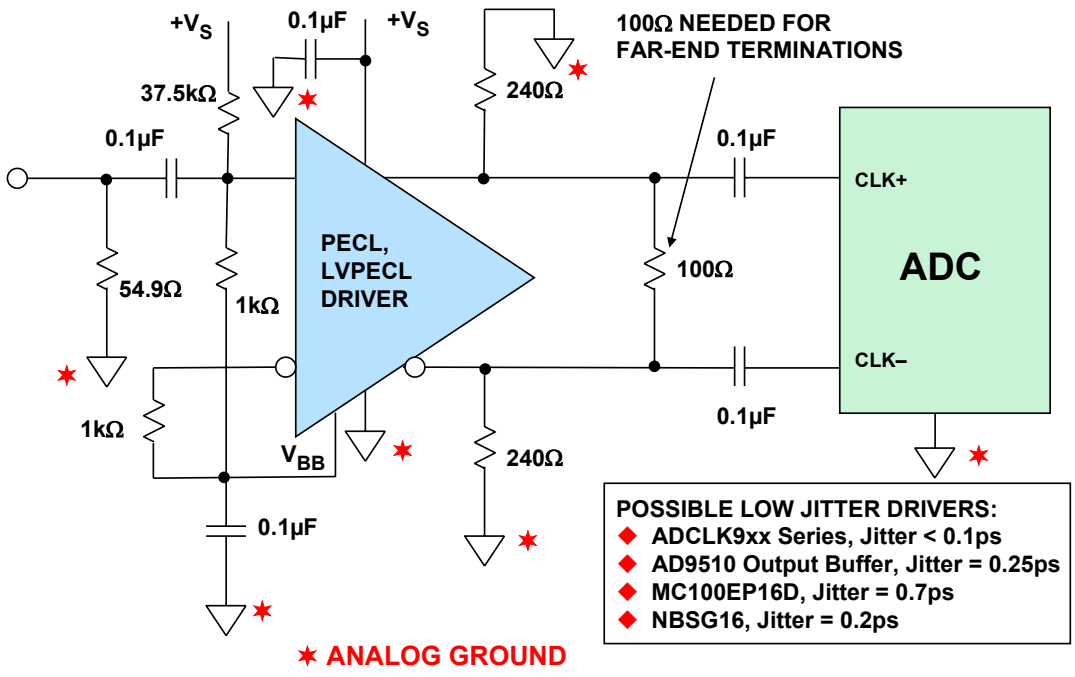
In some applications where optimum jitter performance is not required, differential clock inputs can be driven single-ended.

In this figure, a low jitter CMOS gate is used to drive the CLK+ input of the ADC, while the CLK– input is biased to the appropriate value of 0.95V for a 1.8V supply. Note that this bias level is highly product specific, so the data sheet must always be consulted to determine the optimum bias circuit and level.

A simple resistor divider is used at the input of the gate driver to set the proper dc bias level.

Several possible low jitter 1.8V and 3V CMOS drivers are listed in the figure. In all cases, the jitter specification on the CMOS driver should be compatible with the overall system requirements.

## Low Jitter Single-Ended to Differential PECL Driver




Most high-performance ADCs have differential clock inputs for lowest jitter.

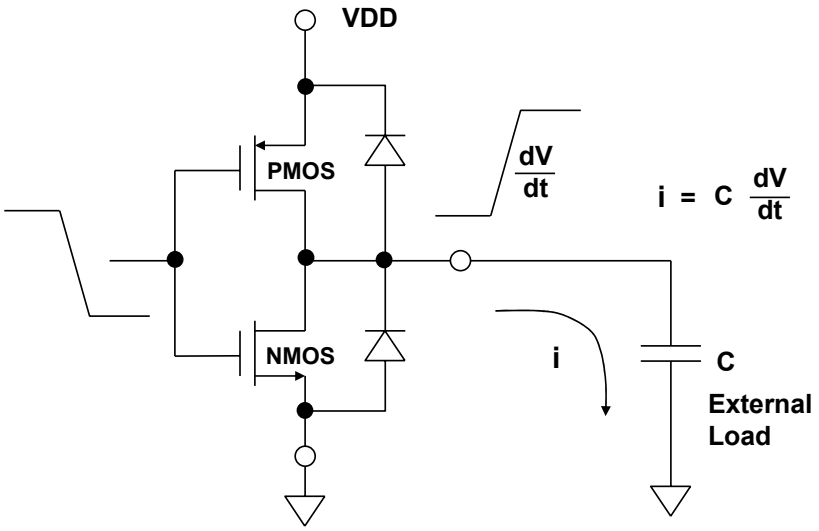
Low jitter PECL or reduced signal PECL drivers can be used to convert a single-ended signal to a differential one. These are made by ON-SEMI, and have specified jitter as low as 0.2ps.

The Analog Devices' new ADCKL9xx-series of low jitter clock drivers have additive jitter less than 0.1ps.

Note that the clock driver circuit as well as the ADC should be referenced to the same ground plane. More discussion on grounding and decoupling can be found in Section 4.

# ADC Data Outputs

# Typical CMOS Digital Output Drivers

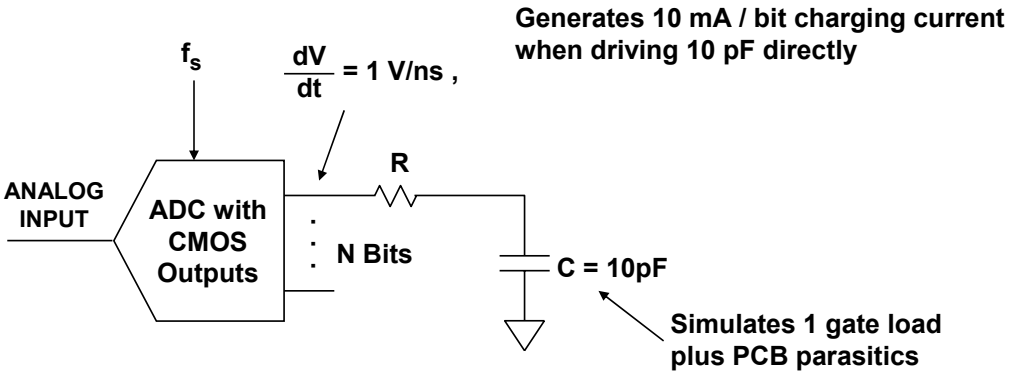



The final interface to be considered is the data output. Although these are digital outputs, they should be treated with care, because transient currents can increase the noise and distortion of the ADC by coupling back into the analog input.

Typical CMOS drivers shown in this figure are capable of generating large transient currents, especially when driving capacitive loads.

Particular care must be taken with CMOS data output ADCs so that these currents are minimized and do not generate additional noise and distortion in the ADC.

# Use Series Resistance to Minimize Charging Current of CMOS Digital Outputs



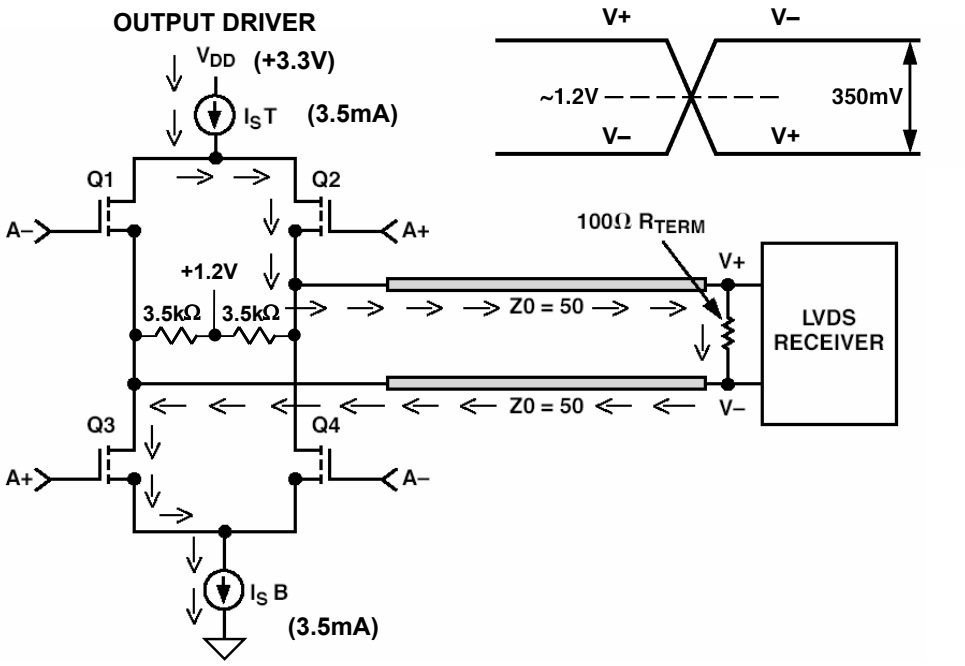

- Make RC < 0.1 $\left[\frac{1}{f_s}\right]$
- For $f_s$ = 100 MSPS, RC < 1 ns
- If C = 10 pF, R = 100 Ω

Consider the case of a 16-bit parallel CMOS output ADC. With a 10pF load on each output (simulates one gate load plus PCB parasitics), each driver generates a charging current of 10mA when driving a 10pF load. The total transient current for the 16-bit ADC can therefore be as high as 16×10mA = 160mA.

These transients currents can be suppressed by adding a small resistor, R, in series with each data output. The value should be chosen so that the RC time constant is less than 10% of the total sampling period. For $f_S$ = 100MSPS, RC should be less than 1ns. With C = 10pF, an R of about 100Ω is optimum. Choosing larger values of R can degrade output data settling time and interfere with proper data capture.

Capacitive loading on CMOS ADC outputs should be limited to a single gate load (usually an external data capture register). Under no circumstances should the data output be connected directly to a noisy data bus. An intermediate buffer register must be used to minimize direct loading of the ADC outputs.

# LVDS Driver Designed in CMOS



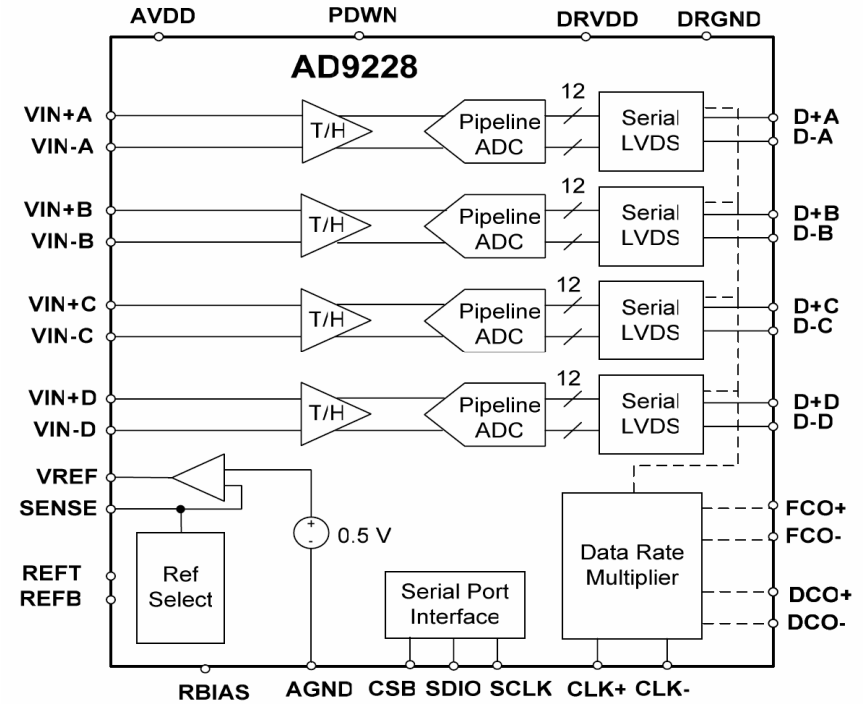

Emitter-coupled-logic (ECL) has long been known for low noise and its ability to drive terminated transmission lines with rise/fall times less than 2ns. The family presents a constant load to the power supply, is non-saturating, and the low-level differential outputs provide a high degree of common-mode rejection. However, ECL dissipates lots of power.

Recently, low-voltage-differential-signaling (LVDS) logic has attained widespread popularity because of similar characteristics, but with lower amplitudes and lower power dissipation than ECL. The LVDS logic swing is typically 350mV peak-to-peak centered about a common-mode voltage of +1.2V. A typical driver and receiver configuration is shown in this figure. The driver consists of a nominal 3.5mA current source with polarity switching provided by PMOS and NMOS transistors. The output voltage of the driver is nominally 350mV peak-to-peak at each output, and can vary between 247mV and 454 mV. The output current can vary between 2.47mA and 4.54mA. The LVDS receiver is terminated in a 100Ω line-to-line. According to the LVDS specification, the receiver must respond to signals as small as 100mV, over a common-mode voltage range of 50mV to +2.35V. The wide common-mode receiver voltage range is to accommodate ground voltage differences up to ±1V between the driver and receiver.

LVDS outputs for high-performance ADCs should be treated differently than standard LVDS outputs used in digital logic. While standard LVDS can drive 1 to 10 meters in high-speed digital applications (dependent on data rate), it is not recommended to let a high-performance ADC drive that distance. It is recommended to keep the output trace lengths short (< 2 in.), minimizing the opportunity for any noise coupling onto the outputs from the adjacent circuitry, which may get back to the analog inputs. The differential output traces should be routed close together, maximizing common-mode rejection, with the 100Ω termination resistor close to the receiver. Users should pay attention to PCB trace lengths to minimize any delay skew.

LVDS also offers some benefits in reduced EMI, because the EMI fields generated by the opposing LVDS currents tend to cancel each other.

# AD9228 Quad 12-Bit, 40/60MSPS, 1.8V LVDS Output ADC

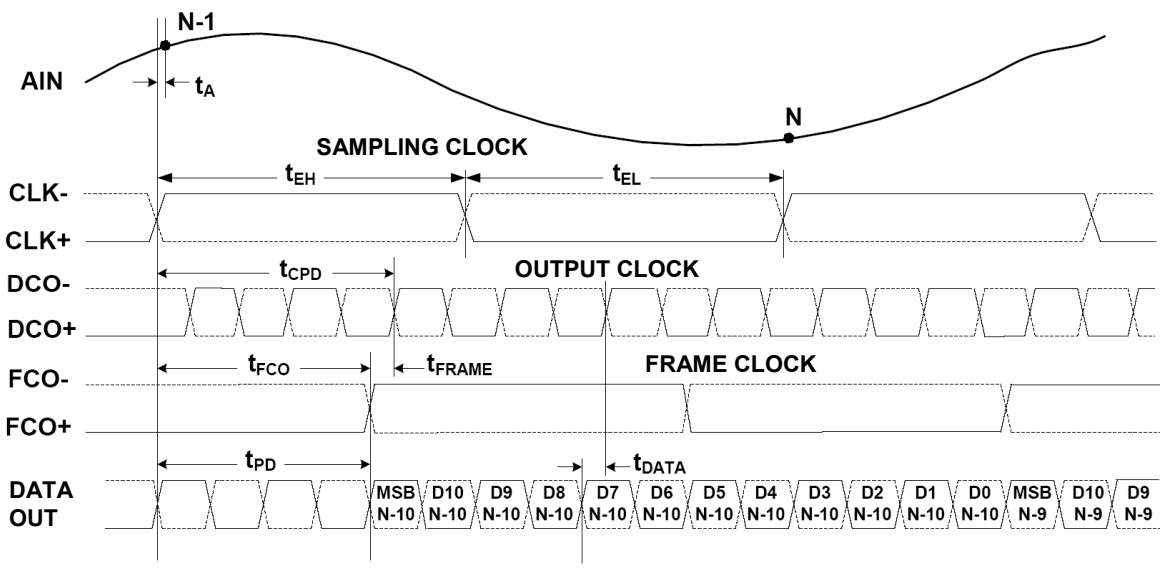



LVDS interface data rates can be as high as 800Mbits/s, thereby making serial data transfer practical even for some high speed ADCs. For instance, the AD9228 quad 12-bit, 65-MSPS ADC uses four serial LVDS outputs, each operating at 780Mbits/s. A functional block diagram of the quad ADC is shown in this figure.

The AD9228 has an on-chip track-and-hold circuit and is designed for low cost, low power, small size, and ease of use. The converter operates up to 65MSPS conversion rate and is optimized for outstanding dynamic performance where a small package size is critical. The ADC requires a single +1.8V power supply and CMOS/TTL sample rate clock for full performance operation. Total power dissipation is 477mW.

No external reference or driver components are required for many applications. A separate output power supply pin supports LVDS-compatible serial digital output levels. The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. An MSB trigger is provided to signal a new output byte. In addition, a power down mode is supported.

# AD9228 LVDS Output Data Timing Diagram




This figure shows the data output timing diagram for the AD9228. Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 12-bits times the sample clock rate, with a maximum of 780MHz (12-bits × 65MSPS = 780MHz).

Data is clocked out of the AD9228 on the rising and falling edges of DCO. The MSB clock (FCO) is used to signal the MSB of a new output byte and is equal to the sampling clock rate.

The use of high-speed serial LVDS data outputs in the AD9228 results in a huge savings in the pin count, compared with parallel outputs. A total of 48 data pins would be required to provide four individual parallel 12-bit single-ended CMOS outputs. Using serial LVDS, the AD9228 requires only four differential LVDS data outputs, or eight pins, thereby saving a total 40 pins. In addition, the use of LVDS rather than CMOS reduces digital output transient currents and the overall ADC noise.

In most applications, the ADCs drive an FPGA, where the serial-to-parallel conversion can be easily performed.

# Output Driving Summary

- **CMOS Outputs**
  - More common output logic standard interface
  - Limited speed capabilities due to board parasitics, etc. ( ≈ 150MSPS)
  - More noise due to larger signal swing causing transient currents and digital ground bounce
  - Series resistor in each data output recommended to reduce transient current
- **LVDS Outputs**
  - Becoming more popular
  - Much faster than single-ended CMOS
  - Less transient noise because LVDS uses current-mode switching and small signal swing
  - Good common-mode rejection
  - Differential resistor termination required
  - Twice the number of traces to route if using parallel outputs
  - Simpler data capture compared to single-ended CMOS demuxed solution

CMOS output ADCs retain their popularity for applications where the optimum noise performance is not mandatory. The noise produced by the high output transient currents can be reduced by placing an appropriate resistor in series with each data output. CMOS data outputs greater than about 150MSPS require demuxed outputs.

LVDS is becoming more popular because it is much faster than single-ended CMOS and generates less noise. Although LVDS requires two pins per bit output, the pin count is no greater than single-ended demuxed CMOS which also requires two pins per bit output.