Evaluation Board for 20 A Step-Down DC-to-DC Controller

EVAL-ADP1821

EVALUATION BOARD DESCRIPTION

This data sheet describes the design, operation, and test of the ADP1821 standard evaluation board. In all tests, the board is operated from an input voltage range of 9 V to 15 V, and generates up to 10 A at VOUT = 1.8 V. The switching frequency is fixed at 600 kHz.

ADP1821 DEVICE DESCRIPTION

The ADP1821 is a versatile and inexpensive synchronous buck pulse-width modulation (PWM) controller. The converter power input voltage range is 1 V to 24 V and the ADP1821 controller is specified from 3.0 V to 5.5 V. The ADP1821 free-running frequency is logic-selectable at either 300 kHz or 600 kHz. Alternatively, it can be synchronized to an external clock at any frequency between 300 kHz and 1.2 MHz. The internal gate drivers control an all N-channel power stage to regulate a converter output voltage as low as 0.6 V with up to 20 A load current.

The ADP1821 includes an adjustable soft start to limit input inrush current and facilitate sequencing. It provides current-limit and short-circuit protection, and a power-good logic output.

The ADP1821 is well suited for a wide range of power applications, such as DSP and processor core power in telecom, medical imaging, high performance servers, and industrial applications.

EVALUATION BOARD

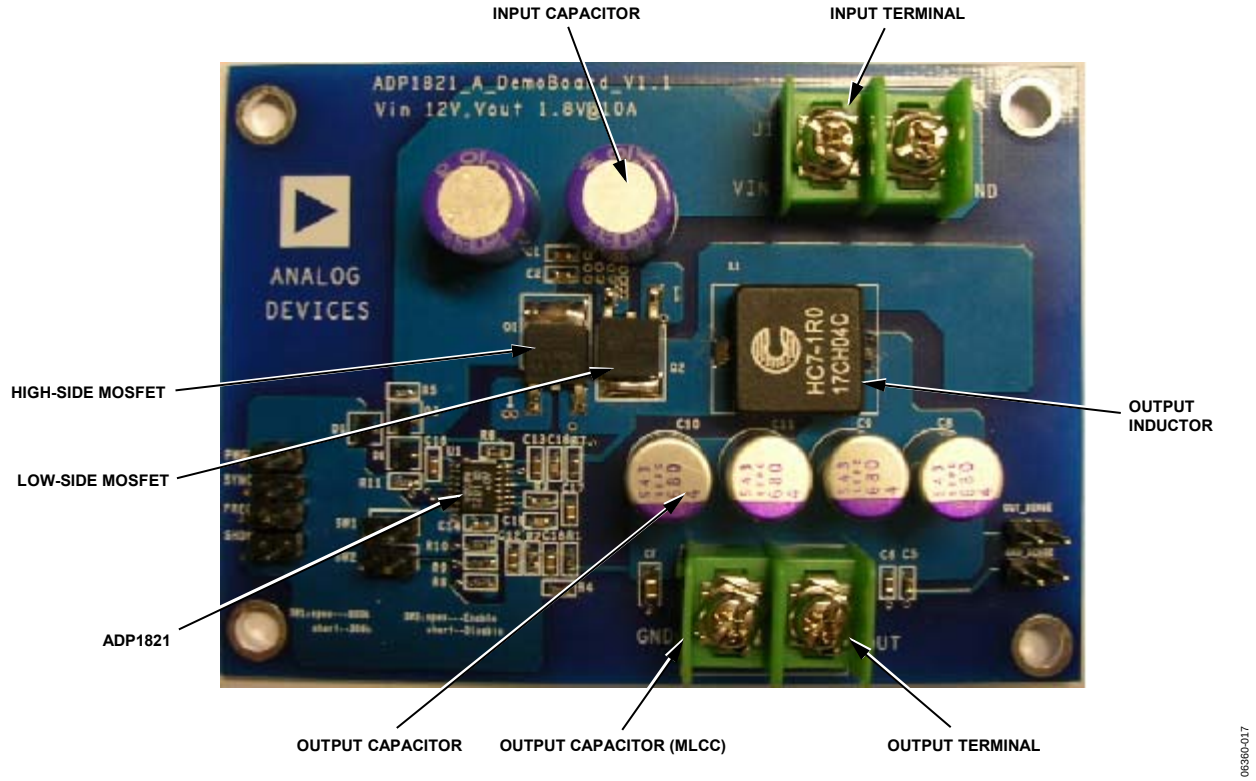

Figure 1.

Rev. 0

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REVISION HISTORY

11/06—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

COMPONENT SELECTION

Output Inductor

The output inductor can be chosen according to the following equation:

$$L = \frac{V_{OUT}}{I_O \times K_{CR} \times f_{SW}} \times (1 - D)$$

where:

V_{OUT} is the output voltage, 1.8 V.
I_o is the rated output current, 10 A.
K_{CR} is the ratio of current ripple, $K_{CR} = \Delta I/I_O$.
f_{SW} is the switching frequency.
D is the duty cycle, $D = \frac{V_{OUT}}{V_{IN}} = 0.15$

Generally, K_{CR} can be set at 20% to 40%. Thus, the inductance of L can be set at 0.63 µH to 1.2 µH.

Choosing the Output Capacitor

The capacitance and ESR of the output capacitor have a major impact on the performance of the converter, including output ripple and transient response.

Voltage ripple caused by the capacitance can be calculated by the following formula:

$$\Delta V_{CAP} = \int_0^t \frac{1}{C} \Delta I_{C_{OUT}}(\tau) d\tau$$

Voltage ripple caused by the ESR can be calculated by the following formula:

$$\Delta V_{ESR\_MAX} = \Delta I_L \times R_{ESR\_C}$$

Generally, the voltage ripple caused by the capacitance or ESR depends on the capacitor chosen.

In the evaluation board, the parameters of the output filter OS-CON capacitors are as follows:

C = 2720 µF, R_{ESR_C} = 1.75 mΩ at 600 kHz

Setting the Output Voltage

The regulation threshold at the FB pin is 0.6 V, and the maximum input bias current is 100 nA. This bias current can introduce significant errors if the divider impedance is too high. In order to get the best accuracy, the bottom resistor R2 should be no higher than 50 kΩ. However, very low values of R2 will dissipate excess power. It is recommend that R2 be a 1% resistor with a value between 1 kΩ and 10 kΩ.

The upper divider is then set with the following formula:

$$R1 = R2 \times \frac{V_{OUT} - 0.6}{0.6}$$

Current Limit Set Resistor

The voltage on the CSL pin can be calculated with the following formula:

$$V_{CSL} = I_{CSL} \times (R_{CSL} + R_{RDSON\_LOW}) - \left(I_L + \frac{\Delta I_L}{2}\right) \times R_{RDSON\_LOW}$$

where:

V_{CSL} is the voltage on the CSL pin.
I_{CSL} is the source current out of the CSL pin, 42 µA.
R_{CSL} is the current limited resistor.
R_{DSON_LOW} is the conduction resistor of the low-side MOSFET.
I_L is the output current.
ΔI_L is the output current ripple.

In normal operation, the direction of current flow through the low-side MOSFET causes a negative voltage to appear on its drain,

$$V = I \times R$$

where I is the instantaneous MOSFET current and R is R_{DSON}.

A 42 µA current source at the ADP1821 CSL pin causes a fixed voltage drop in the current sense resistor that is connected from the CSL pin to the drain of the low-side MOSFET. This current through the current limit set resistor produces a voltage in the opposite direction, thus raising in the positive direction the potential at the CSL pin. The resulting net voltage on the CSL pin is compared with ground. During normal operation, the CSL pin stays above ground potential. The overcurrent protection circuitry is triggered when an increased MOSFET current produces increased negative voltage on the low-side MOSFET drain, thus causing the voltage on the CSL pin to go negative with respect to ground.

The resistor R_{CSL} can be calculated from the following equation:

$$R_{CSL} = \frac{\left(I_{LIMIT} + \frac{\Delta I_L}{2}\right) \times R_{DSON\_LOW}}{I_{CSL}}$$

where I_{LIMIT} is the desired load current limit.

Setting the Soft Start

The soft start characteristic is set by the capacitor connected from SS to GND. The ADP1821 charges C_{SS} to 0.8 V through an internal resistor. The soft start period t_{SS} is achieved with V (C_{SS}) = 0.6 V.

$$C_{SS} = \frac{t_{SS}}{-\ln\left(1 - \frac{0.6}{0.8}\right) \times 100\ \text{k}\Omega}$$

where 100 kΩ is the internal resistor.

DESIGN AND CONTROL LOOP EQUATIONS

See Figure 2 for a simplified schematic diagram of the overall control loop.

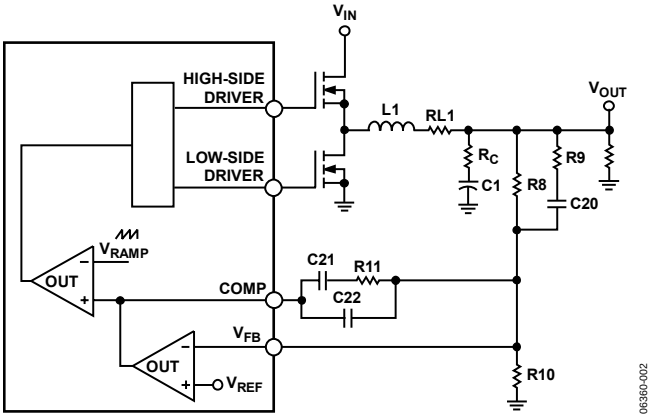

Figure 2. Control Loop

Power Stage Transfer Function

The power stage transfer function of ADP1821 is given by the following equations. Figure 3 shows the Bode plots of the phase and gain margin.

$$G_{VD}(s) = \frac{V_{OUT}(s)}{D(s)}$$

$$G_{VD}(s) = \left(\frac{V_{IN}}{1+\frac{R_L}{R}}\right) \times \left(\frac{1+\left(R_C \times C \times s\right)}{1+\frac{s}{Q \times \omega_0}+\frac{s^2}{\omega_0{}^2}}\right)$$

where:

$$\omega_0 = \frac{\sqrt{\frac{R_L+R}{R_C+R}}}{\sqrt{L \times C}}$$

$$Q = \frac{\frac{R_L}{R}+1}{\frac{L}{R}+\left(R_L+R_C\right) \times C+\frac{R_C \times R_L \times C}{R}} \times \frac{1}{\omega_0}$$

R_C is the ESR of output capacitor.
R_L is the series resistor of output inductor.
ω_0 is the resonant frequency.

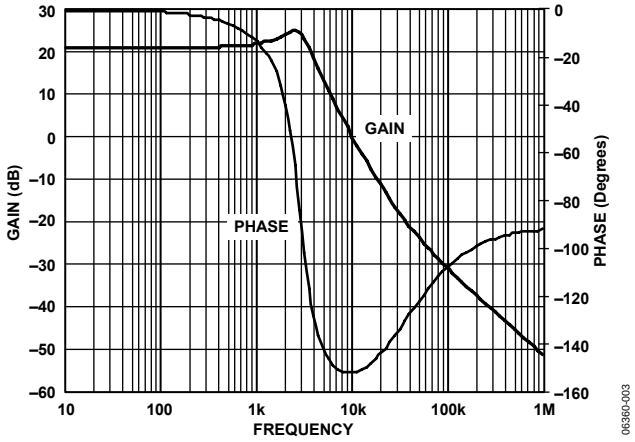

Figure 3. Power Stage Gain and Phase Margin

Control Circuit and Transfer Function

The compensation circuit is used for the control circuit and transfer function as shown in Figure 4.

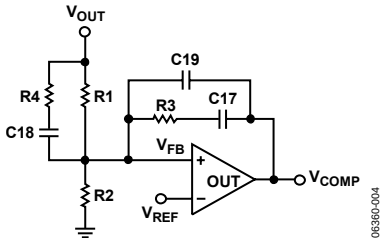

Figure 4. Compensation Circuit

The equation for the compensation transfer function is:

$$G_{EA}(s) = \frac{V_{COMP}(s)}{V_{OUT}(s)}$$

$$G_{EA}(s) = k \times \frac{\left(1+\frac{s}{2\pi f_{Z1}}\right)\left(1+\frac{s}{2\pi f_{Z2}}\right)}{\left(1+\frac{x}{2\pi f_{P1}}\right)\left(1+\frac{x}{2\pi f_{P2}}\right)}$$

where:

V_{COMP} is the voltage at the COMP pin.
f_{Z1} is the first compensator zero frequency produced by R3 and C17.
f_{Z2} is the second compensator zero frequency produced by R1, R2, and C18.
f_{P1} is the first compensator pole frequency produced by C17 and C19.
f_{P2} is the second compensator pole frequency produced by C18.

$$k = -\frac{R3}{R1}$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R3 \times C17}$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1+R2) \times C18}$$

$$f_{P1} = \frac{1}{2 \times \pi \times R3\left(\frac{C17 \times C19}{C17 + C19}\right)}$$

$$f_{P2} = \frac{1}{2 \times \pi \times R4 \times C18}$$

The switching frequency is 600 kHz. For best performance, setting the crossover frequencies to ~1/10 of switching frequency, f_{SW}, or ~60 kHz is recommend. Lower crossover frequencies cause poor dynamic response, and higher crossover frequencies can cause instability. The best performance usually results from the highest possible crossover frequency that allows adequate gain and phase margins. A phase margin in the range of 40 to 60 degrees is recommended (see Figure 5).

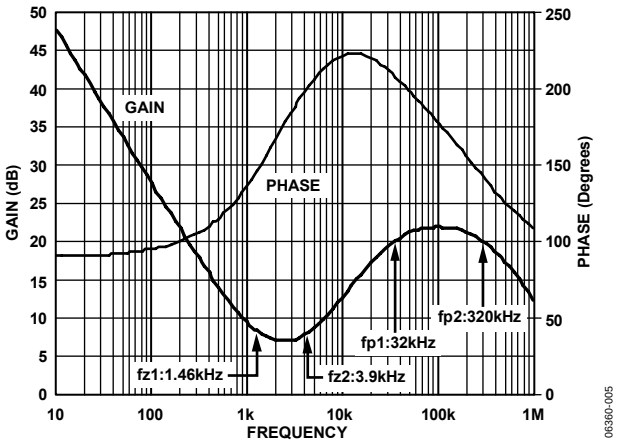

Figure 5. Compensation Gain and Phase

Overall Loop Results

The overall control loop gain can be shown as:

$$T(s) = \frac{G_{VD}(s) \times G_{EA}(s)}{V_{RAMP}}$$

where:

G_{VD} is the power stage transfer function.
G_{EA} is the compensation transfer function.
V_{RAMP} is the peak ramp voltage (typically 1.25 V) of the ADP1821 PWM controller.

The overall control loop Bode plot is shown in Figure 6.

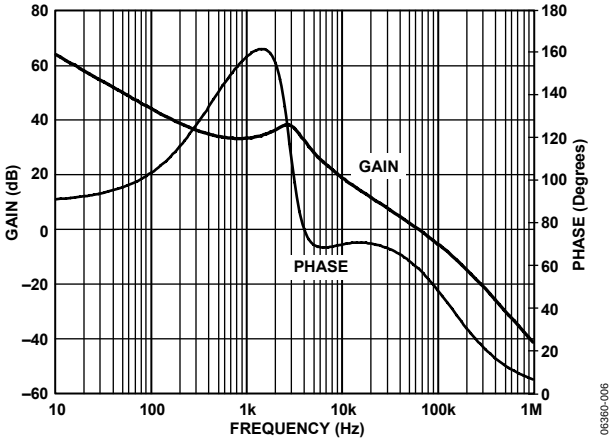

Figure 6. Overall Control Loop Gain
Cross Frequency: 63 kHz, Phase Margin: 55 Degrees

TEST RESULTS AND WAVEFORMS

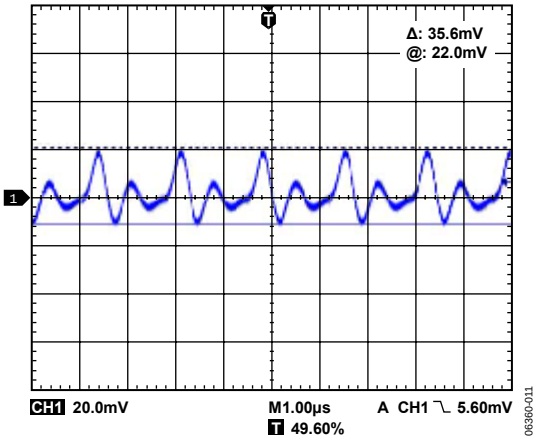

Figure 7. Output Voltage Ripple of Channel 1
V_{IN} = 12 V, V_{OUT} = 1.8 V, Load = 10 A

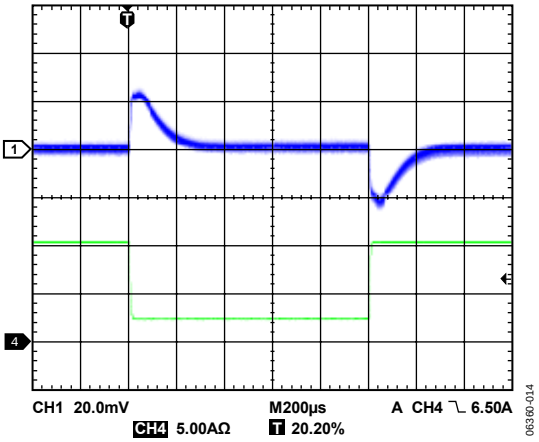

Figure 10. Transient Response, Channel 1: V_{OUT}, Channel 4: I_{OUT}
V_{IN} = 12 V, V_{OUT} = 1.8 V, Load = 2 A to 10 A

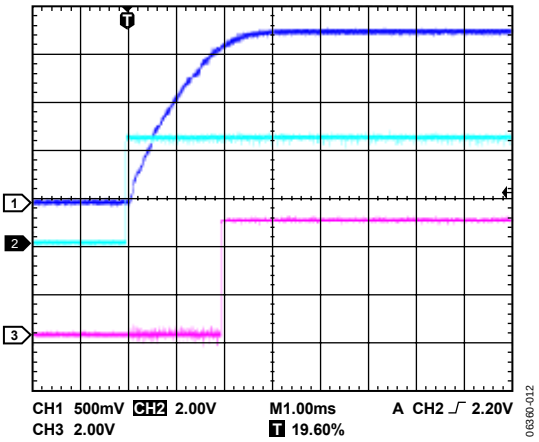

Figure 8. Enable On, Channel 1: V_{OUT}, Channel 2: EN, Channel 3: PWGD
V_{IN} = 12 V, V_{OUT} = 1.8 V, Load = 10 A

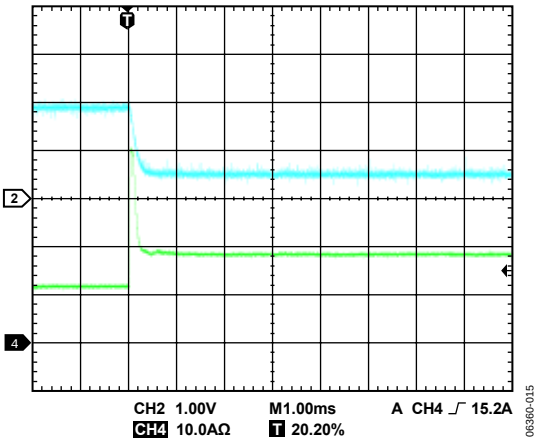

Figure 11. Load Short, Channel 2: V_{OUT}, Channel 4: I_{OUT}
V_{IN} = 12 V, V_{OUT} = 1.8 V

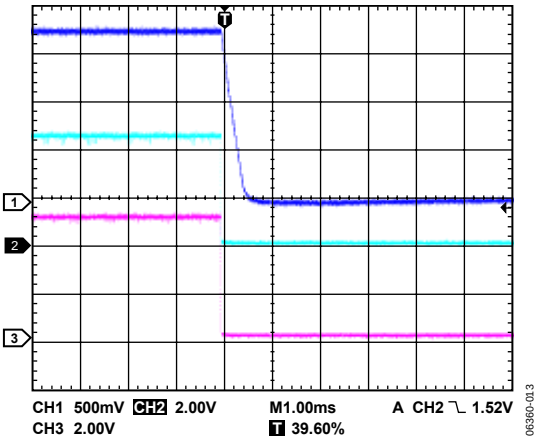

Figure 9. Enable Off, Channel 1: V_{OUT}, Channel 2: EN, Channel 3: PWGD
V_{IN} = 12 V, V_{OUT} = 1.8 V, Load = 10 A

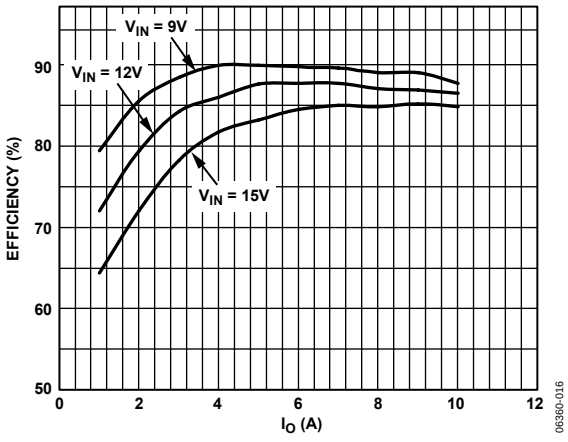

Figure 12. Efficiency vs. Load Current

PCB LAYOUT GUIDELINES

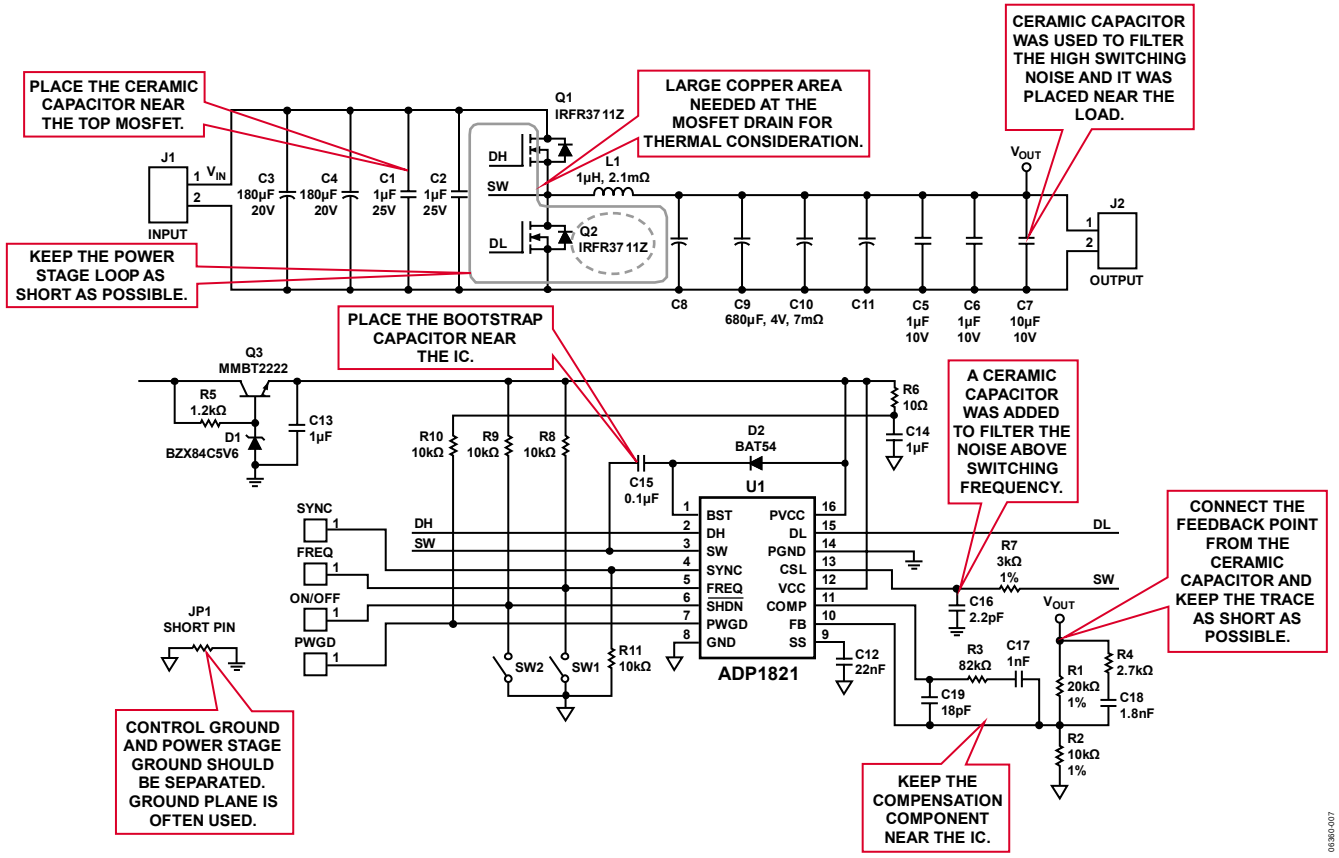

Figure 13. PCB Layout Guide

To keep the inductance down, the traces running from the high-side MOSFET and the low-side MOSFET to the DH and DL pins of the ADP1821, respectively, need to be relatively short and wide.

The source of Q1 and drain of Q2 should be placed as close as possible to minimize the inductance in this portion of the circuit. Keep this connection short and wide. However, too much copper area on this switch node increases capacitively coupled common-mode noise.

Note the following:

- Ceramic input decoupling capacitors C1 and C2 should be located as close as possible to the drain of Q1 and source of Q2.
- C13 and C14 should be close to the VIN pin of IC.
- The compensation components should also be placed closed to the IC.

The analog GND of the ADP1821 and the ground of the signal components should be connected to the AGND plane. The PGND of the ADP1821 and the ground of all the power components, such as the low-side MOSFET, and input and output bulk capacitors, should be connected to the PGND plane. The connection between the ground of the power components and the PGND plane needs to be kept as short as possible. This minimizes noise, electromagnetic interference (EMI), and ground bouncing.

EVALUATION BOARD SCHEMATIC AND ARTWORK

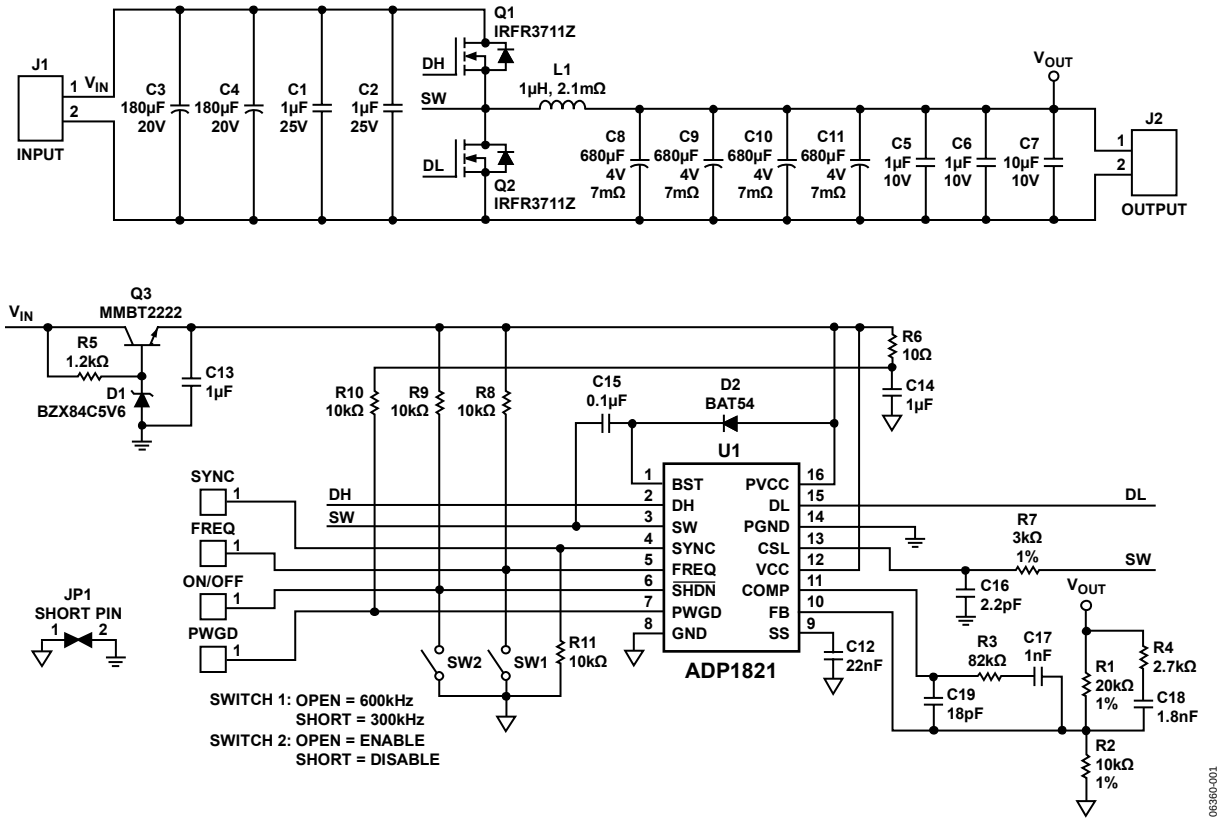

Figure 14. ADP1821 Typical Application Schematic Diagram

PCB LAYOUT

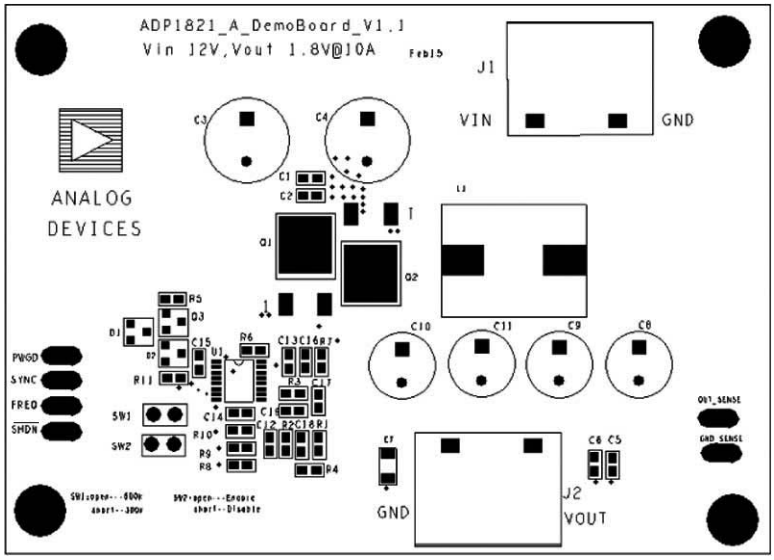

Figure 15. Silkscreen Top

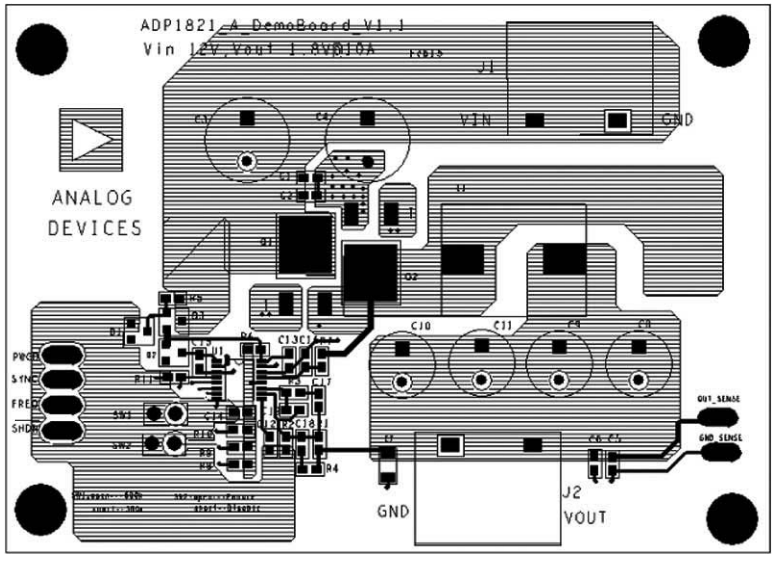

Figure 16. Top Layer

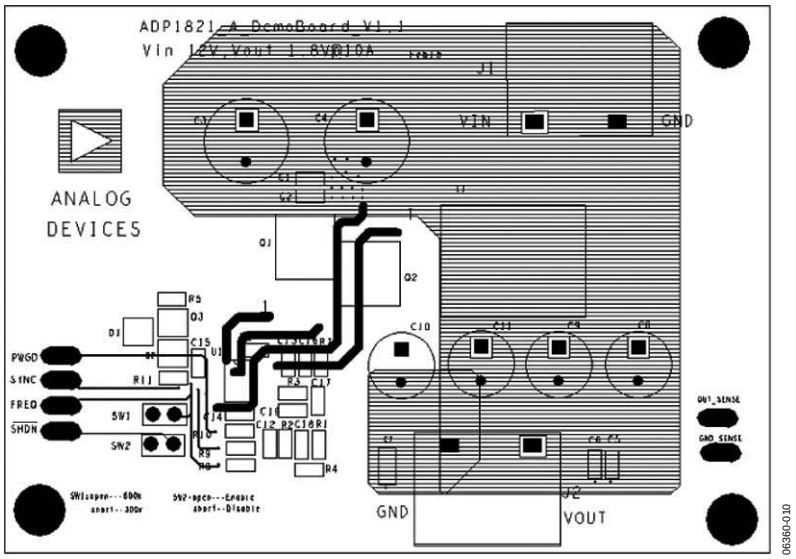

Figure 17. Bottom layer

ORDERING INFORMATION

BILL OF MATERIALS

Typical application circuit (12 V to 1.8 V@ 10 A, f_{SW} = 600 kHz)

Table 1.

Qty	Reference Designator	Description	Supplier	Supplier Number
2	C1,C2	Capacitor, ceramic, 1 µF, 25 V, X5R, 0603	Murata	GRM188RC1E105KA
2	C3, C4	Capacitor, OS-CON, 180 µF, 20 V, 20 mΩ, 11 mm x 10 mm x 5 mm	Sanyo	20SP180M
4	C5, C6, C13, C14	Capacitor, ceramic, 1 µF, 10 V, X5R, 0603	Murata	GRM188R61A105KA
1	C7	Capacitor, ceramic, 10 µF, 10 V, X5R, 1206	Murata	GRM319R61A106KE19
4	C8, C9, C10, C11	Capacitor, OS-CON, 680 µF, 4 V, 7 mΩ, 13 mm x 8 mm x 3.5 mm	Sanyo	4SEPC680M
1	C12	Capacitor, ceramic, 22 nF, 16 V, X7R, 0603	Vishay or equivalent	VJ0603Y223KXXA
1	C15	Capacitor, ceramic, 0.1 µF, 16 V, X7R, 0603	Vishay or equivalent	VJ0603Y104MXQ
1	C16	Capacitor, ceramic, 2.2 pF, 16 V, NPO, 0603	Vishay or equivalent	VJ0603Y2R2KXXA
1	C17	Capacitor, ceramic, 1 nF, 16 V, X7R, 0603	Vishay or equivalent	VJ0603Y102KXXA
1	C18	Capacitor, ceramic, 1.8 nF, 16 V, X7R, 0603	Vishay or equivalent	VJ0603Y182KXXA
1	C19	Capacitor, ceramic, 18 pF, 50 V, NPO, 0603	Vishay or equivalent	VJ0603Y180KXXA
1	D1	Diode_Zener, 5.6 V, SOT-23	ON Semiconductor®	BZX84C5V6
1	D2	Diode, 30 V, 200 mA, 4 ns, SOT-23	Fairchild	BAT54
1	L1	Inductor, 1 µH, 2.1 mΩ, 20.3 A	Coiltronics	HC7-1R0
1	Q1	N-MOSFET, 20 V, D-PAK, 5.7 mΩ, 18 nC	IR	IRFR3711Z
1	Q2	N-MOSFET, 20 V, D-PAK, 5.7 mΩ, 18 nC	IR	IRFR3711Z
1	Q3	BJT- NPN, 40 V, 600 mA, SOT-23	ON Semiconductor®	MMBT2222
1	R1	Resistor, 20 kΩ, 1/10 W, 1%, 0603	Vishay or equivalent	CRCW06032002F
1	R2	Resistor, 10 kΩ, 1/10 W, 1%, 0603	Vishay or equivalent	CRCW06031002F
1	R3	Resistor, 82 kΩ, 1/10 W, 1%, 0603	Vishay or equivalent	CRCW06038202F
1	R4	Resistor, 2.7 kΩ, 1/10 W, 1%, 0603	Vishay or equivalent	CRCW06032701F
1	R5	Resistor, 1.2 kΩ, 1/10 W, 1%, 0603	Vishay or equivalent	CRCW06031201F
1	R6	Resistor, 10 Ω, 1/10 W, 1%, 0603	Vishay or equivalent	CRCW060310R0F
1	R7	Resistor, 3 kΩ, 1/10 W, 1%, 0603	Vishay or equivalent	CRCW06033001F
4	R8, R9, R10, R11	Resistor, 10 kΩ, 1/10 W, 1%, 0603	Vishay or equivalent	CRCW06031002F
1	U1	Step-down dc-to-dc controller	Analog Devices, Inc.	ADP1821
4	VOUT, GND	Terminals		

ORDERING GUIDE

Model	Description
ADP1821-EVAL	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

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