19-4573; Rev 2; 6/10

MAXIM

超低功耗、立体声音频编解码器

概述

MAX9867是一款超低功耗立体声音频编解码器，设计用于手机和便携式游戏机等便携式消费类电子产品。

该器件具有立体声差分麦克风输入，可连接至模拟或数字麦克风。单端线入信号经过可配置前置放大器，能够输入到ADC用于录音或直接切换到耳机放大器用于回放。辅助ADC通道可用于跟踪任何直流电压。

立体声耳机放大器支持差分、单端以及无滤波电容的输出配置。采用无滤波电容输出配置时，器件可为32Ω负载提供10mW输出功率。完备的咔嗒/噼噗声抑制电路能够在音量变化、启动或关断过程中消除可闻噪声。

采用Maxim专有的数字电路，器件可接受任何10MHz至60MHz范围的系统时钟。该架构省去了外部PLL和多个晶体振荡器。立体声ADC和DAC通道提供用户可配置的语音频段或音频频段的数字滤波器。语音频段滤波器在GSM分组频段提供额外的衰减，在$f_S/2$频点具有大于70dB的阻带衰减。

MAX9867采用1.8V单电源供电，支持1.65V至3.6V逻辑电平。可通过2线、I²C串行接口控制音量、信号混音以及常规工作模式。

MAX9867采用小尺寸、2.2mm x 2.7mm、0.4mm焊球间距的WLP封装。另外还可提供32引脚、5mm x 5mm TQFN封装。

特性

- ♦ 1.8V单电源供电
- ♦ 6.7mW回放功耗
- ♦ 90dB立体声DAC，8kHz ≤ f_S ≤ 48kHz
- ♦ 85dB立体声ADC，8kHz ≤ f_S ≤ 48kHz
- ♦ 辅助ADC，用于电池测量
- ♦ 支持10MHz至60MHz任意主时钟频率
- ♦ 支持立体声数字麦克风输入
- ♦ 立体声模拟差分麦克风输入
- ♦ 立体声耳机放大器：差分、单端或无滤波电容三种配置
- ♦ 立体声线入
- ♦ 语音频段滤波器，阻带衰减大于70dB
- ♦ 1.65V至3.6V数字接口供电电源
- ♦ I²S/TDM兼容的数字音频总线
- ♦ 30焊球、2.2mm x 2.7mm、0.4mm焊球间距的WLP封装

应用

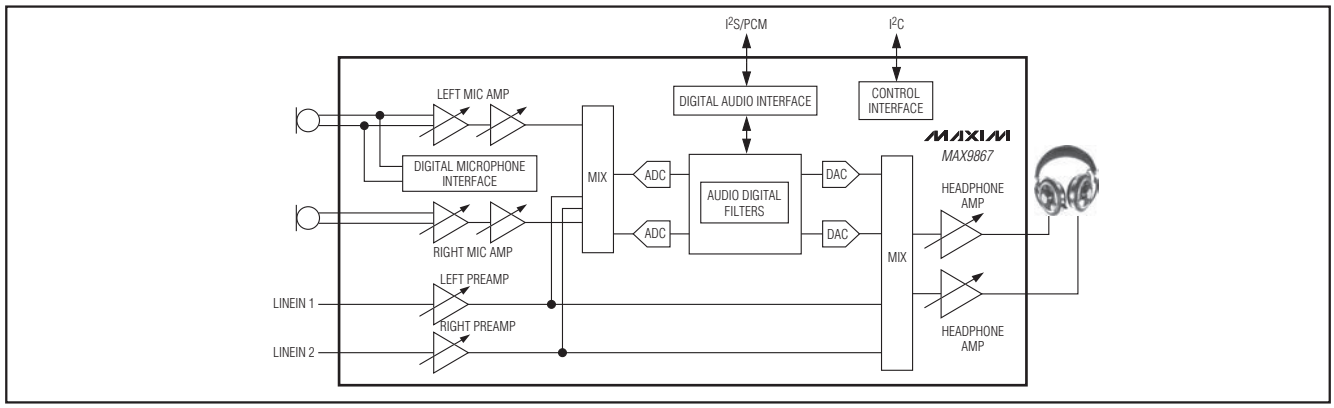
蜂窝电话
便携式游戏机
便携式导航设备
便携式多媒体播放器
无线耳机

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX9867EWV+	-40°C to +85°C	30 WLP
MAX9867ETJ+	-40°C to +85°C	32 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*

简化框图



ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to AGND.)
DVDD, AVDD, and PVDD .....-0.3V to +2V
DVDDIO .....-0.3V to +3.6V
DGND and PGND .....-0.1V to +0.1V
PREG, REF, REG, MICBIAS .....-0.3V to (AVDD + 0.3V)
MCLK, LRCLK, BCLK
SDOUT, SDIN .....-0.3V to (DVDDIO + 0.3V)
SDA, SCL, IRQ .....-0.3V to +3.6V
LOUTP, LOUTN, ROUTP,
ROUTN .....(PGND - 0.3V) to (PVDD + 0.3V)
LINL, LINR, JACKSNS/AUX, MICLP/DIGMICDATA,
MICLN/DIGMICCLK, MICRP, MICRN..-0.3V to (AVDD + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
30-Bump WLP (derate 12.5mW/°C above +70°C) 1000mW
32-Pin TQFN-EP (derate 34.5mW/°C above +70°C) .2759mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
30-Bump WLP .....80°C/W
32-Pin TQFN-EP .....29°C/W
Operating Temp Range .....-40°C to +85°C
Storage Temp Range .....-65°C to +150°C
Lead Temperature (TQFN only, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range		PVDD, DVDD, AVDD		1.65	1.8	1.95	V
		DVDDIO		1.65	1.8	3.6	
Total Supply Current	I_{VDD}	Full-duplex 8kHz mono (voice mode) (Note 3)	Analog (AVDD + PVDD)		4.65	7	mA
			Digital (DVDD + DVDDIO)		0.96	1.5	
		DAC playback 48kHz stereo (audio mode) (Note 3)	Analog (AVDD + PVDD)		3.28	5	
			Digital (DVDD + DVDDIO)		1.40	2	
		Full-duplex 48kHz stereo (audio mode) (Note 3)	Analog (AVDD + PVDD)		8.0	12	
			Digital (DVDD + DVDDIO)		2.0	3	
		Stereo line-in only	Analog (AVDD + PVDD)		3.8	6	
			Digital (DVDD + DVDDIO)		0.004	0.05	
Shutdown Supply Current		T_A = +25°C	Analog (AVDD + PVDD)		1	5	µA
			Digital (DVDD + DVDDIO)		1	5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown to Full Operation		Excludes PLL lock time			10		ms
Soft-Start/-Stop Time					10		ms
DAC (Note 4)							
Dynamic Range (Note 5)	DR	f_S = 48kHz, AV_{VOL} = 0dB, T_A = +25°C	Master or slave mode		90		dB
			Slave mode	84			
Full-Scale Output		V_{OLL}/V_{OLR} = 0x09	Differential mode		1		V_{RMS}
			Capacitorless and single-ended modes		0.56		
Gain Error		DC accuracy, measured with respect to full-scale output			1	5	%
Voice Path Phase Delay	P_{DLY}	f = 1kHz, 0dBFS, HP filter disabled, digital input to analog output	f_S = 8kHz		1.2		ms
			f_S = 16kHz		0.59		
Total Harmonic Distortion	THD	MCLK = 12.288MHz, f_S = 48kHz, 0dBFS, measured at headphone outputs			-80		dB
DAC Attenuation Range	AV_{DAC}	DACA = 0xF to 0x0		-15		0	dB
DAC Gain Adjust	AV_{GAIN}	DACG = 00 to 11		0		+18	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V		60	78		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			75		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			62		
DAC VOICE MODE DIGITAL IIR LOWPASS FILTER							
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz			0.448 x f_S		Hz
		-3dB cutoff			0.451 x f_S		
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz			0.476 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz		75			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC VOICE MODE DIGITAL 5th ORDER IIR HIGHPASS FILTER						
5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable)	f_{DHPPB}	DVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0161 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0312 x f_S		
		DVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0321 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0625 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)		0.0042 x f_S		
5th Order Stopband Cutoff (-30dB from Peak, I²C Register Programmable)	f_{DHPSB}	DVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0139 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0156 x f_S		
		DVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0279 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0312 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)		0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	DVFLT ≠ 000		90		dB
DAC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.43 x f_S		Hz
		-3dB cutoff		0.47 x f_S		
		-6.02dB cutoff		0.50 x f_S		
Passband Ripple		$f < f_{PLP}$		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.58 x f_S		Hz
Stopband Attenuation			60			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC STEREO AUDIO MODE DIGITAL DC BLOCKING HIGHPASS FILTER						
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT = 0x1		0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	DVFLT = 0x1		90		dB
ADC (Note 6)						
Dynamic Range (Note 5)	DR	f_S = 8kHz, MODE = 0 (IIR voice)	75	84		dB
		f_S = 8kHz to 48kHz, MODE = 1 (FIR audio)		85		
Full-Scale Input		Differential MIC input or stereo-line inputs, AV_{PRE} = 0dB, AV_{PGAM} = 0dB		1		V_{P-P}
Gain Error (Note 7)		DC accuracy, measured with respect to 80% of full-scale output		1	5	%
Voice Path Phase Delay	P_{DLY}	f = 1kHz, 0dBFS, HP filter disabled, analog input to digital output; f_S = 8kHz		1.2		ms
		f = 1kHz, 0dBFS, HP filter disabled, analog input to digital output; f_S = 16kHz		0.61		
Total Harmonic Distortion	THD	f = 1kHz, f_S = 8kHz, T_A = +25°C, 0dBFS		-81	-70	dB
ADC Level Adjust Range	AV_{ADC}	AVL/AVR = 0xF to 0x0	-12		+3	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred	60	85		dB
		f = 217Hz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		85		
		f = 1kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
		f = 10kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
ADC VOICE MODE DIGITAL IIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.445 x f_S		Hz
		-3dB cutoff		0.449 x f_S		
Passband Ripple		f < f_{PLP}		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.469 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz	74			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC VOICE MODE DIGITAL 5th ORDER IIR HIGHPASS FILTER						
5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable)	f_{AHPPB}	AVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0161 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0312 x f_S		
		AVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0321 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0625 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0042 x f_S		
Stopband Cutoff (-30dB from Peak)	f_{AHPSB}	AVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0139 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0156 x f_S		
		AVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0279 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0312 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	AVFLT ≠ 000		90		dB
ADC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.43 x f_S		Hz
		-3dB cutoff		0.48 x f_S		
		-6.02dB cutoff		0.5 x f_S		
Passband Ripple		$f < f_{PLP}$		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.58 x f_S		Hz
Stopband Attenuation		$f > f_{SLP}$, f = 20Hz to 20kHz	60			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC STEREO AUDIO MODE DIGITAL DC BLOCKING HIGHPASS FILTER							
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1			0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	AVFLT = 0x1			90		dB
OUTPUT VOLUME CONTROL							
Line Input to Output Volume Control	AV_{VOL}	VOLL/VOLR = 0x00		14.55	14.9	15.15	dB
		VOLL/VOLR = 0x01		14.1	14.4	14.6	
		VOLL/VOLR = 0x02		13.6	13.9	14.1	
		VOLL/VOLR = 0x04		12.6	12.9	13.1	
		VOLL/VOLR = 0x08		9.35	9.9	10.35	
		VOLL/VOLR = 0x10		0.35	0.9	1.35	
		VOLL/VOLR = 0x20		-50.15	-49.2	-48.15	
Output Volume Control Step Size		VOLL/VOLR = 0x00 to 0x06 (+6dB to +3dB)			0.5		dB
		VOLL/VOLR = 0x06 to 0x0F (+3dB to -6dB)			1		
		VOLL/VOLR = 0x0F to 0x17 (-6dB to -22dB)			2		
		VOLL/VOLR = 0x17 to 0x3F (-22dB to mute)			4		
Output Volume Control Mute Attenuation		f = 1kHz			100		dB
HEADPHONE AMPLIFIER (Note 8)							
Output Power per Channel (Differential Mode)	P_{OUT}	f = 1kHz, THD < 1%, T_A = +25°C	R_L = 16Ω	30	52		mW
			R_L = 32Ω		32		
Output Power per Channel (Capacitorless Mode)	P_{OUT}	f = 1kHz, THD < 1%, T_A = +25°C	R_L = 16Ω		19		mW
			R_L = 32Ω	8	10		
Total Harmonic Distortion + Noise (Differential Mode)	THD+N	R_L = 16Ω, P_{OUT} = 25mW, f = 1kHz			-76		dB
		R_L = 32Ω, P_{OUT} = 25mW, f = 1kHz	MCLK = 13MHz, f_S = 8kHz		-77	-70	
			MCLK = 12.288MHz, f_S = 48kHz		-80		
Total Harmonic Distortion + Noise (Capacitorless Mode)	THD+N	R_L = 16Ω, P_{OUT} = 6.25mW, f = 1kHz			-72		dB
		R_L = 32Ω, P_{OUT} = 6.25mW, f = 1kHz	MCLK = 13MHz, f_S = 8kHz		-74	-65	
			MCLK = 12.288MHz, f_S = 48kHz		-74		
Total Harmonic Distortion + Noise (SE Mode)	THD+N	R_L = 16Ω, P_{OUT} = 6.25mW, f = 1kHz			-74		dB
		R_L = 32Ω, P_{OUT} = 6.25mW, f = 1kHz	MCLK = 13MHz, f_S = 8kHz		-74	-65	
			MCLK = 12.288MHz, f_S = 48kHz		-76		
Dynamic Range	DR	AV_{VOL} = +6dB (Notes 5, 7)		76	90		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 7)	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V		60	78		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			75		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			62		
Output Offset Voltage	V_{OS}	AV_{VOL} = -84dB differential mode	(LOUTP–LOUTN, ROUTP–ROUTN), T_A = +25°C		±0.2		mV
		AV_{VOL} = -84dB capacitorless mode	(LOUTP–LOUTN, ROUTP–LOUTN), T_A = +25°C		±0.8		
Crosstalk	X_{TALK}	Differential mode, P_{OUT} = 5mW, f = 1kHz			87		dB
		Capacitorless mode, P_{OUT} = 5mW, f = 1kHz	TQFN		55		
			WLP		60		
Capacitive Drive		No sustained oscillations	R_L = 32Ω		500		pF
			R_L = ∞		100		
Click-and-Pop Level (Differential, Capacitorless Modes)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-80		dBV
			Out of shutdown		-69		
Click-and-Pop Level (SE Mode)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-75		dBV
			Out of shutdown		-75		
MICROPHONE AMPLIFIER							
Preamplifier Gain	AV_{PRE}	PALEN/PAREN = 01		-0.5	0	+0.5	dB
		PALEN/PAREN = 10		19.5	20	20.5	
		PALEN/PAREN = 11		29.5	30	30.5	
MIC PGA Gain	AV_{PGAM}	PGAML/PGAMR = 0x1F		-0.6	-0.1	+0.4	dB
		PGAML/PGAMR = 0x00		19.3	19.75	20.3	
Common-Mode Rejection Ratio	CMRR	V_{IN} = 100mV_{P-P}, f = 217Hz			50		dB
MIC Input Resistance	R_{IN_MIC}	All gain settings		30	50		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion + Noise	THD+N	AV_{PRE} = 0dB, V_{IN} = $1V_{P-P}$, f = 1kHz		-80		dB
		AV_{PRE} = +30dB, V_{IN} = $32mV_{P-P}$, f = 1kHz, ($1V_{P-P}$ at ADC input)		-67		
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred	60	85		dB
		f = 217Hz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		85		
		f = 1kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
		f = 10kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
MICROPHONE BIAS						
Output Voltage	$V_{MICBIAS}$	V_{AVDD} = 1.8V, I_{LOAD} = 1mA	1.5	1.525	1.55	V
Load Regulation		I_{LOAD} = 1mA to 2mA		0.2	10	V/A
Line Regulation		V_{AVDD} = 1.65V to 1.95V		10		µV/V
Power-Supply Rejection Ratio	PSRR	f = 217Hz, V_{RIPPLE} = $100mV_{P-P}$		85		dB
		f = 10kHz, V_{RIPPLE} = $100mV_{P-P}$		81		
Noise Voltage		A-weighted		9.1		$µV_{RMS}$
LINE INPUT						
Full-Scale Input	V_{IN}	AV_{LINE} = 0dB		1.0		V_{P-P}
Line Input Level Adjust Range	AV_{LINE}	LIGL/LIGR = 0xF to 0x0	-6.5		+24.5	dB
Line Input Mute Attenuation		f = 1kHz		100		dB
Input Resistance	R_{IN_LINE}	AV_{LINE} = +24dB	20			kΩ
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $0.1V_{P-P}$, f = 1kHz, differential output		-83		dB
AUXIN INPUT						
Input DC Voltage Range		AUXEN = 1	0		0.738	V
AUXIN Input Resistance	R_{IN}	AUXEN = 1, 0V ≤ AUXIN ≤ 0.738V	10	40		MΩ
JACK SENSE OPERATION						
Threshold	V_{TH}	JDETEN = 1, $\overline{SHDN}$ = 1, JACKSNS	0.92 x MICBIAS	0.95 x MICBIAS	0.98 x MICBIAS	V
		JDETEN = 1, $\overline{SHDN}$ = 0, JACKSNS, LOUTP	AVDD - 0.8	AVDD - 0.4	AVDD - 0.15	
Pullup Current	I_{PU}	JDETEN = 1, $\overline{SHDN}$ = 1, JACKSNS = GND		4		µA
		JDETEN = 1, $\overline{SHDN}$ = 0, JACKSNS = LOUTP = GND		4	20	
Pullup Voltage		JDETEN = 1, JACKSNS, LOUTP		AVDD		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL SIDETONE							
Sidetone Gain Adjust Range	AV_{STGA}	Differential output mode, DVST = 0x1F to 0x01		-60		0	dB
Voice Path Phase Delay	P_{DLY}	MIC input to headphone output, f = 1kHz, HP filter disabled, f_S = 8kHz			2.2		ms
INPUT CLOCK CHARACTERISTICS							
MCLK Input Frequency	f_{MCLK}	For any LRCLK sample rate		10		60	MHz
MCLK Input Duty Cycle		Prescaler = /1 mode		40		60	%
		/2 or /4 modes		30		70	
Maximum MCLK Input Jitter		Maximum allowable RMS for performance limits			100		ps_{RMS}
LRCLK Sample Rate Range				8		48	kHz
LRCLK PLL Lock Time		Any allowable LRCLK and PCLK rate, slave mode	Rapid lock mode		2	7	ms
			Nonrapid lock mode		12	25	
LRCLK Acceptable Jitter for Maintaining PLL Lock		Allowable LRCLK period change from nominal for slave PLL mode at any allowable LRCLK and PCLK rates				±100	ns
LRCLK Average Frequency Error (Master and Slave Modes) (Note 9)		FREQ = 0x8 through 0xF		0		0	%
		PCLK = 192xf_S, 256xf_S, 384xf_S, 512xf_S, 768xf_S, and 1024xf_S		0		0	
		All other modes		-0.025		+0.025	
DIGITAL INPUT (MCLK)							
Input High Voltage	V_{IH}			1.2			V
Input Low Voltage	V_{IL}					0.6	V
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C				±1	µA
Input Capacitance					10		pF
DIGITAL INPUTS (SDIN, BCLK, LRCLK)							
Input High Voltage	V_{IH}			0.7 x DVDDIO			V
Input Low Voltage	V_{IL}					0.3 x DVDDIO	V
Input Hysteresis					200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C				±1	µA
Input Capacitance					10		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDA, SCL)						
Input High Voltage	V_{IH}		0.7 x DVDD			V
Input Low Voltage	V_{IL}				0.3 x DVDD	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C			±1	µA
Input Capacitance				10		pF
DIGITAL INPUT (DIGMICDATA)						
Input High Voltage	V_{IH}		0.65 x DVDD			V
Input Low Voltage	V_{IL}				0.35 x DVDD	V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C			±35	µA
Input Capacitance				10		pF
CMOS DIGITAL OUTPUTS (BCLK, LRCLK, SDOUT)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 3mA	DVDDIO - 0.4			V
CMOS DIGITAL OUTPUT (DIGMICCLK)						
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 1mA	DVDD - 0.4			V
OPEN-DRAIN DIGITAL OUTPUTS (SDA, $\overline{IRQ}$)						
Output High Current	I_{OH}	V_{OUT} = V_{DVDD}, T_A = +25°C			1	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.2 x DVDD	V
DIGITAL MICROPHONE TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
DIGMICCLK Divide Ratio	f_{MICCLK}	MICCLK = 00		PCLK/8		MHz
		MICCLK = 01		PCLK/6		
DIGMICDATA to DIGMICCLK Setup Time	$t_{SU, MIC}$	Either clock edge	20			ns
DIGMICDATA to DIGMICCLK Hold Time	$t_{HD, MIC}$	Either clock edge	0			ns
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
Minimum BCLK Cycle Time	t_{BCLKS}	Slave operation		75		ns
	t_{BCLKM}	Master operation		325		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

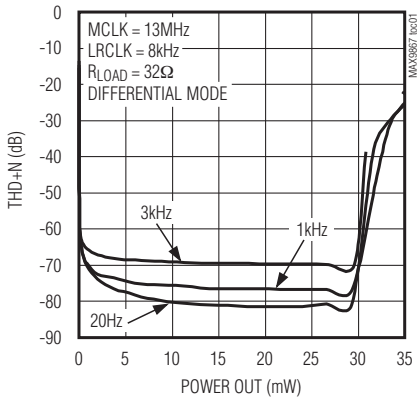
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum BCLK High Time	t_{BCLKH}	Slave operation		30		ns
Minimum BCLK Low Time	t_{BCLKL}	Slave operation		30		ns
BCLK or LRCLK Rise and Fall	t_R, t_F	Master operation, C_L = 15pF		7		ns
SDIN or LRCLK to BCLK Setup Time	t_{SU}		20			ns
SDIN or LRCLK to BCLK Hold Time	t_{HD}		0			ns
SDOUT Delay Time from BCLK Rising Edge	t_{DLY}	C_L = 30pF	0		40	ns
I^2C TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (REPEATED) START Condition	$t_{HD, STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a REPEATED START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	$R_{PU, SDA}$ = 475Ω	0		900	ns
Data Setup Time	$t_{SU, DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 10)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 10)	20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	$R_{PU, SDA}$ = 475Ω (Note 10)	20 + 0.1C_B		250	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 2: The MAX9867 is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 3: Clocking all zeros into the DAC, master mode, and differential headphone mode.
Note 4: DAC performance measured at the headphone outputs.
Note 5: Dynamic range measured using the EIAJ method. -60dBFS 1kHz output signal, A-weighted, and normalized to 0dBFS. f = 20Hz to 20kHz.
Note 6: Performance measured using microphone inputs, unless otherwise stated.
Note 7: Performance measured using line inputs.
Note 8: Performance measured using DAC, unless otherwise stated. LRCLK = 8kHz, unless otherwise stated.
Note 9: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.
Note 10: C_B is in pF.

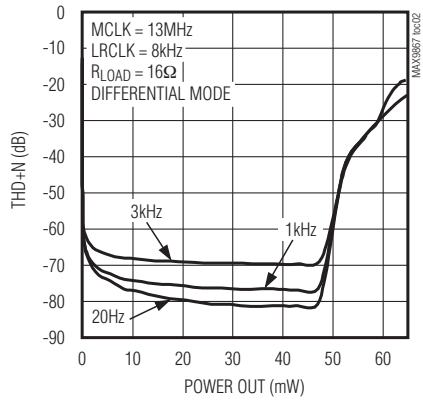
典型工作特性

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



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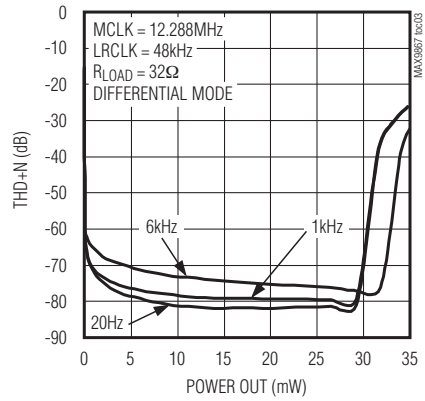
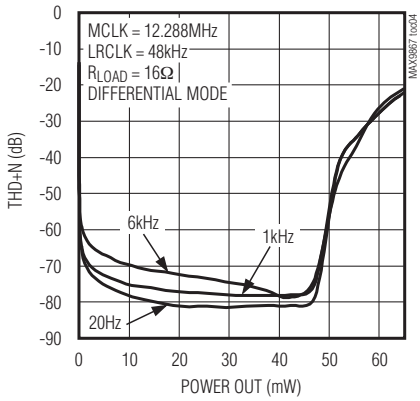
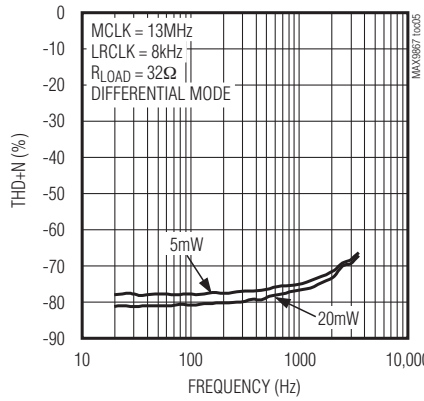


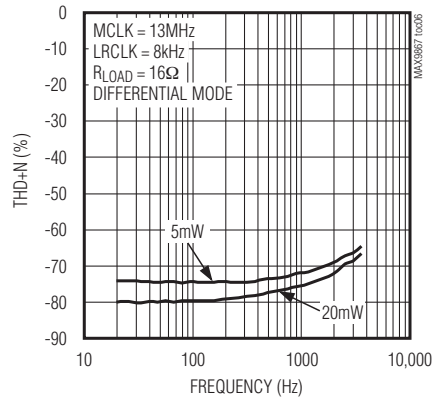
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



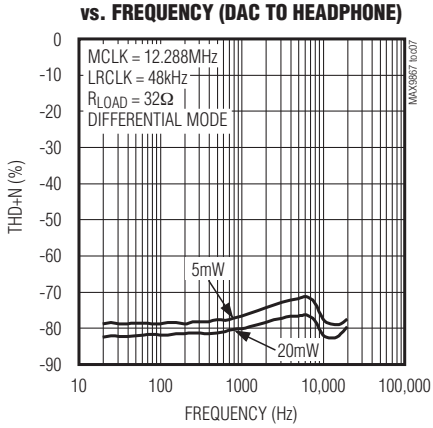
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



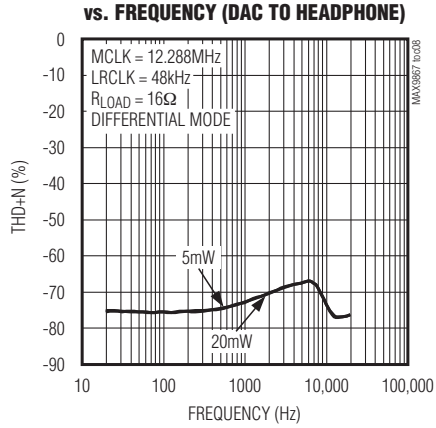
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



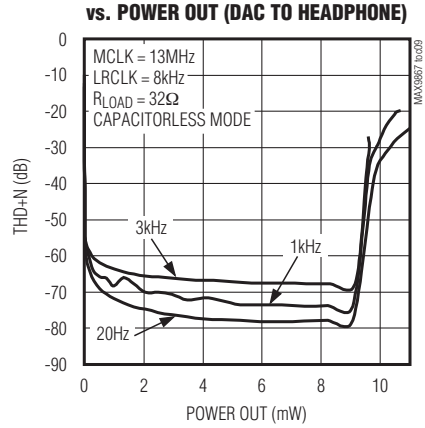
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)

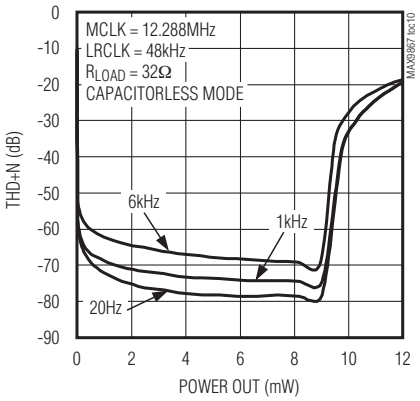


超低功耗、立体声音频编解码器

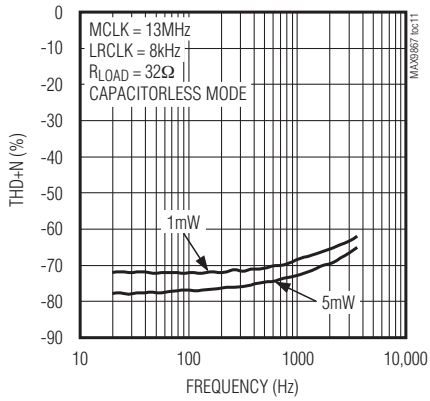
典型工作特性(续)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



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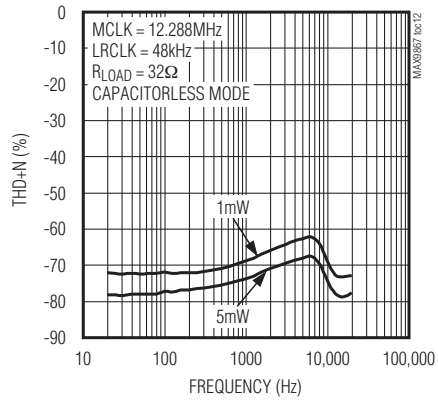

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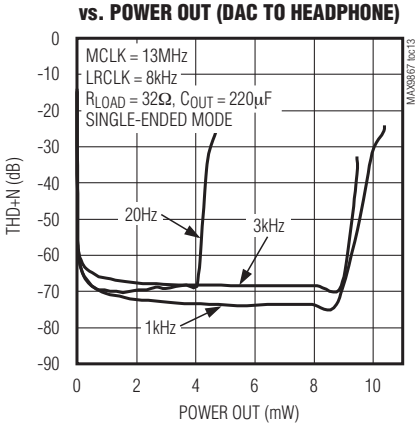

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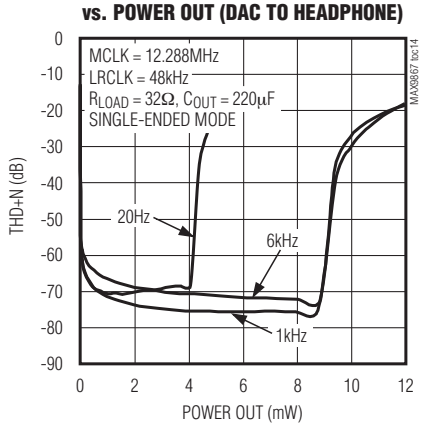
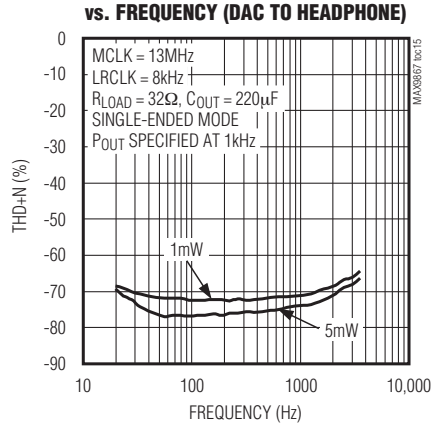
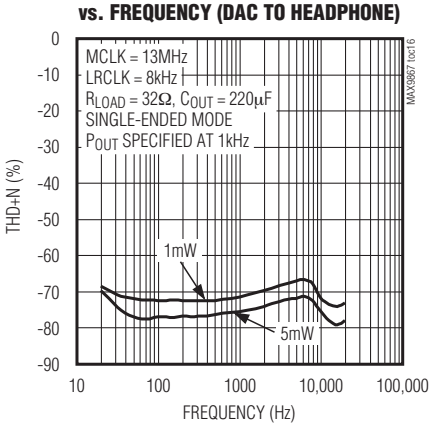


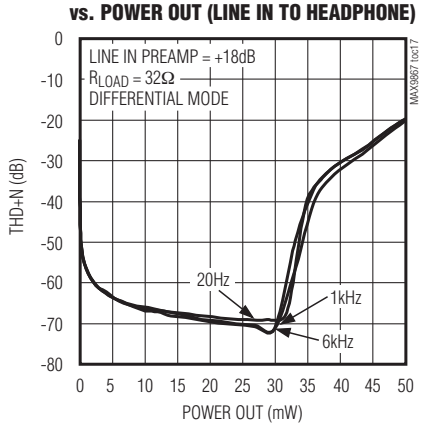
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



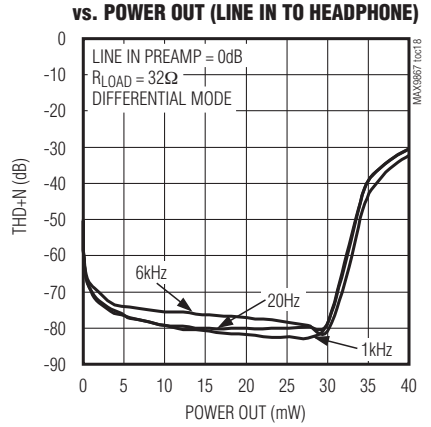
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE IN TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE IN TO HEADPHONE)



典型工作特性(续)

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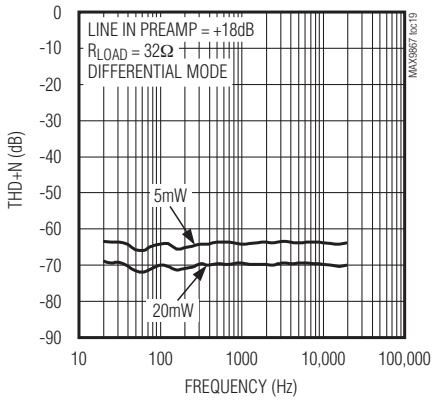
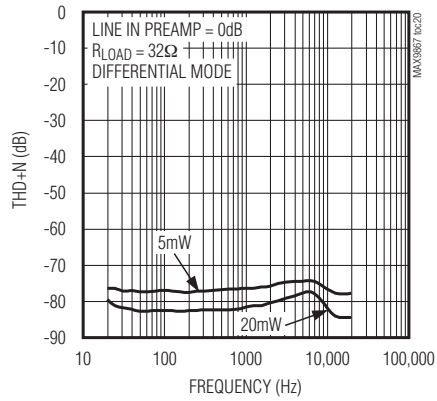
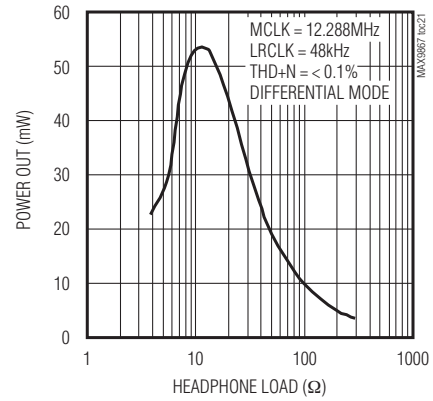
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE IN TO HEADPHONE)



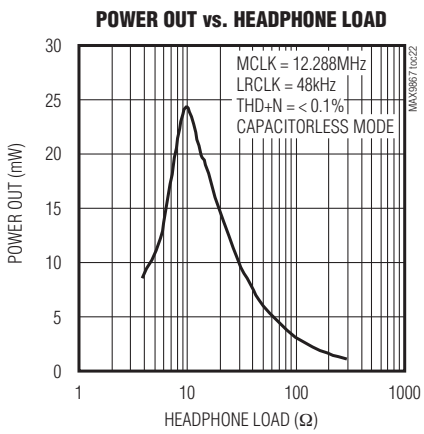
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE IN TO HEADPHONE)



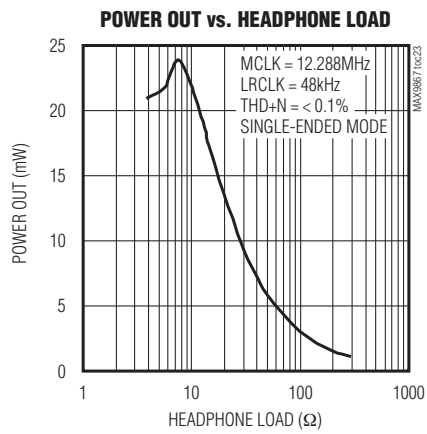
POWER OUT vs. HEADPHONE LOAD



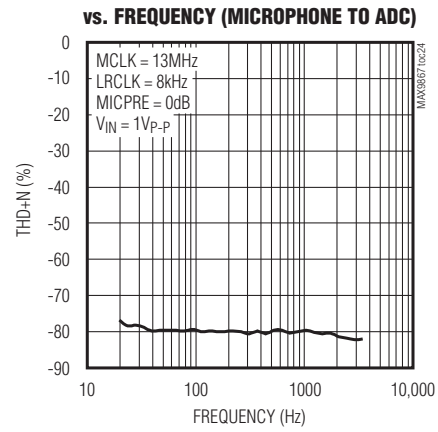
POWER OUT vs. HEADPHONE LOAD



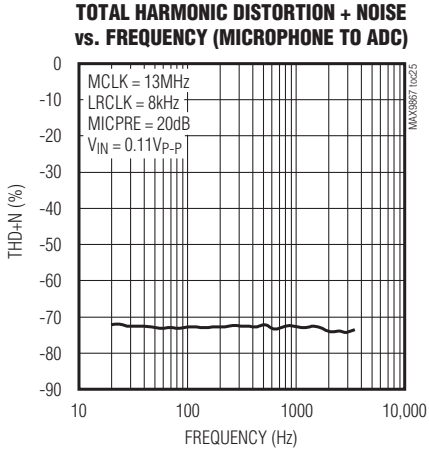
POWER OUT vs. HEADPHONE LOAD



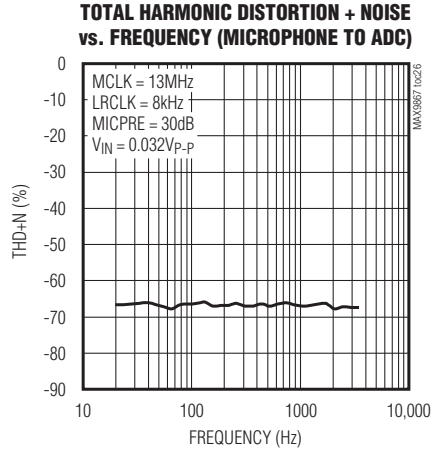
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



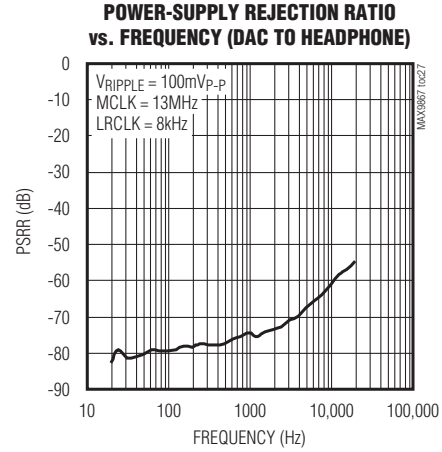
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)

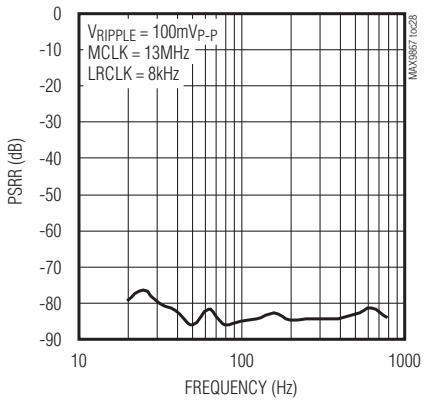


超低功耗、立体声音频编解码器

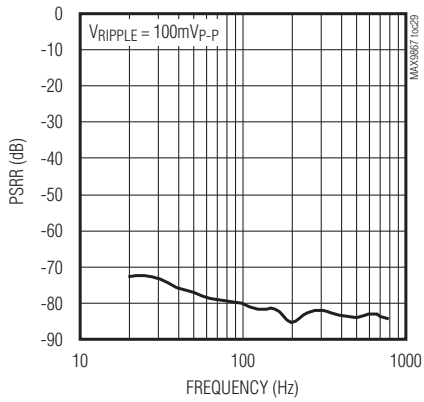
典型工作特性(续)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

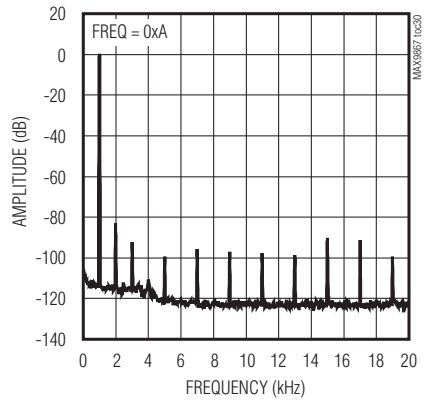
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



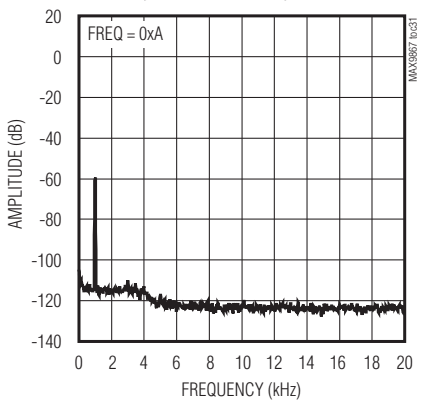
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MICBIAS)



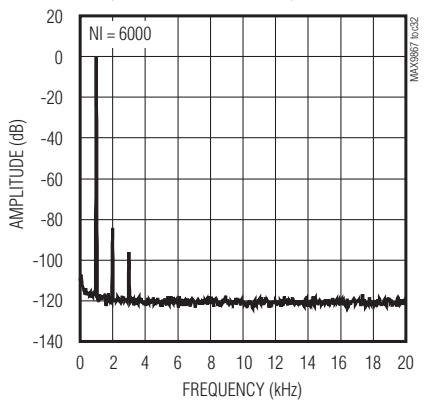
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 8kHz



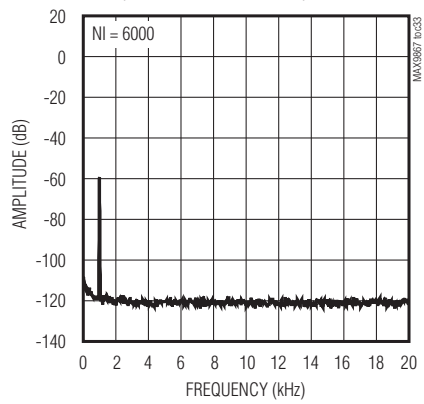
FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 8kHz



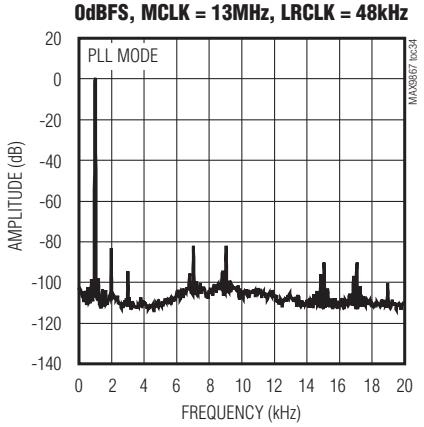
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



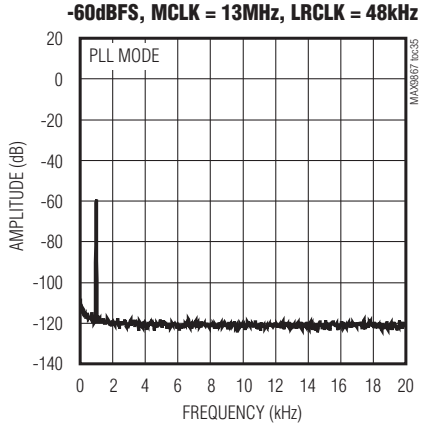
FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



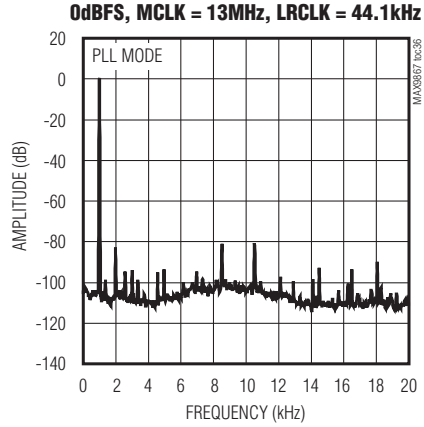
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 48kHz



FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 48kHz



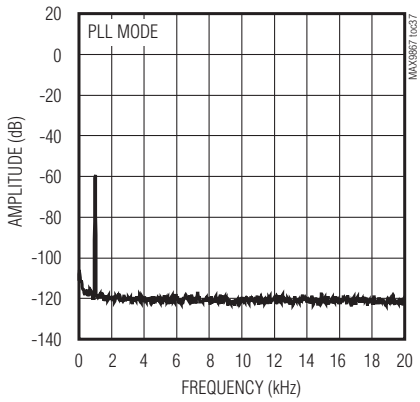
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 44.1kHz



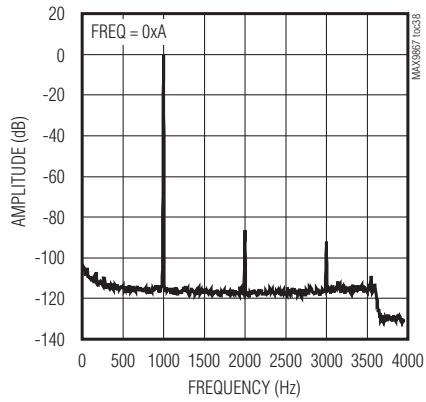
典型工作特性(续)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to $f_S/2$, T_A = +25°C, unless otherwise noted.)

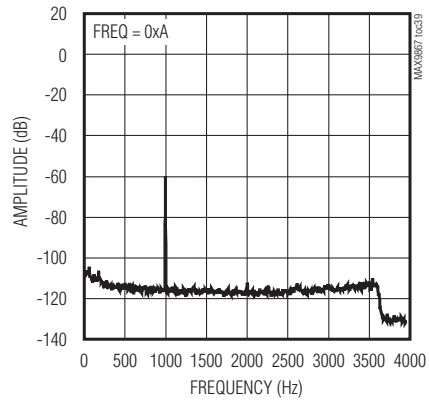
FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 44.1kHz



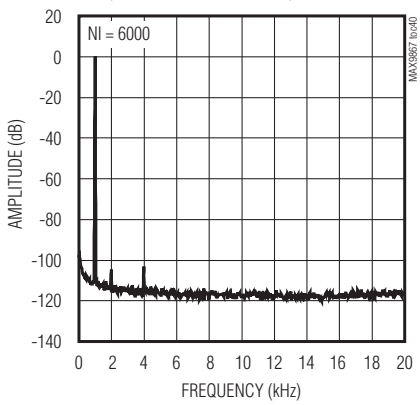
FFT, MICROPHONE TO ADC, 0dBFS, MCLK = 13MHz, LRCLK = 8kHz



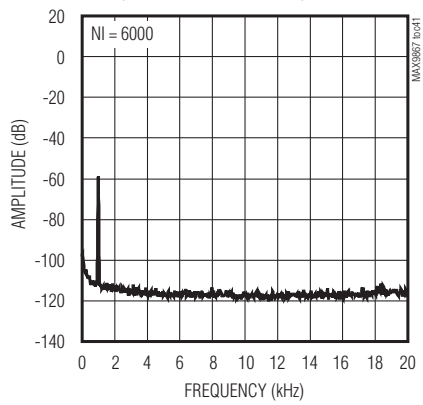
FFT, MICROPHONE TO ADC, -60dBFS, MCLK = 13MHz, LRCLK = 8kHz



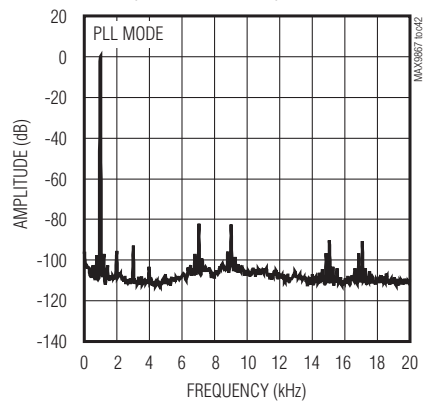
FFT, MICROPHONE TO ADC, 0dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



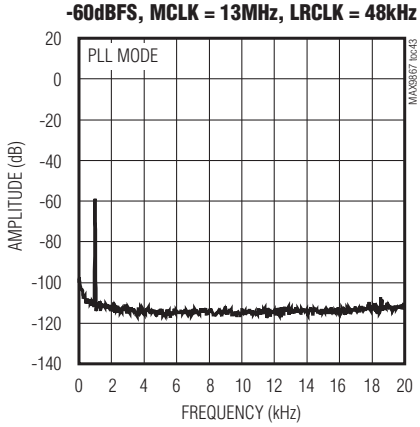
FFT, MICROPHONE TO ADC, -60dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



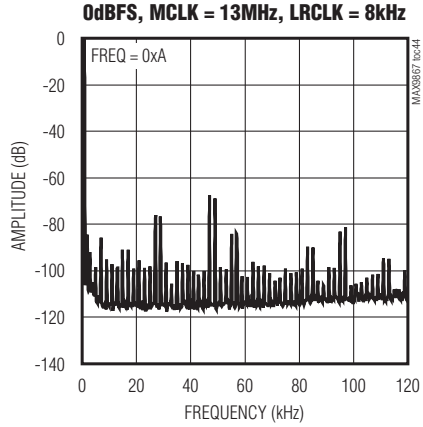
FFT, MICROPHONE TO ADC, 0dBFS, MCLK = 13MHz, LRCLK = 48kHz



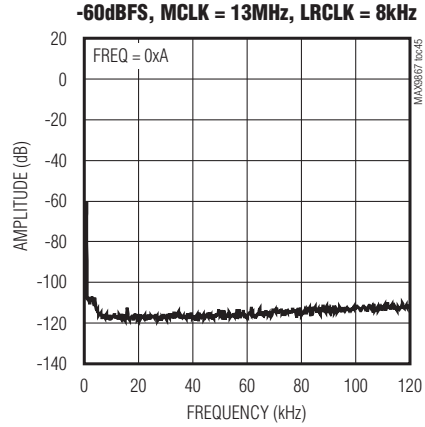
FFT, MICROPHONE TO ADC, -60dBFS, MCLK = 13MHz, LRCLK = 48kHz



WIDEBAND FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 8kHz



WIDEBAND FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 8kHz

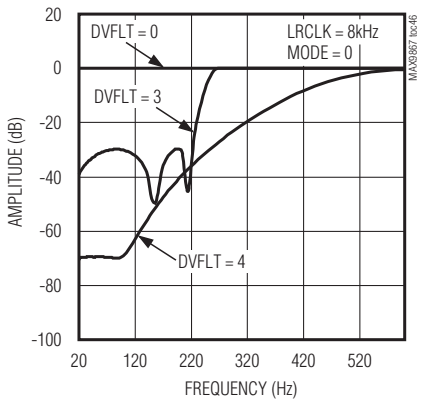


超低功耗、立体声音频编解码器

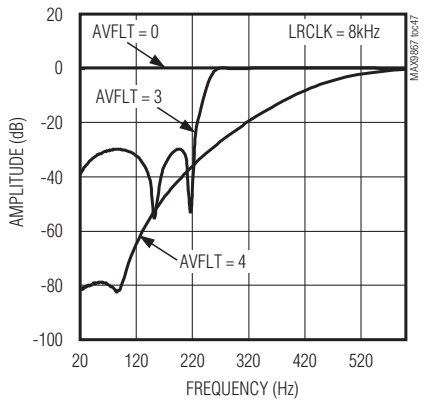
典型工作特性(续)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

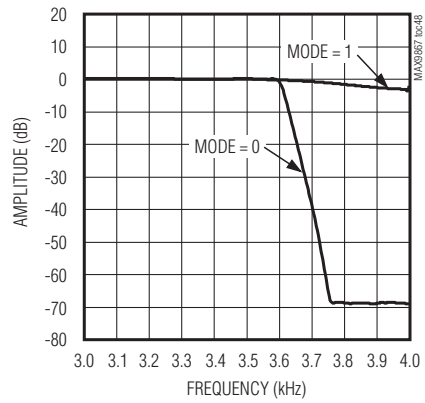
DAC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



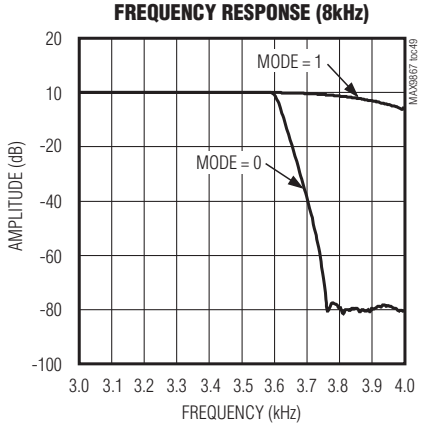
DAC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



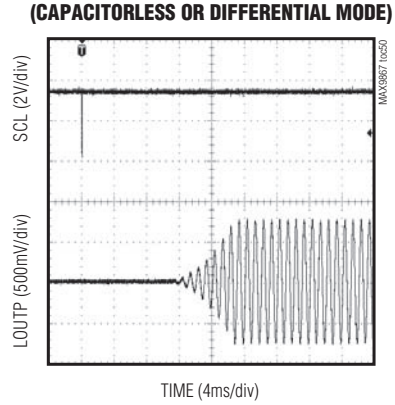
DAC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (8kHz)



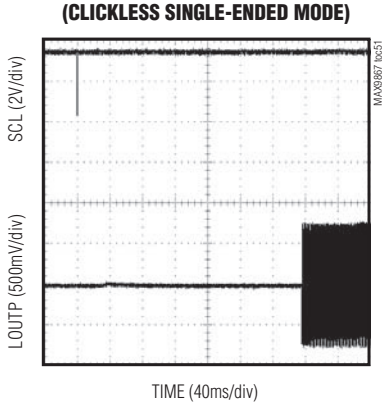
ADC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (8kHz)



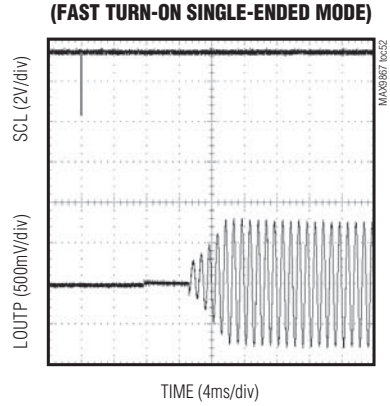
SHUTDOWN TO DAC FULL OPERATION (CAPACITORLESS OR DIFFERENTIAL MODE)



SHUTDOWN TO DAC FULL OPERATION (CLICKLESS SINGLE-ENDED MODE)



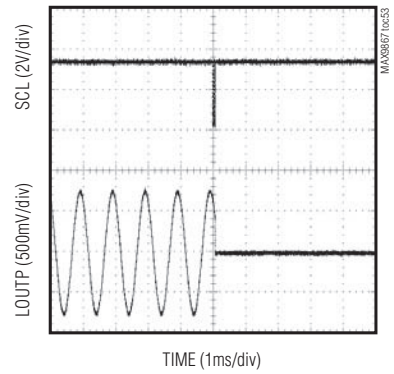
SHUTDOWN TO DAC FULL OPERATION (FAST TURN-ON SINGLE-ENDED MODE)



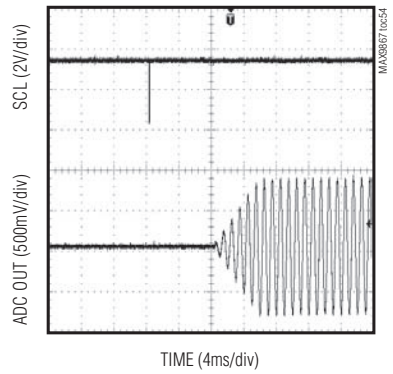
典型工作特性(续)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

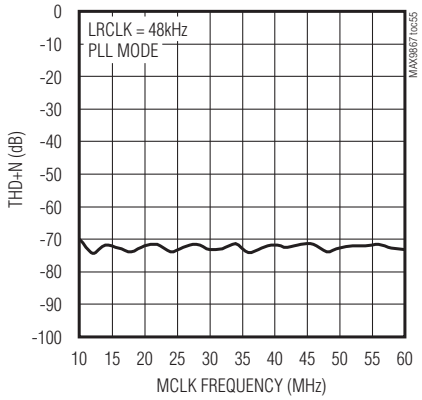
FULL OPERATION TO SHUTDOWN (DAC)



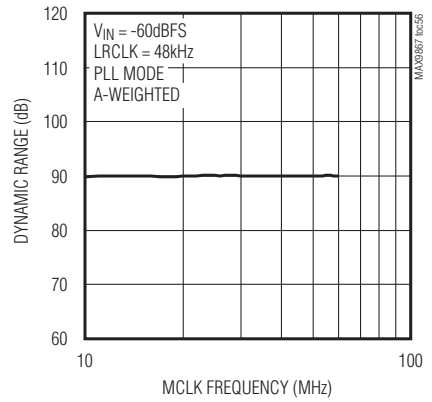
ADC SOFT-START



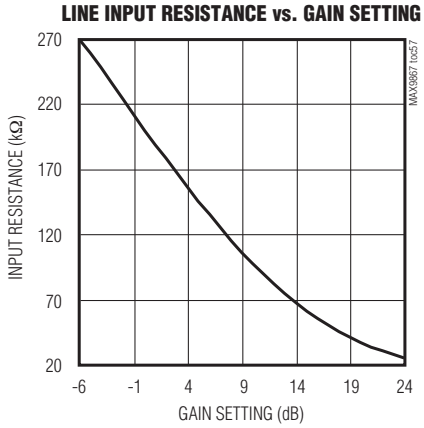
TOTAL HARMONIC DISTORTION + NOISE vs. MCLK FREQUENCY, 0dBFS



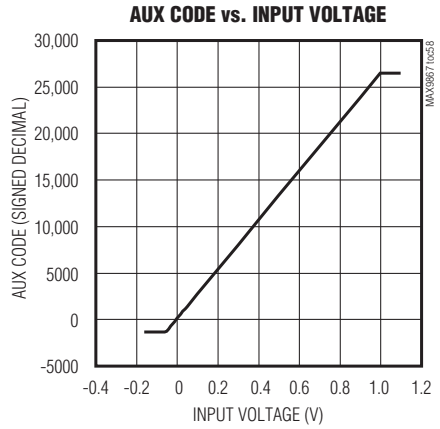
DYNAMIC RANGE vs. MCLK FREQUENCY



LINE INPUT RESISTANCE vs. GAIN SETTING



AUX CODE vs. INPUT VOLTAGE



引脚说明

引脚/焊球		名称	功能
TQFN-EP	WLP		
1	A2	DGND	数字地。
2	B3	SCL	I^2C串行时钟输入，通过一个电阻上拉到1.7V至3.3V电源。
3	A3	SDA	I^2C串行数据输入/输出，通过一个电阻上拉到1.7V至3.3V电源。
4	C3	$\overline{IRQ}$	硬件中断输出。$\overline{IRQ}$可设置成状态寄存器0x00中的状态位发生置位时拉低，读取状态寄存器0x00可清除$\overline{IRQ}$。通过读取寄存器0x00清中断之前，重复故障对$\overline{IRQ}$没有影响。将该引脚通过一个10kΩ电阻上拉到1.7V至3.3V电源。
5	A4	AVDD	模拟电源，采用一个1µF电容旁路至AGND。
6	B4	REF	转换器基准(1.23V标称值)，采用一个2.2µF电容旁路至AGND。
7	A5	PREG	正电压内部稳压源(1.6V标称值)，采用一个1µF电容旁路至AGND。
8	B5	REG	PREG/2电压基准(0.8V标称值)，采用一个1µF电容旁路至AGND。
9	A6	AGND	模拟地。
10	B6	MICBIAS	低噪声麦克风偏置。在麦克风的正向输出(1.525V标称值)端连接一个2.2kΩ至470Ω的外部电阻。采用一个1µF电容将其旁路至AGND。
11	C5	MICLN/ DIGMICCLK	左声道麦克风差分输入负端或数字麦克风时钟输出。对于模拟麦克风，通过1µF电容交流耦合至麦克风输出负端；对于数字麦克风，将其连接至麦克风时钟输入端。
12	C6	MICLP/ DIGMICDATA	左声道麦克风差分输入正端或数字麦克风数据输入。对于模拟麦克风，通过1µF电容交流耦合至麦克风输出正端；对于数字麦克风，将其连接至麦克风的数据输出端。可连接两个数字麦克风。
13	C4	MICRP	右声道麦克风差分输入正端，通过1µF电容交流耦合至麦克风输出正端。
14	D6	MICRN	右声道麦克风差分输入负端，通过1µF电容交流耦合至麦克风输出负端。
15	D5	LINL	左声道线入，通过1µF电容将模拟音频信号交流耦合至LINL。
16	E6	LINR	右声道线入，通过1µF电容将模拟音频信号交流耦合至LINR。
17	D4	JACKSNS/AUX	插孔检测或辅助ADC输入端。配置为插孔检测时，JACKSNS用于检测是否有信号线连接到插孔，详细信息请参考*模式配置*部分；配置为辅助ADC输入时，AUX用来测量直流电压。
18	E5	PGND	耳机电源地。
19	D3	ROUTP	右声道耳机输出正端。差分模式和无滤波电容模式下直接连接至负载；单端模式下交流耦合至负载。
20	E4	ROUTN	右声道耳机输出负端。差分模式下为反相输出；无滤波电容模式和快速开启单端模式下，该引脚悬空；无咔嗒声、单端模式下，通过1µF电容旁路至AGND。
21	D2	LOUTN	左声道耳机输出负端。差分模式下为同相输出；无滤波电容模式下为耳机返回公共端；快速开启单端模式下该引脚悬空；无咔嗒声、单端模式下，通过1µF电容旁路至AGND。

引脚说明(续)

引脚/焊球		名称	功能
TQFN-EP	WLP		
22	E3	LOUTP	左声道耳机输出正端。差分模式和无滤波电容模式下，直接连接至负载；单端模式下交流耦合至负载。
23	E2	PVDD	耳机电源，通过1µF电容旁路至PGND。
24, 25	—	N.C.	无连接。
26	E1	DVDDIO	数字音频接口电源，通过1µF电容旁路至DGND。
27	D1	SDOUT	数字音频串行数据ADC输出。
28	C2	SDIN	数字音频串行数据DAC输入。
29	C1	LRCLK	数字音频左/右声道时钟输入/输出。LRCLK为音频采样速率时钟，决定SDIN音频数据是否切换到左声道或右声道。TDM模式下，LRCLK为帧同步脉冲。MAX9867处于从机模式时，LRCLK为输入；MAX9867处于主机模式时，LRCLK为输出。
30	B1	BCLK	数字音频位的时钟输入/输出。MAX9867处于从机模式时，BCLK为输入；MAX9867处于主机模式时，BCLK为输出。
31	B2	MCLK	主机时钟输入，可接受输入频率范围：10MHz至60MHz。
32	A1	DVDD	数字电源。为数字电路、I²C接口供电，通过1µF电容旁路至DGND。
—	—	EP	裸焊盘，将裸焊盘连接至AGND。

详细说明

MAX9867是一款低功耗、立体声音频编解码器，设计用于需要低功耗的便携式应用。

立体声回放通路通过一个兼容于I²S、TDM和左对齐音频信号的接口接收数字音频信号。过采样Σ-Δ DAC将输入的数字数据流转换为模拟音频，并通过立体声耳机放大器输出。耳机放大器可配置为差分、单端以及无滤波电容输出模式。

立体声录音通路带有两路模拟麦克风输入，具有可选增益。麦克风可以由集成麦克风偏置电源供电。左声道模拟麦克风输入能够接受两个数字麦克风的数据。过采样Σ-Δ ADC转换麦克风信号，并通过数字音频接口输出数字比特流。

集成数字滤波为回放和录音通路提供一系列陷波和高通滤波器，抑制不需要的低频信号和GSM传输噪声。数字滤波能够提供高达70dB的带外能量衰减，消除音频混叠。数字侧音功能将录音通道的音频信号经过数字滤波后叠加到回放通路。

MAX9867还包括两路具有可调增益的立体声、单端线入，能够输入到ADC用于录音和/或耳机放大器输出。利用右声道音频ADC，辅助ADC可以精确测量直流电压，并通过I²C接口报告直流电压。插孔检测功能能够检测耳机、麦克风和耳机插孔。可对插入和拔出事件进行编程，用于触发硬件中断并置位I²C寄存器标志位。

MAX9867灵活的时钟电路采用可编程时钟分频器和数字PLL，使DAC和ADC能够在任何主时钟(MCLK)和采样速率(LRCLK)下实现最大的工作动态范围，无需消耗额外的电源电流。在8kHz至48kHz之间采样率下，主时钟支持10MHz至60MHz的任意频率，器件支持主、从模式，提供最大灵活性。

超低功耗、立体声音频编解码器

I²C寄存器

MAX9867音频编解码器可完全通过I²C接口进行软件控制。上电默认设置为全关断，需要通过编程内部寄存器开启器件，表1给出了完整的器件寄存器列表。

I²C从地址

MAX9867响应从地址为0x30的所有写命令和从地址为0x31的所有读操作。

表1. I²C寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS	POWER-ON RESET STATE
STATUS										
Status (Read Only)	CLD	SLD	ULK	0	0	0	JDET	0	0x00	—
Jack Sense (Read Only)	LSNS	JKSNS	JKMIC	0	0	0	0	0	0x01	—
AUX High (Read Only)	AUX[15:8]								0x02	—
AUX Low (Read Only)	AUX[7:0]								0x03	—
Interrupt Enable	ICLD	ISLD	IULK	0	0	$\overline{\text{SDODLY}}$	IJDET	0	0x04	0x00
CLOCK CONTROL										
System Clock	0	0	PSCLK		FREQ				0x05	0x00
Stereo Audio Clock Control High	PLL	NI[14:8]							0x06	0x00
Stereo Audio Clock Control Low	NI[7:1]							RLK/ NI[0]	0x07	0x00
DIGITAL AUDIO INTERFACE										
Interface Mode	MAS	WCI	BCI	DLY	HIZOFF	TDM	0	0	0x08	0x00
Interface Mode	0	0	0	LVOLFIX	DMONO	BSEL			0x09	0x00
DIGITAL FILTERING										
Codec Filters	MODE	AVFLT			0	DVFLT			0x0A	0x00
LEVEL CONTROL										
Sidetone	DSTS		0	DVST					0x0B	0x00
DAC Level	0	DACM	DACG		DACA				0x0C	0x00
ADC Level	AVL				AVR				0x0D	0x00
Left-Line Input Level	0	LILM	0	0	LIGL				0x0E	0x00
Right-Line Input Level	0	LIRM	0	0	LIGR				0x0F	0x00
Left Volume Control	0	VOLLM	VOLL						0x10	0x00
Right Volume Control	0	VOLRM	VOLR						0x11	0x00
Left Microphone Gain	0	PALEN	PGAML						0x12	0x00
Right Microphone Gain	0	PAREN	PGAMR						0x13	0x00
CONFIGURATION										
ADC Input	MXINL		MXINR		AUXCAP	AUXGAIN	AUXCAL	AUXEN	0x14	0x00
Microphone	MICCLK		DIGMICL	DIGMICR	0	0	0	0	0x15	0x00
Mode	DSLEW	$\overline{\text{VSEN}}$	$\overline{\text{ZDEN}}$	0	JDETEN	HPMODE			0x16	0x00
POWER MANAGEMENT										
System Shutdown	$\overline{\text{SHDN}}$	LNLEN	LNREN	0	DALEN	DAREN	ADLEN	ADREN	0x17	0x00
Revision	REV								0xFF	0x42

器件状态

状态寄存器0x00和0x01为只读寄存器，报告各种器件功能状态。在对状态寄存器执行读操作时清零状态寄存器位，并在下次发生了相应事件时置位。寄存器0x02和0x03报告加载到AUX的直流电压，详细信息请参考*ADC*部分和表2。

表2. 状态寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Status (Read Only)	CLD	SLD	ULK	0	0	0	JDET	0	0x00
Jack Sense (Read Only)	LSNS	JKSNS	JKMIC	0	0	0	0	0	0x01
AUX High (Read Only)	AUX[15:8]								0x02
AUX Low (Read Only)	AUX[7:0]								0x03

BITS	FUNCTION
CLD	**Clip Detect Flag** Indicates that a signal has reached or exceeded full scale in the ADC or DAC.
SLD	**Slew Level Detect Flag** When volume or gain changes are made, the slewing circuitry smoothly steps through all intermediate settings. When SLD is set high, all slewing has completed and the volume or gain is at its final value. SLD is also set when soft-start or stop is complete.
ULK	**Digital PLL Unlock Flag** Indicates that the digital audio PLL has become unlocked and digital signal data is not reliable.
JDET	**Headset Configuration Change Flag** JDET is set whenever there is a change in register 0x01, indicating that the headset configuration has changed.
LSNS	**LOUTP State (Valid if $\overline{SHDN}$ = 0, JDETEN = 1)** LSNS is set when the voltage at LOUTP exceeds AVDD - 0.4V. An internal pullup from AVDD to LOUTP causes this condition whenever there is no load on LOUTP. LSNS is only valid in differential and capacitorless output modes.
JKSNS	**JACKSNS State (Valid if JDETEN = 1)** JKSNS is set when the voltage at JACKSNS exceeds AVDD - 0.4V. An internal pullup from AVDD to JACKSNS causes this condition whenever there is no load on JACKSNS.
JKMIC	**Microphone Detection (Valid if PALEN or PAREN ≠ 00 and JDETEN = 1)** JKMIC is set when JACKSNS exceeds 0.95 x $V_{MICBIAS}$.
AUX	**Auxiliary Input Measurement** AUX is a 16-bit signed two's complement number representing the voltage measured at JACKSNS/AUX. Before reading a value from AUX, set AUXCAP to 1 to ensure a stable reading. After reading the value, set AUXCAP to 0. Use the following formula to convert the AUX value into an equivalent JACKSNS/AUX voltage: $Voltage = 0.738V \times \left(\frac{AUX}{k}\right)$ k = AUX value when AUXGAIN = 1. See the *ADC* section for complete details.

硬件中断

漏极开路引脚$\overline{IRQ}$用于报告硬件中断。发生中断时，$\overline{IRQ}$保持低电平，直到通过读取状态寄存器0x00响应中断。只有在中断使能位置位时，才会报告相应的置位状态位的硬件中断。每个中断使能位在寄存器0x00中都有一个相应的状态标识，请参见表3。

$\overline{SDODLY}$用于控制SDOUT时序，详细信息请参考*数字音频接口*部分。

时钟控制

MAX9867采用介于10MHz至60MHz的系统时钟作为主时钟(MCLK)。在内部，MAX9867需要10MHz至20MHz的时钟，因此需要预先对主时钟进行1、2或4分频，以产生内部时钟(PCLK)。PCLK为MAX9867的所有电路提供时钟，参见表4。

MAX9867支持从8kHz至48kHz的任何采样率，包括所有常见采样率(8kHz、16kHz、24kHz、32kHz、44.1kHz和48kHz)。为了适应各种系统架构，MAX9867支持三种主要时钟模式：

- **常规模式**：该模式利用15位时钟分频系数设置相对于预分频MCLK输入(PCLK)的采样率，使MCLK和LRCLK频率具有高度灵活性，并可用于主模式和从模式。
- **整数模式**：主机和从机模式下，可以对常见的MCLK频率(12MHz、13MHz、16MHz和19.2MHz)进行编程，支持整数模式下的8kHz和16kHz采样速率。这些模式下，MCLK和LRCLK速率通过FREQ位选择，而非NI和PLL控制位。
- **PLL模式**：工作在从模式时，PLL可以使能锁相到外部产生的LRCLK信号，该信号与PCLK之间不是整数倍关系。使能接口之前，将NI设置到最接近的要求比值，设置NI[0] = 1，使能PLL的快速锁定模式。如果NI[0] = 0，将忽略NI，且PLL锁定时间变慢。

表3. 中断寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Interrupt Enable	ICLD	ISLD	IULK	0	0	$\overline{SDODLY}$	IJDET	0	0x04

表4. 时钟控制寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER
System Clock	0	0	PSCLK		FREQ				0x05
Stereo Audio Clock Control High	PLL	NI[14:8]							0x06
Stereo Audio Clock Control Low	NI[7:1]							NI[0]	0x07

BITS	FUNCTION
PSCLK	**MCLK Prescaler** Divides MCLK to generate a PCLK between 10MHz and 20MHz. 00 = Disable clock for low-power shutdown. 01 = Select if MCLK is between 10MHz and 20MHz. 10 = Select if MCLK is between 20MHz and 40MHz. 11 = Select if MCLK is between 40MHz and 60MHz.

表4. 时钟控制寄存器(续)

BITS	FUNCTION			
FREQ	**Exact Integer Modes** Allows integer sampling for specific PCLK (prescaled MCLK) frequencies and 8kHz or 16kHz sample rates.			
	FREQ[3:0]	**PCLK (MHz)**	**LRCLK (kHz)**	**PCLK/LRCLK**
	0x00	Normal or PLL mode		
	0x1–0x7	Reserved	Reserved	Reserved
	0x8 **0x9**	12 12	8 16	1500 750
	0xA **0xB**	13 13	8 16	1625 812.5
	0xC **0xD**	16 16	8 16	2000 1000
	0xE **0xF**	19.2 19.2	8 16	2400 1200
	Modes 0x8–0xF are available in either master or slave mode. In slave mode, if the indicated PCLK/LRCLK ratio cannot be guaranteed, use PLL mode instead.			
PLL	**PLL Mode Enable** 0 = Valid for slave and master mode. The frequency of LRCLK is set by the NI divider bits. In master mode, the MAX9867 generates LRCLK using the specified divide ratio. In slave mode, the MAX9867 expects an LRCLK as specified by the divide ratio. 1 = Valid for slave mode only. A digital PLL locks on to any externally supplied LRCLK signal. **Rapid Lock Mode** To enable rapid lock mode, set NI to the nearest desired ratio and set NI[0] = 1 before enabling the interface.			
NI	**Normal Mode LRCLK Divider** When PLL = 0, the frequency of LRCLK is determined by NI. See Table 5 for common NI values. $NI = (65536 \times 96 \times f_{LRCLK})/f_{PCLK}$ f_{LRCLK} = LRCLK frequency f_{PCLK} = Prescaled MCLK internal clock frequency (PCLK) LRCLK > 24kHz is only valid for MODE = 0 (stereo audio mode). MODE = 1 (voice mode) requires LRCLK ≤ 24kHz.			

表5. 常见NI值

MCLK (MHz)	LRCLK (kHz)						
	PSCLK	**8**	**16**	**24**	**32**	**44.1**	**48**
11.2896	01	0x116A	0x22D4	0x343F	0x45A9	**0x6000**	0x687D
12	01	0x1062	0x20C5	0x3127	0x4189	0x5A51	0x624E
12.288	01	**0x1000**	**0x2000**	**0x3000**	**0x4000**	0x5833	**0x6000**
13	01	0x0F20	0x1E3F	0x2D5F	0x3C7F	0x535F	0x5ABE
19.2	01	0x0A3D	0x147B	0x1EB8	0x28F6	0x3873	0x3D71
24	10	0x1062	0x20C5	0x1893	0x4189	0x5A51	0x624E
26	10	0x0F20	0x1E3F	0x16AF	0x3C7F	0x535F	0x5ABE
27	10	0x0E90	0x1D21	0x15D8	0x3A41	0x5048	0x5762

注：用粗体表示的整数值可提供最大的满度性能。

数字音频接口

MAX9867的数字音频接口支持各种工作模式，提供广泛的兼容性，请参考图1至图4时序图。主模式下，MAX9867输出LRCLK和BCLK；从模式下，这些引脚为输入。工作在主模式时，能以各种方式配置BCLK，确保与其它音频装置兼容。

无论VOLL和VOLR状态如何，LVOLFIX可以将线入回放音量固定到0dB，详细信息请参考线入和表6。

表6. 数字音频接口寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Interface Mode	MAS	WCI	BCI	DLY	HIZOFF	TDM	0	0	0x08
Interface Mode	0	0	0	LVOLFIX	DMONO	BSEL			0x09

BITS	FUNCTION
MAS	**Master Mode** 0 = The MAX9867 operates in slave mode with LRCLK and BCLK configured as inputs. 1 = The MAX9867 operates in master mode with LRCLK and BCLK configured as outputs.
WCI	**LRCLK Invert** 0 = Left-channel data is input and output while LRCLK is low. 1 = Right-channel data is input and output while LRCLK is low. **Note:** WCI is ignored when TDM = 1.
BCI	**BCLK Invert** In master and slave modes: 0 = SDIN is latched into the part on the rising edge of BCLK. SDOUT transitions after the rising edge of BCLK as determined by $\overline{\text{SDODLY}}$. 1 = SDIN is latched into the part on the falling edge of BCLK. SDOUT transitions after the falling edge of BCLK as determined by $\overline{\text{SDODLY}}$. In master mode: 0 = LRCLK changes state immediately after the rising edge of BCLK. 1 = LRCLK changes state immediately after the falling edge of BCLK.
$\overline{\text{SDODLY}}$	**SDOUT Delay** 0 = SDOUT transitions one half BCLK cycle after SDIN is latched into the part. 1 = SDOUT transitions on the same BCLK edge as SDIN is latched into the part. See Figures 1–4 for complete details. See Register 0x04 (interrupt registers).
DLY	**Delay Mode** 0 = SDIN/SDOUT data is latched on the first BCLK edge following an LRCLK edge. 1 = SDIN/SDOUT data is assumed to be delayed one BCLK cycle so that it is latched on the 2nd BCLK edge following an LRCLK edge (I^2S-compatible mode). **Note:** DLY is ignored when TDM = 1.
HIZOFF	**SDOUT High-Impedance Mode** 0 = SDOUT goes to a high-impedance state after all data bits have been transferred out of the MAX9867, allowing SDOUT to be shared by other devices. 1 = SDOUT is set either high or low after all data bits have been transferred out of the MAX9867. **Note:** High-impedance mode is intended for use when TDM = 1.
LVOLFIX	See the *Line Inputs* section.

表6. 数字音频接口寄存器(续)

BITS	FUNCTION
TDM	**TDM Mode Select** 0 = LRCLK signal polarity indicates left and right audio. 1 = LRCLK is a framing pulse that transitions polarity to indicate the start of a frame of audio data consisting of multiple channels. When operating in TDM mode, the left channel is output immediately following the frame sync pulse. If right-channel data is being transmitted, the 2nd channel of data immediately follows the 1st channel data.
DMONO	**Mono Playback Mode** 0 = Stereo data input on SDIN is processed separately. 1 = Stereo data input on SDIN is mixed to a single channel and routed to both the left and right DAC.
BSEL	**BCLK Select** Configures BCLK when operating in master mode. BSEL has no effect in slave mode. Set BSEL = 010, unless sharing the bus with multiple devices: 000 = Off 001 = 64x LRCLK (192x internal clock divided by 3) 010 = 48x LRCLK (192x internal clock divided by 4) 011 = Reserved for future use. 100 = PCLK/2 101 = PCLK/4 110 = PCLK/8 111 = PCLK/16

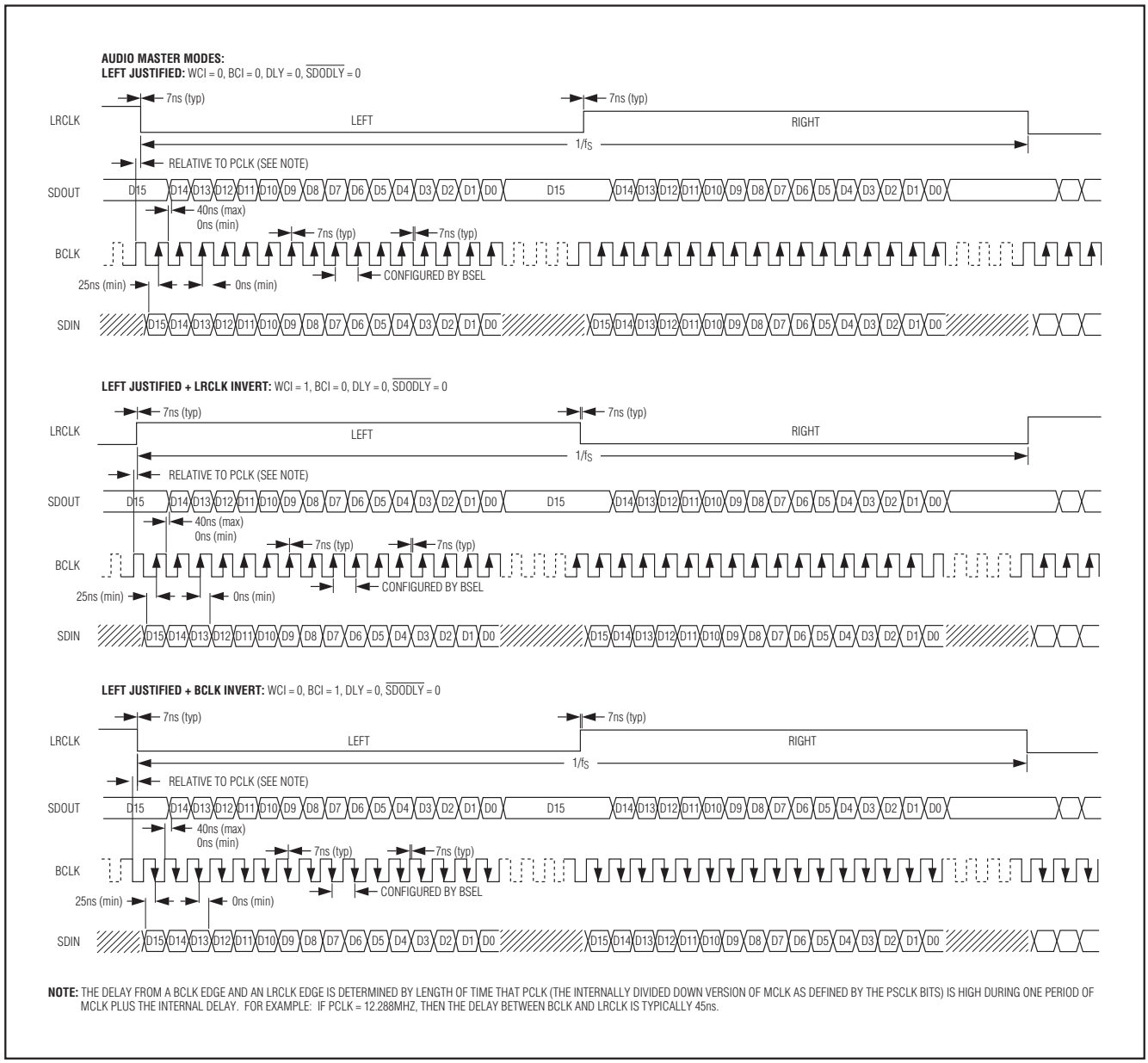


图1. 数字音频接口音频主模式示例(1/2)

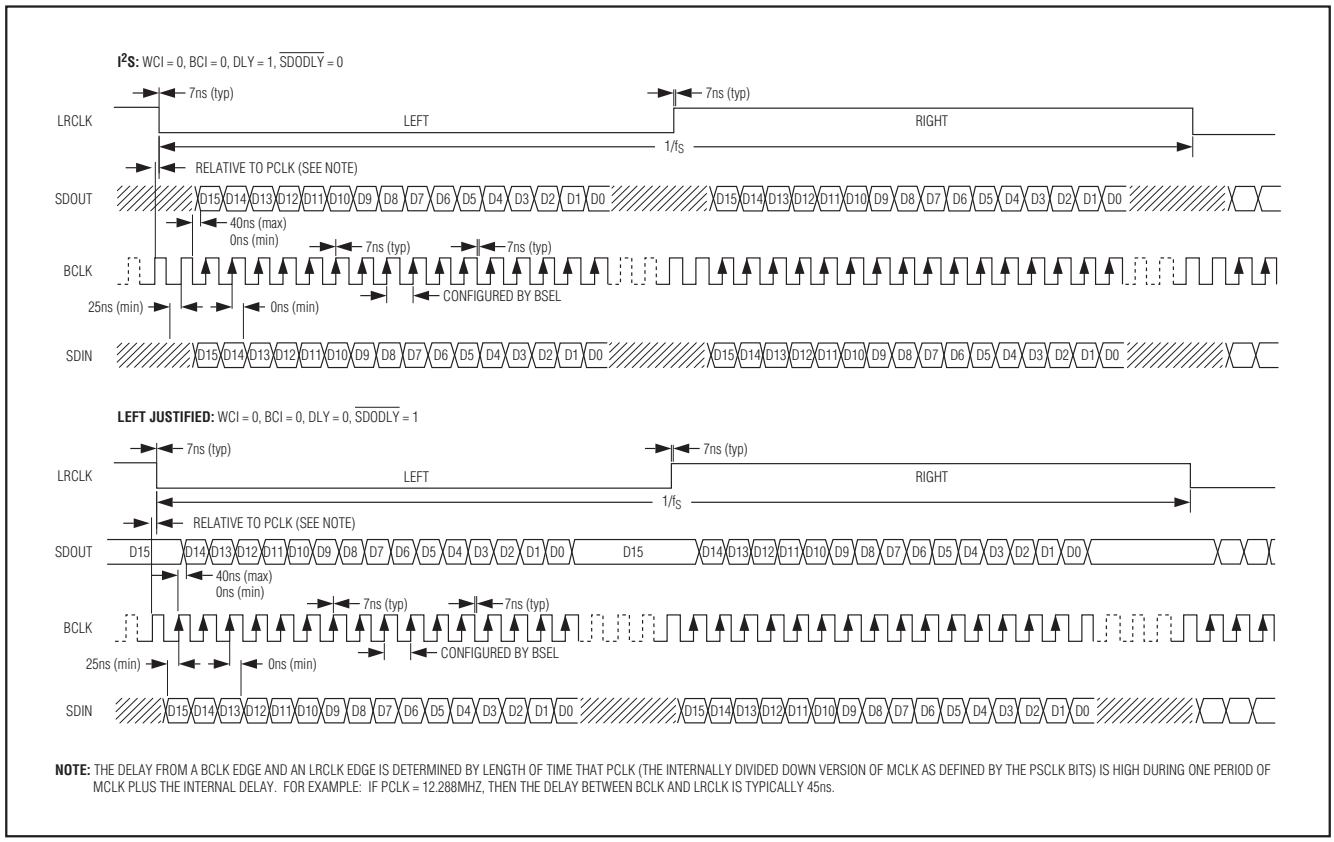


图1. 数字音频接口音频主模式示例(2/2)

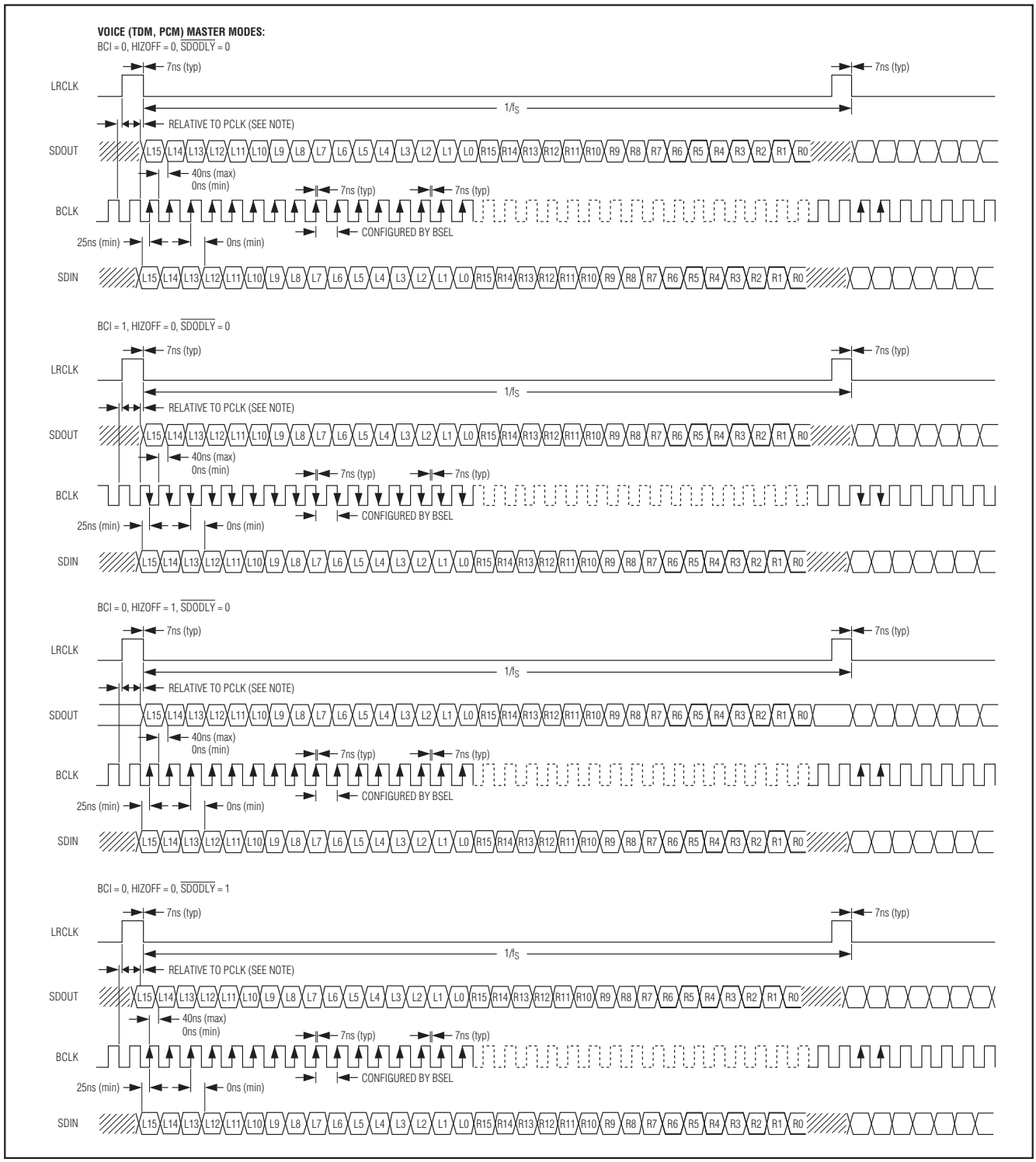


图2. 数字音频接口语音主模式示例

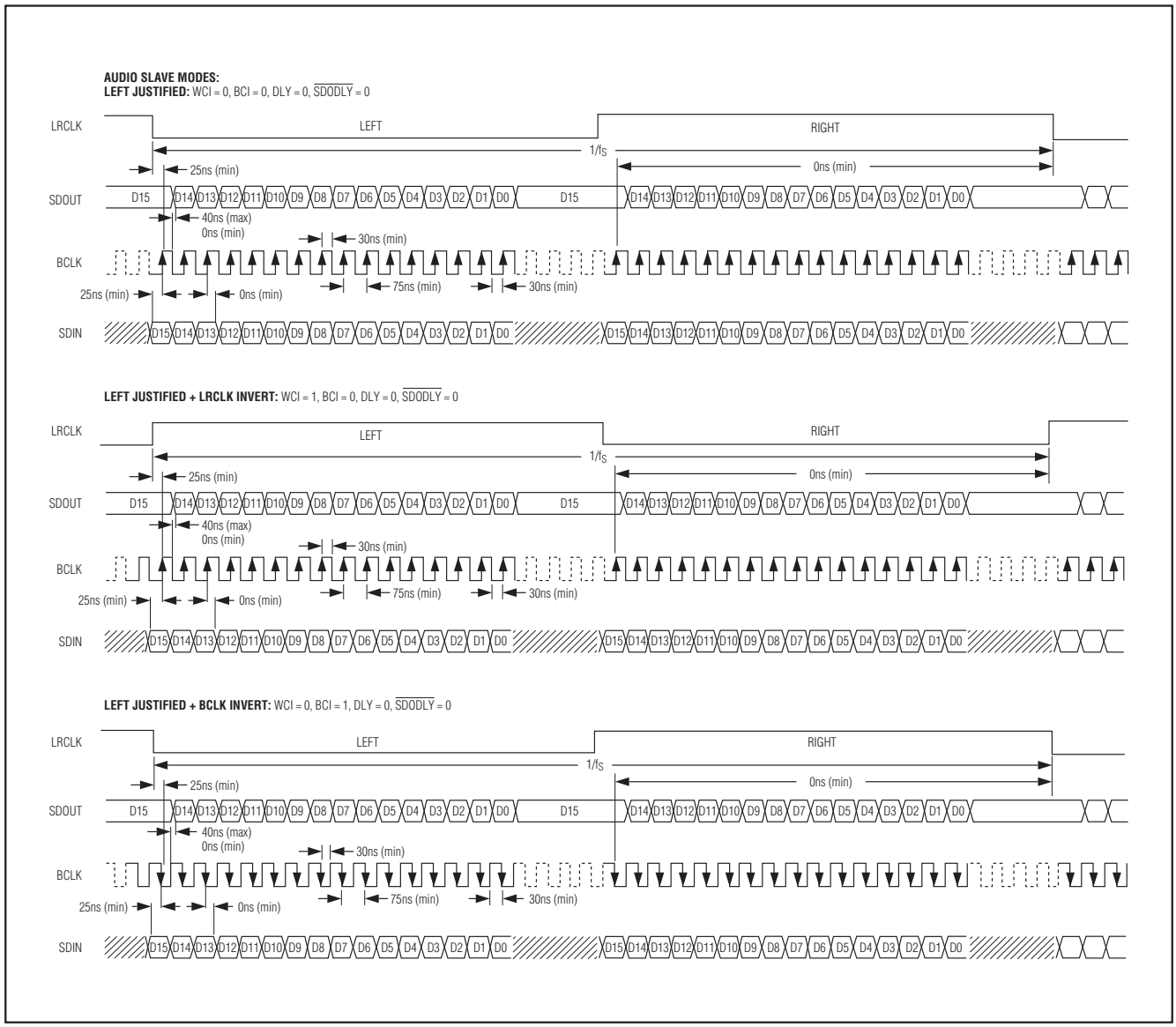


图3. 数字音频接口音频从模式示例(1/2)

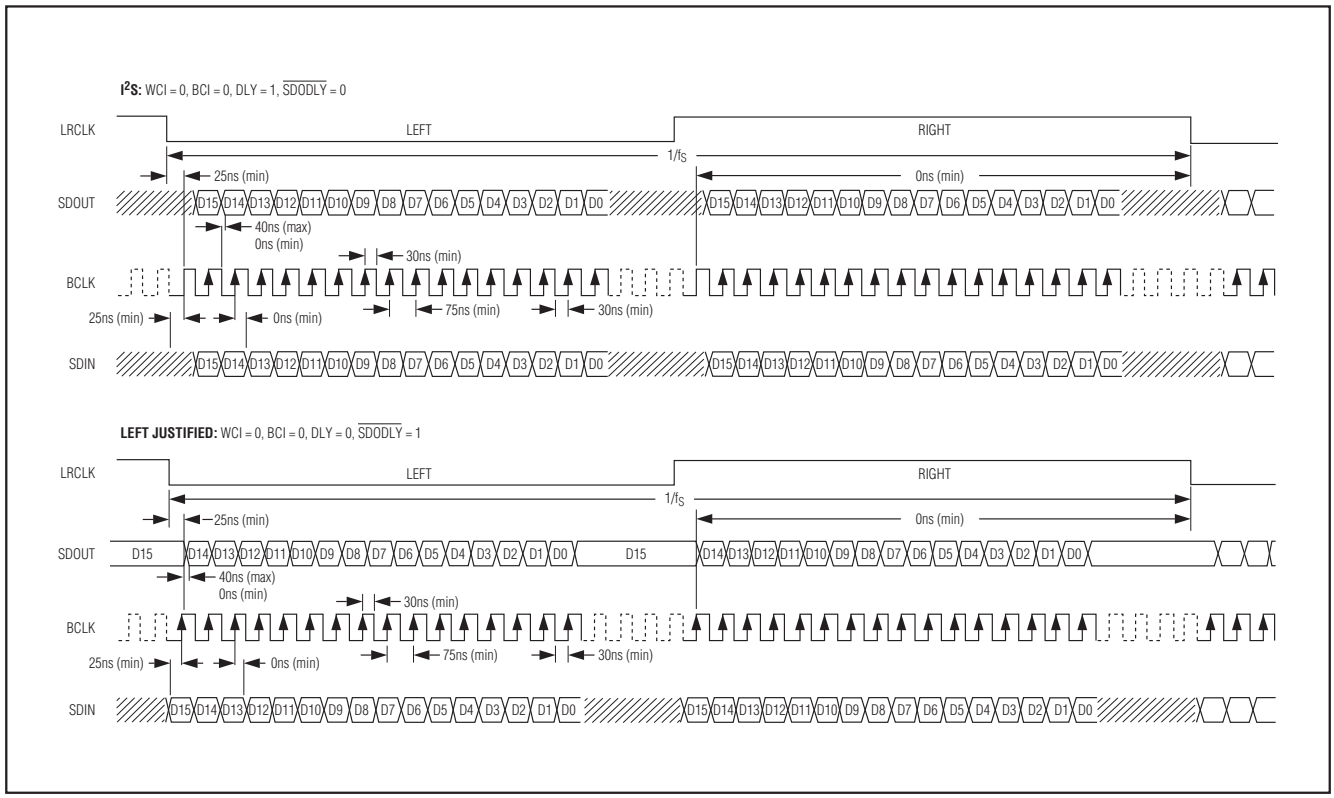


图3. 数字音频接口音频从模式示例(2/2)

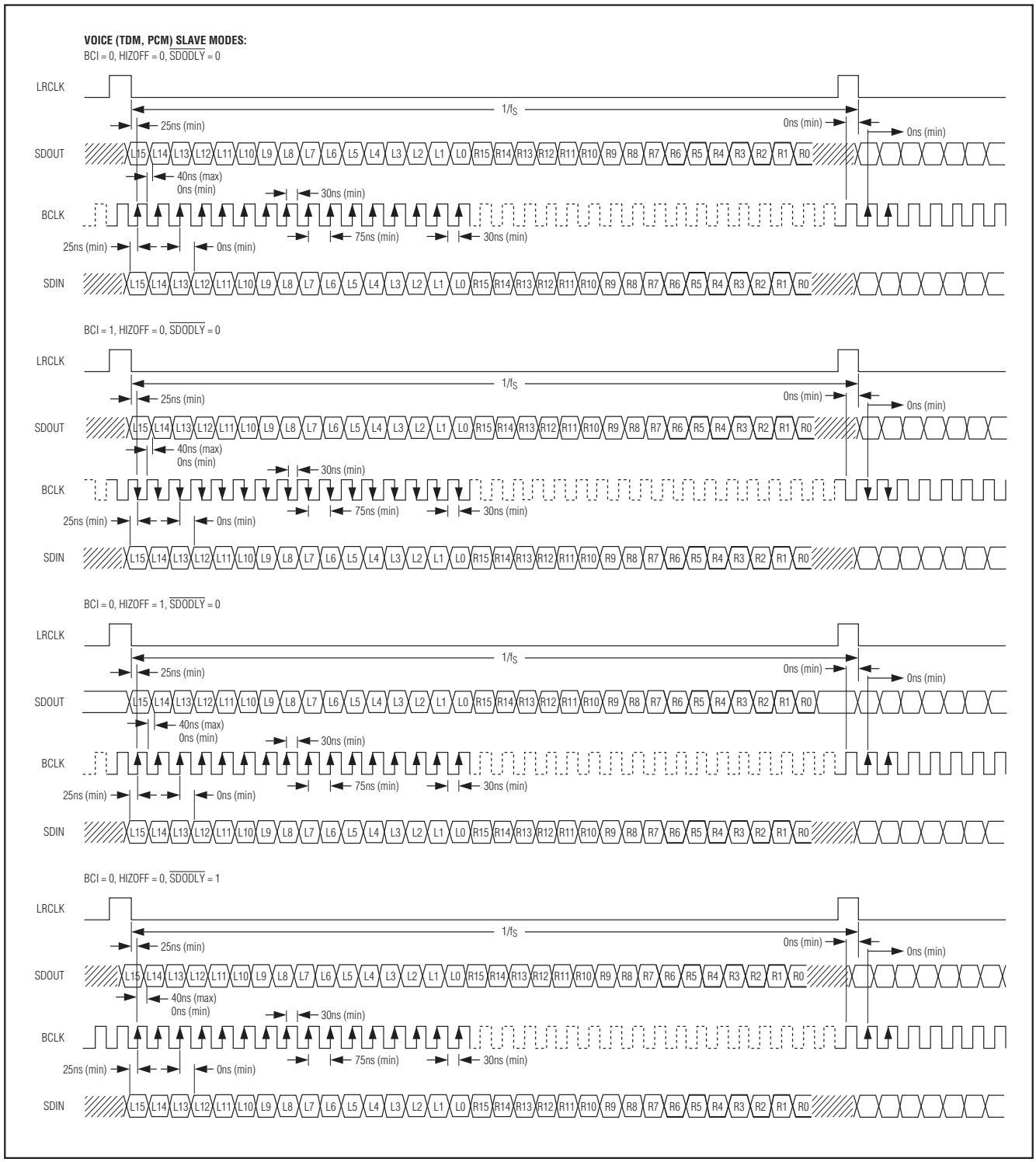


图4. 数字音频接口语音从模式示例

数字滤波

MAX9867带有IIR (语音)和FIR (音频)数字滤波器，可适应范围较广的音频源。IIR滤波器提供70dB阻带衰减以及可选择的高通滤波器。FIR滤波器具有低功耗和线性相位特性，可保持立体声镜像，表7所示为数字滤波寄存器。

表7. 数字滤波寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Codec Filters	MODE	AVFLT			0	DVFLT			0x0A

BITS	FUNCTION
MODE	**Digital Audio Filter Mode** 0 = IIR Voice Filters 1 = FIR Audio Filters
AVFLT	**ADC Digital Audio Filter** **MODE = 0** Select the desired digital filter response from Table 8. See the Frequency Response graph in the *Typical Operating Characteristics* section for details on each filter. **MODE = 1** 0x0 = DC-blocking filter is disabled. Any other setting = DC-blocking filter is enabled.
DVFLT	**DAC Digital Audio Filter** **MODE = 0** Select the desired digital filter response from Table 8. See the Frequency Response graph in the *Typical Operating Characteristics* section for details on each filter. **MODE = 1** 0x0 = DC-blocking filter is disabled. Any other setting = DC-blocking filter is enabled.

表8. IIR高通数字滤波器

CODE	FILTER TYPE	INTENDED SAMPLE RATE (kHz)	HIGHPASS CORNER FREQUENCY (Hz)	217Hz NOTCH
0x0	Disabled			
0x1	Elliptical	16	256	Yes
0x2	Butterworth	16	500	No
0x3	Elliptical	8	256	Yes
0x4	Butterworth	8	500	No
0x5	Butterworth	8 to 24	f_S/240	No
0x6 to 0x7	Reserved			

数字增益控制

MAX9867为回放和录音通路提供数字增益调整功能。两个录音通道的增益调整相互独立。器件还提供侧音增益调整，用于设置相对于回放电平的侧音电平，表9所示为数字增益寄存器。

表9. 数字增益寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Sidetone	DSTS		0	DVST					0x0B
DAC Level	0	DACM	DACG		DACA				0x0C
ADC Level	AVL				AVR				0x0D

BITS	FUNCTION
DSTS	**Digital Sidetone Source Mixer** 00 = No sidetone is selected. 01 = Left ADC 10 = Right ADC 11 = Left + right ADC
DVST	**Digital Sidetone Level Control** All gain settings are relative to the ADC input voltage.

Differential Headphone Output Mode

SETTING	GAIN (dB)	SETTING	GAIN (dB)	SETTING	GAIN (dB)
0x00	Off	0x0B	-20	0x16	-42
0x01	0	0x0C	-22	0x17	-44
0x02	-2	0x0D	-24	0x18	-46
0x03	-4	0x0E	-26	0x19	-48
0x04	-6	0x0F	-28	0x1A	-50
0x05	-8	0x10	-30	0x1B	-52
0x06	-10	0x11	-32	0x1C	-54
0x07	-12	0x12	-34	0x1D	-56
0x08	-14	0x13	-36	0x1E	-58
0x09	-16	0x14	-38	0x1F	-60
0x0A	-18	0x15	-40	—	—

Capacitorless and Single-Ended Headphone Output Mode

SETTING	GAIN (dB)	SETTING	GAIN (dB)	SETTING	GAIN (dB)
0x00	Off	0x0B	-25	0x16	-47
0x01	-5	0x0C	-27	0x17	-49
0x02	-7	0x0D	-29	0x18	-51
0x03	-9	0x0E	-31	0x19	-53
0x04	-11	0x0F	-33	0x1A	-55
0x05	-13	0x10	-35	0x1B	-57
0x06	-15	0x11	-37	0x1C	-59
0x07	-17	0x12	-39	0x1D	-61
0x08	-19	0x13	-41	0x1E	-63
0x09	-21	0x14	-43	0x1F	-65
0x0A	-23	0x15	-45	—	—

BITS	FUNCTION
DACM	**DAC Mute Enable** 0 = No mute 1 = Mute

表9. 数字增益寄存器(续)

BITS	FUNCTION			
DACG	**DAC Gain** 00 = 0dB 01 = +6dB 10 = +12dB 11 = +18dB **Note:** DACG is only used when MODE = 0. If MODE = 1, the DAC level is only set by DACA.			
DACA	**DAC Level Control** DACA works in all modes.			
	SETTING	**GAIN (dB)**	**SETTING**	**GAIN (dB)**
	0x0	0	0x8	-8
	0x1	-1	0x9	-9
	0x2	-2	0xA	-10
	0x3	-3	0xB	-11
	0x4	-4	0xC	-12
	0x5	-5	0xD	-13
	0x6	-6	0xE	-14
	0x7	-7	0xF	-15
AVL/AVR	**ADC Left/Right Level Control**			
	SETTING	**GAIN (dB)**	**SETTING**	**GAIN (dB)**
	0x0	+3	0x8	-5
	0x1	+2	0x9	-6
	0x2	+1	0xA	-7
	0x3	0	0xB	-8
	0x4	-1	0xC	-9
	0x5	-2	0xD	-10
	0x6	-3	0xE	-11
	0x7	-4	0xF	-12

线入

MAX9867包括一对单端线入。使能时，线入直接连接至耳机放大器，也可连接至ADC，用于录音，表10所示为线入寄存器。

表10. 线入寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Left-Line Input Level	0	LILM	0	0	LIGL				0x0E
Right-Line Input Level	0	LIRM	0	0	LIGR				0x0F

表10. 线入寄存器(续)

BITS	FUNCTION			
LILM/LIRM	**Line-Input Left/Right Playback Mute** 0 = Line input is connected to the headphone amplifiers. 1 = Line input is disconnected from the headphone amplifiers.			
LIGL/LIGR	**Line-Input Left/Right Gain**			
	SETTING	**GAIN (dB)**	**SETTING**	**GAIN (dB)**
	0x0	+24	0x8	+8
	0x1	+22	0x9	+6
	0x2	+20	0xA	+4
	0x3	+18	0xB	+2
	0x4	+16	0xC	0
	0x5	+14	0xD	-2
	0x6	+12	0xE	-4
	0x7	+10	0xF	-6
LVOLFIX	**Fix Line Input Volume** 0 = Line input to headphone output volume tracks VOLL and VOLR bits. 1 = Line input to headphone output volume fixed at VOLL and VOLR bits. See the *Digital Audio Interface* section.			

回放音量

MAX9867包含音量和静音控制，为回放音频通道提供电平控制。通过寄存器0x10和0x11设置所要求的音量，参见表11。

表11. 回放音量寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Left Volume Control	0	VOLLM	VOLL						0x10
Right Volume Control	0	VOLRM	VOLR						0x11

表11. 回放音量寄存器(续)

<table>
<tr><th>BITS</th><th colspan="6">FUNCTION</th></tr>
<tr><td>VOLLM/VOLRM</td><td colspan="6">Left/Right Playback Mute
VOLLM and VOLRM mute both the DAC and line input audio signals.
0 = Audio playback is unmuted.
1 = Audio playback is muted
Note: VSEN has no effect on the mute function. When VOLLM or VOLRM is set, the output is muted immediately ($\overline{ZDEN}$ = 1) or at the next zero-crossing ($\overline{ZDEN}$ = 0).</td></tr>
<tr><td rowspan="19">VOLL/VOLR</td><td colspan="6">Left/Right Playback Volume
VOLL and VOLR control the playback volume for both the DAC and line input audio signals.</td></tr>
<tr><td>SETTING</td><td>GAIN (dB)</td><td>SETTING</td><td>GAIN (dB)</td><td>SETTING</td><td>GAIN (dB)</td></tr>
<tr><td>0x00</td><td>+6</td><td>0x0E</td><td>-5</td><td>0x1C</td><td>-42</td></tr>
<tr><td>0x01</td><td>+5.5</td><td>0x0F</td><td>-6</td><td>0x1D</td><td>-46</td></tr>
<tr><td>0x02</td><td>+5</td><td>0x10</td><td>-8</td><td>0x1E</td><td>-50</td></tr>
<tr><td>0x03</td><td>+4.5</td><td>0x11</td><td>-10</td><td>0x1F</td><td>-54</td></tr>
<tr><td>0x04</td><td>+4</td><td>0x12</td><td>-12</td><td>0x20</td><td>-58</td></tr>
<tr><td>0x05</td><td>+3.5</td><td>0x13</td><td>-14</td><td>0x21</td><td>-62</td></tr>
<tr><td>0x06</td><td>+3</td><td>0x14</td><td>-16</td><td>0x22</td><td>-66</td></tr>
<tr><td>0x07</td><td>+2</td><td>0x15</td><td>-18</td><td>0x23</td><td>-70</td></tr>
<tr><td>0x08</td><td>+1</td><td>0x16</td><td>-20</td><td>0x24</td><td>-74</td></tr>
<tr><td>0x09</td><td>0</td><td>0x17</td><td>-22</td><td>0x25</td><td>-78</td></tr>
<tr><td>0x0A</td><td>-1</td><td>0x18</td><td>-26</td><td>0x26</td><td>-82</td></tr>
<tr><td>0x0B</td><td>-2</td><td>0x19</td><td>-30</td><td>0x27</td><td>-84</td></tr>
<tr><td>0x0C</td><td>-3</td><td>0x1A</td><td>-34</td><td rowspan="2">0x28 to 0x3F</td><td rowspan="2">MUTE</td></tr>
<tr><td>0x0D</td><td>-4</td><td>0x1B</td><td>-38</td></tr>
<tr><td colspan="6">Note: Gain settings apply when the headphone amplifier is configured in differential mode. In the single-ended and capacitorless modes, the actual gain is 5dB lower for each setting.</td></tr>
</table>

麦克风输入

MAX9867提供了两路差分麦克风输入以及用于麦克风供电的低噪声麦克风偏置。典型应用中，左声道麦克风用于记录语音信号，右声道麦克风用于记录背景噪声信号。对于那些仅需要一个麦克风的应用，只使用左声道麦克风输入，并且禁止右声道ADC。麦克风信号经过两级增益放大，送入ADC。第一级提供可选择的0dB、20dB或30dB设置；第二级为可编程增益放大器(PGA)，从0dB至20dB可调，步长为1dB。PGA提供过零检测功能，使增益变化时的蜂鸣噪声降至最小，麦克风输入结构的详细电路请参考图5，表12所示为麦克风输入寄存器。

表12. 麦克风输入寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Left Microphone Gain	0	PALEN		PGAML					0x12
Right Microphone Gain	0	PAREN		PGAMR					0x13

表12. 麦克风输入寄存器(续)

BITS	FUNCTION			
PALEN/PAREN	**Left/Right Microphone Preamplifier Gain** Enables the microphone circuitry and sets the preamplifier gain. 00 = Disabled 01 = 0dB 10 = +20dB 11 = +30dB			
PGAML/PGAMR	**Left/Right Microphone Programmable Gain Amplifier**			
	SETTING	**GAIN (dB)**	**SETTING**	**GAIN (dB)**
	0x00	+20	0x0B	+9
	0x01	+19	0x0C	+8
	0x02	+18	0x0D	+7
	0x03	+17	0x0E	+6
	0x04	+16	0x0F	+5
	0x05	+15	0x10	+4
	0x06	+14	0x11	+3
	0x07	+13	0x12	+2
	0x08	+12	0x13	+1
	0x09	+10	0x14 to 0x1F	0
	0x0A	+11		

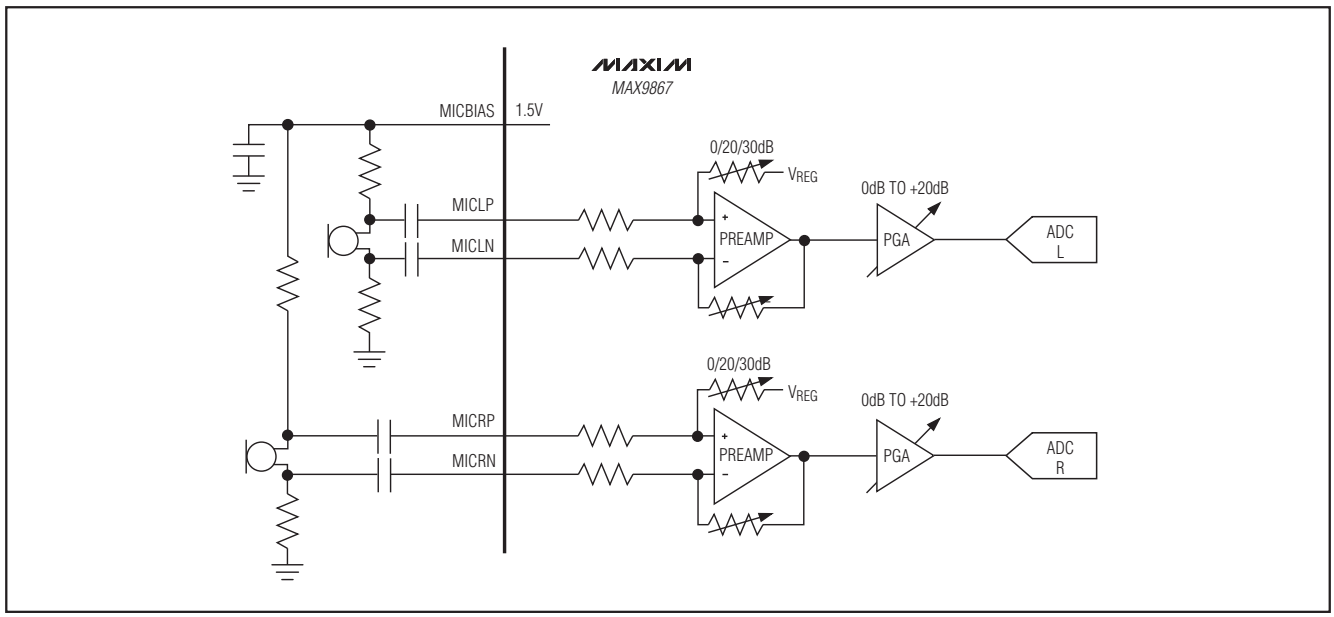


图5. 麦克风输入信号通道

ADC

MAX9867包括两路16位ADC，第一路ADC用来记录左声道麦克风和线入音频信号；第二路ADC用来记录右声道麦克风和线入信号，经过配置也可用于精确测量直流电压。

测量直流电压时，必须通过设置寄存器0x17中的ADLEN和ADREN位使能左、右声道ADC。连接至第二路ADC的输入为JACKSNS/AUX，在AUX (寄存器0x02和0x03)报告输出。由于音频ADC用于执行测量操作，必须正确配置数字音频接口。如果左声道ADC用来转换音频，则以相同采样速率测量直流电压。当不使用左声道ADC时，将数字接口配置为48kHz采样率，以确保最快建立时间。

为确保得到精确的测量结果，MAX9867包含两个校准方案。每次MAX9867上电时校准ADC，且MAX9867处于关断模式时校准设置不会丢失。测量时，将AUXCAP设置为1，以防AUX在读取寄存器时发生变化。

设置步骤

1) 确保提供有效的MCLK信号，并正确配置PSCLK。

2) 选择时钟模式。以下是几种可能的选项：

- **带LRCLK和BCLK信号的从机模式**。测量采样率由外部时钟决定。
- **不带LRCLK和BCLK信号的从机模式**。利用NI比将器件配置在正常时钟模式。设置f_S = 48kHz，允许最快的建立时间。
- **带音频信号的主机模式**。利用NI比将器件配置在正常时钟模式或根据音频信号要求通过FREQ设置为整数模式。
- **不带音频信号的主机模式**。利用NI比将器件配置在正常时钟模式。设置f_S = 48kHz，允许最快的建立时间。

3) 确保JACKSNS禁止。

4) 使能左、右声道ADC；使MAX9867脱离关断模式。

失调校准步骤

MAX9867上电后，在进行首次直流电压测量之前应执行下列步骤：

1) 使能AUX输入(AUXEN = 1)。

2) 使能失调校准(AUXCAL = 1)。

3) 等待适当时间(参见表13)。

4) 完成校准(AUXCAL = 0)。

表13. AUX ADC等待时间

WAIT TIMES	
LRCLK (kHz)	**WAIT TIME (ms)**
48	40
44.1	44
32	60
24	80
22.05	90
16	120
12	160
11.025	175
8	240

增益校准步骤

MAX9867上电之后，进行首次直流电压测量之前或温度变化显著时应执行下列步骤：

1) 使能AUX输入(AUXEN = 1)。

2) 启动增益校准(AUXGAIN = 1)。

3) 等待适当时间(参见表13)。

4) 锁定测量结果(AUXCAP = 1)。

5) 读取AUX值，并将该值保存到存储器，用于后续测量的校准(k = AUX[15:0]，k典型值为19500)。

6) 完成校准(AUXGAIN = AUXCAP = 0)。

直流测量步骤

完成失调和增益校准后，执行下列步骤：

1) 使能AUX输入(AUXEN = 1)。

2) 等待适当时间(参见表13)。

3) 锁定测量结果(AUXCAP = 1)。

4) 读取AUX值，并根据增益校准值进行修正：

$$V_{AUX} = 0.738\left(\frac{AUX[15:0]}{k}\right)$$

5) 完成测量(AUXCAP = 0)。

完整的直流电压测量实例

MCLK = 13MHz、从机模式，BCLK和LRCLK不是由外部提供：

1) 针对f_S = 48kHz配置数字音频接口(PSCLK = 01、FREQ = 0x0、PLL = 0、NI = 0x5ABE、MAS = 0)。
2) 禁止JACKSNS (JDETEN = 0)。
3) 使能左声道和右声道ADC；使MAX9867脱离关断模式(ADLEN = ADREN = $\overline{SHDN}$ = 1)。
4) 失调校准：
   a. 使能AUX输入(AUXEN = 1)。
   b. 使能失调校准(AUXCAL = 1)。
   c. 等待40ms。
   d. 完成校准(AUXCAL = 0)。
5) 校准增益：
   a. 启动增益校准(AUXGAIN = 1)。
   b. 等待40ms。
   c. 锁定测量结果(AUXCAP = 1)。
   d. 读取AUX并将该值保存到存储器，用于后续测量的校准(k = AUX[15:0])。
   e. 完成校准(AUXGAIN = AUXCAP = AUXEN = 0)。
6) 测量JACKSNS/AUX的电压：
   a. 使能AUX输入(AUXEN = 1)。
   b. 等待40ms。
   c. 锁定测量结果(AUXCAP = 1)。
   d. 读取AUX值并根据增益校准值进行修正。
   e. 完成测量(AUXCAP = 0)。
7) 完成直流电压测量。

表14. ADC输入寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
ADC Input	MXINL		MXINR		AUXCAP	AUXGAIN	AUXCAL	AUXEN	0x14

BITS	FUNCTION
MXINL/MXINR	**Left/Right ADC Audio Input Mixer** 00 = No input is selected. 01 = Left/right analog microphone 10 = Left/right line input 11 = Left/right analog microphone + line input **Note:** If the right-line input is disabled, then the left-line input is connected to both mixers. Enabling the left and right digital microphones disables the left and right audio mixers, respectively. See DIGMICL/DIGMICR in Table 15 for more details.
AUXCAP	**Auxiliary Input Capture** 0 = Update AUX with the voltage at JACKSNS/AUX. 1 = Hold AUX for reading.
AUXGAIN	**Auxiliary Input Gain Calibration** 0 = Normal operation 1 = The input buffer is disconnected from JACKSNS/AUX and connected to an internal voltage reference. While in this mode, read the AUX register and store the value. Use the stored value as a gain calibration factor, K, on subsequent readings.
AUXCAL	**Auxiliary Input Offset Calibration** 0 = Normal operation 1 = JACKSNS/AUX is disconnected from the input and the ADC automatically calibrates out any internal offsets.
AUXEN	**Auxiliary Input Enable** 0 = Use JACKSNS/AUX for jack detection. 1 = Use JACKSNS/AUX for DC measurements. **Note:** For AUXEN = 1, set MXINR = 00, ADLEN = 1, and ADREN = 1.

数字麦克风输入

MAX9867能够接受两个数字麦克风的音频信号。采用数字麦克风时，左声道模拟麦克风输入重新配置为数字麦克风输入，右声道模拟麦克风输入可用于模拟和数字麦克风组合，图6所示为数字麦克风接口时序图，参见表15。

表15. 数字麦克风输入寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Microphone	MICCLK		DIGMICL	DIGMICR	0	0	0	0	0x15

BITS	FUNCTION			
MICCLK	**Digital Microphone Clock** 00 = PCLK/8 01 = PCLK/6 10 = Reserved 11 = Reserved			
DIGMICL/DIGMICR	**Digital Left/Right Microphone Enable**			
	DIGMICL	**DIGMICR**	**Left ADC Input**	**Right ADC Input**
	0	0	ADC input mixer	ADC input mixer
	0	1	Line input (left analog microphone unavailable)	Right digital microphone
	1	0	Left digital microphone	ADC input mixer
	1	1	Left digital microphone	Right digital microphone
	Note: The left analog microphone input is never available when DIGMICL or DIGMICR = 1.			

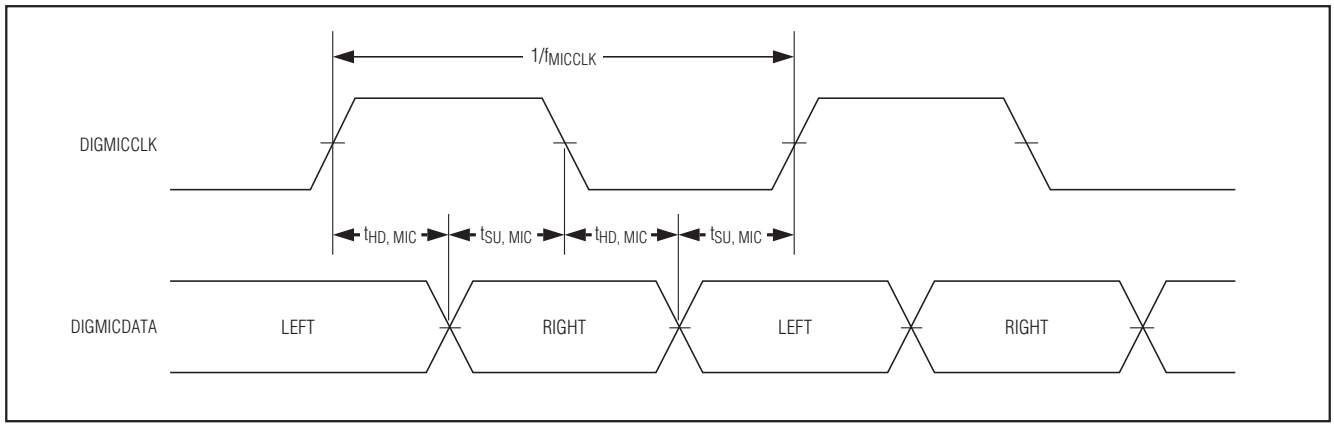


图6. 数字麦克风时序图

模式配置

MAX9867具有噪声抑制电路，能够在音量变化、检测耳机以及配置耳机放大器模式时有效抑制咔嗒/噼噗声。另外，还包括音量摆幅控制和过零检测功能，确保音量变化时消除咔嗒/噼噗声，表16所示为模式配置寄存器。

耳机检测说明

MAX9867具有耳机检测功能，可检测插头的插入、拔出以及负载类型。当检测到有插头插入时，触发$\overline{IRQ}$中断，向微控制器发出事件报警，图7所示为插孔检测的典型配置。

休眠模式下的耳机检测

当MAX9867处于关断状态而保持电源供电时，可使能休眠模式下的耳机检测功能，以检测插孔的插入。休眠模式下，在JACKSNS/AUX和LOUTP施加4µA上拉电流，空载时将JACKSNS/AUX和LOUTP电压拉至AVDD。当有插头插入时，JACKSNS、LOUTP (假定耳机放大器没有配置成单端模式)或二者加载至满负荷，使输出电压几乎降至0V，并分别清除JKSNS或LSNS位。LSNS和JKSNS位的改变将置位JDET，并且，如果IJDET置位将在$\overline{IRQ}$触发一次中断。中断向微控制器报告插孔已插入信号，使微控制器能够进行相应的响应。

上电时的耳机检测

MAX9867处于正常运行状态，并且麦克风接口使能时，可通过JACKSNS/AUX引脚检测插头的插入和拔出。如图7所示，V_{MIC}通过MICBIAS上拉。连接麦克风时，假设V_{MIC}处于0V和$V_{MICBIAS}$的95%之间。如果插头拔出，V_{MIC}增加至$V_{MICBIAS}$。该事件引起JKMIC置位，向系统报告已经拔出耳机。此外，如果插头插入，V_{MIC}降至$V_{MICBIAS}$的95%以下，并清除JKMIC位，报告插头已经插入。可配置JKMIC位产生一个硬件中断，向微控制器报告插头的拔出和插入事件。

耳机模式

耳机放大器支持差分、单端以及无滤波电容输出模式，如图8所示。每种模式下，可将放大器配置为立体声或单声道操作。差分模式和无滤波电容模式内置咔嗒/噼噗声抑制电路；单端模式可选择使用咔嗒/噼噗声抑制功能，以便消除输出耦合电容产生的咔嗒/噼噗声。单端模式下，无需咔嗒/噼噗声抑制功能时可以将LOUTN和ROUTN浮空。

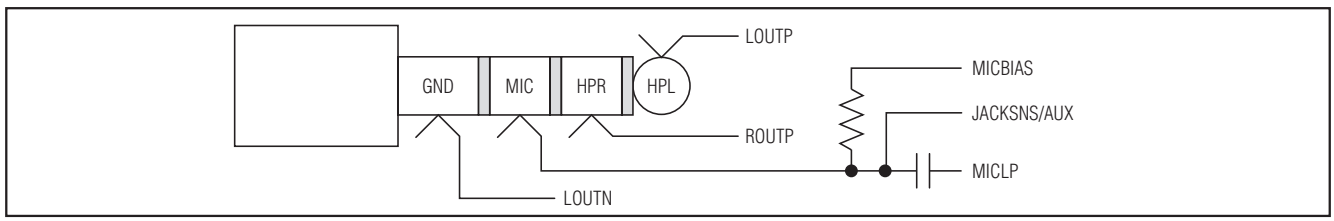


图7. 耳机检测典型配置

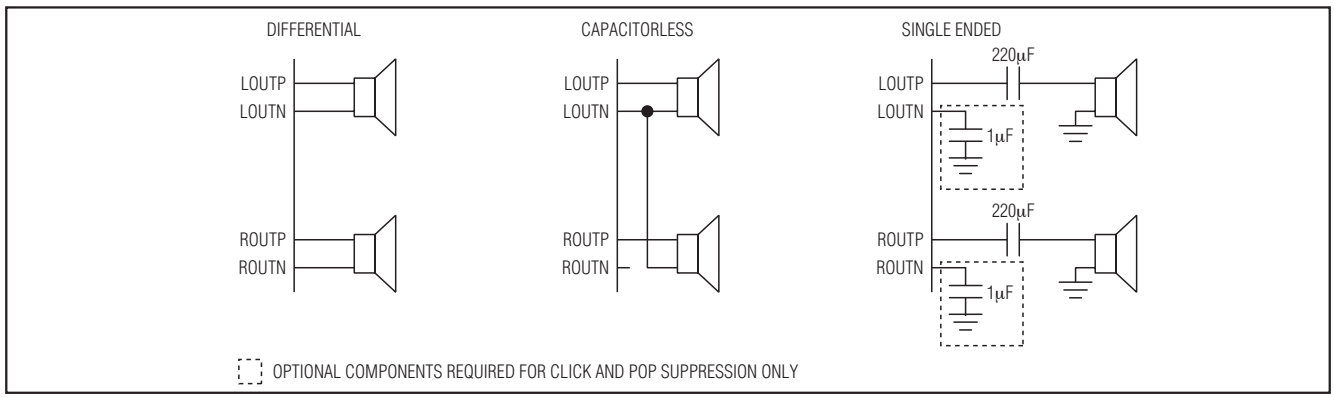


图8. 耳机放大器模式

表16. 模式配置寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Mode	DSLEW	$\overline{VSEN}$	$\overline{ZDEN}$	0	JDETEN	HPMODE			0x16

BITS	FUNCTION
DSLEW	**Digital Volume Slew Speed** 0 = Digital volume changes are slewed over 10ms. 1 = Digital volume changes are slewed over 80ms.
$\overline{VSEN}$	**Volume Change Smoothing** 0 = Volume changes slew through all intermediate values. 1 = Volume changes occur in one step.
$\overline{ZDEN}$	**Line Input Zero-Crossing Detection** 0 = Line input volume changes occur at zero crossings in the audio waveform or after 62ms if no zero crossing occurs. 1 = Line-input volume changes occur immediately.
JDETEN	**Jack Detection Enable** **$\overline{SHDN}$ = 0: Sleep Mode** Enables pullups on LOUTP and JACKSNS/AUX to detect jack insertion. LSNS and JKSNS are valid. LOUTP detection is only valid in differential and capacitorless output modes. **$\overline{SHDN}$ = 1: Normal Mode** Enables the comparator circuitry on JACKSNS/AUX to detect voltage changes. JKMIC is valid if the microphone circuitry is enabled. **Note:** AUXEN must be set to 0 for jack detection to function.
HPMODE	**Headphone Amplifier Mode**

HPMODE	Mode
000	Stereo differential (clickless)
001	Mono (left) differential (clickless)
010	Stereo capacitorless (clickless)
011	Mono (left) capacitorless (clickless)
100	Stereo single-ended (clickless)
101	Mono (left) single-ended (clickless)
110	Stereo single-ended (fast turn-on)
111	Mono (left) single-ended (fast turn-on)

Note: In mono operation, the right amplifier is disabled.

电源管理

MAX9867具有完整的电源管理控制功能，可最大程度地降低功耗。可以分别使能DAC和两个ADC，只有需要的电路处于工作状态。配置改变时触发$\overline{SHDN}$位，表17所示为电源管理寄存器。

表17. 电源管理寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
System Shutdown	$\overline{SHDN}$	LNLEN	LNREN	0	DALEN	DAREN	ADLEN	ADREN	0x17

BITS	FUNCTION
$\overline{SHDN}$	**Shutdown** Places the device in low-power shutdown mode.
LNLEN	**Left-Line Input Enable** Enables the left-line input preamp and automatically enables the left and right headphone amplifiers. If LNREN = 0, the left-line input signal is also routed to the right ADC input mixer and right headphone amplifier. **Note:** Control of the right headphone amplifier can be overridden by HPMODE.
LNREN	**Right-Line Input Enable** Enables the right-line input preamp and automatically enables the right headphone amplifier. **Note:** Control of the right headphone amplifier can be overridden by HPMODE.
DALEN	**Left DAC Enable** Enables the left DAC and automatically enables the left and right headphone amplifiers. If DAREN = 0, the left DAC signal is also routed to the right headphone amplifier. **Note:** Control of the right headphone amplifier can be overridden by HPMODE.
DAREN	**Right DAC Enable** Enabling the right DAC must be done in the same I²C write operation that enables the left DAC. Right DAC operation requires DALEN = 1.
ADLEN	**Left ADC Enable**
ADREN	**Right ADC Enable** Enabling the right ADC must be done in the same I²C write operation that enables the left ADC. The right ADC can be enabled while the left ADC is running if used for DC measurements. $\overline{SHDN}$ must be toggled to disable the right ADC in this case. Right ADC operation requires ADLEN = 1.

版本编码

MAX9867带有一个修订编码，便于识别器件版本。当前版本的编码为0x42，表18所示为版本编码寄存器。

表18. 版本编码寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Revision	REV								0xFF

超低功耗、立体声音频编解码器

I²C串行接口

MAX9867采用I²C/SMBus兼容的2线串行接口，包括一条串行数据线(SDA)和一条串行时钟线(SCL)。SDA和SCL的时钟速率高达400kHz，方便了MAX9867和主机之间的通信。图9所示为2线接口的时序图。主机在总线上产生SCL并启动数据传输。主机发送相应的从地址、寄存器地址，然后发送数据字，向MAX9867写入数据。每次传输由START (S)或REPEATED START (Sr)条件和STOP (P)条件构成帧。发送至MAX9867的每个字长为8位，随后是应答时钟脉冲。主机从MAX9867读取数据时，发送相应的从地址，随后为9个SCL脉冲。MAX9867通过SDA发送数据，与主机产生的SCL脉冲同步。主机在收到每个字节的数据后对其进行应答。每次读操作由START或REPEATED START条件、非应答和STOP条件构成帧。SDA既是输入又是开漏输出，SDA需要一个上拉电阻，通常大于500Ω。SCL仅作为输入。如果总线上有多个主机，或单主机具有开漏SCL输出，SCL则需要连接上拉电阻，通常大于500Ω。SDA和SCL线上的串联电阻可选。串联电阻用于保护MAX9867的数字输入免受总线高压毛刺的影响，并最大程度地降低总线信号的串扰和下冲。

位传输

每个SCL周期传输一个数据位。在SCL脉冲的高电平期间，SDA数据必须保持稳定。SCL为高电平时，SDA的变化表示控制信号(请参见*START和STOP条件*部分)。

START和STOP条件

总线空闲时，SDA和SCL的空闲状态为高电平。主机通过发送START条件启动通信，START条件是SCL为高电平时，SDA由高电平到低电平的跳变；STOP条件是SCL为高电平时，SDA由低电平到高电平的跳变(图10)。来自主机的START条件通知MAX9867开始传输，主机通过发送STOP条件终止传输并释放总线。如果产生REPEATED START条件而非STOP条件，总线将保持有效。

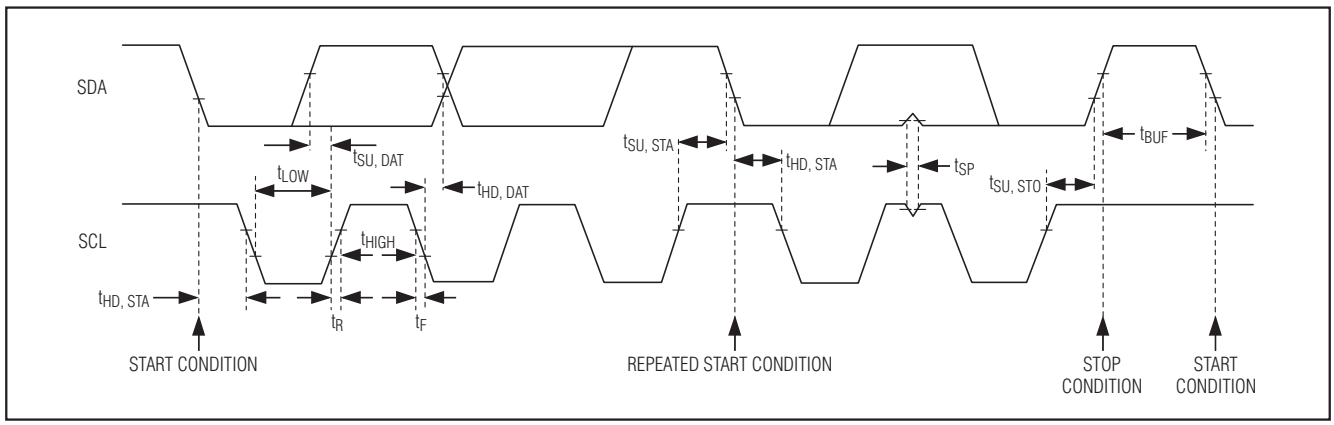


图9. 2线接口时序图

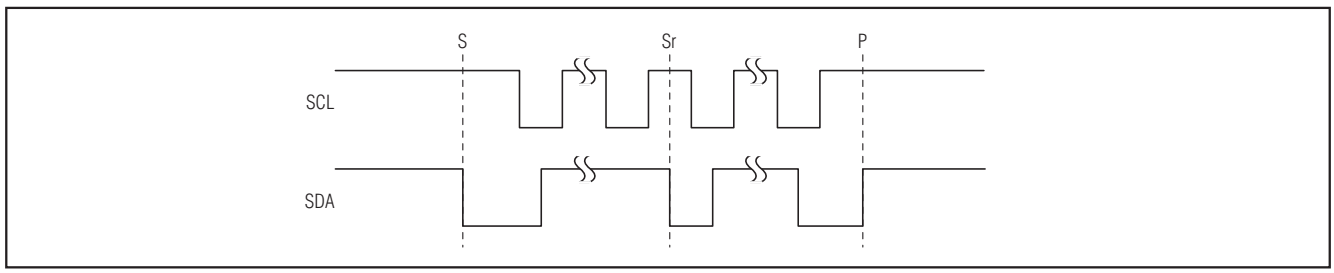


图10. START、STOP和REPEATED START条件

提前STOP条件

MAX9867在数据传输期间可随时识别STOP条件，除非STOP条件与START条件出现在同一高电平脉冲。为了正常工作，请勿在与START条件相同的SCL高电平脉冲期间发送STOP条件。

从地址

从地址定义为7个最高位(MSB)，随后为读/写控制位。对于MAX9867，7个最高有效位是0011000。将读/写控制位置1(从地址 = 0x31)，使MAX9867配置为读模式；将读/写控制位置0 (从地址 = 0x30)使MAX9867配置为写模式。该地址是在START条件后发送到MAX9867的第一个字节信息。

应答

写模式下，应答位(ACK)是第9个时钟位，是MAX9867对每次接收到的数据字节的握手信号(见图11)。如果成功收到数据字节，MAX9867将在主机产生的第9个时钟脉冲期间拉低SDA。监测ACK可以检测失败的数据传输。如果接收器件忙或系统发生故障，则会出现失败的数据传输。若数据传输失败，总线主机会重试通信。当MAX9867处于读模式时，主机将在第9个时钟脉冲拉低SDA，应答数据的接收。每次读取数据字节后，主机均发送应答信号，继续传输数据。当主机从MAX9867读取最后一个数据字节后，将发送非应答位，随后是STOP条件。

写数据格式

对MAX9867的写操作包括START条件、从机地址和R/$\overline{W}$位(置0)、用来配置内部寄存器地址指针的1个数据字节、1个或多个数据字节和STOP条件。图12所示为向MAX9867写入1个字节数据时的正确帧格式；图13所示为向MAX9867写入n个字节数据时的正确帧格式。

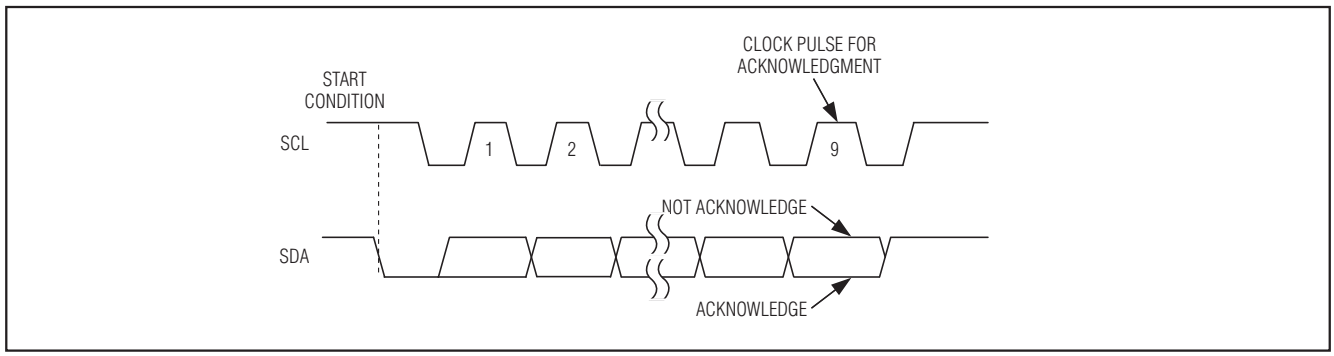


图11. 应答

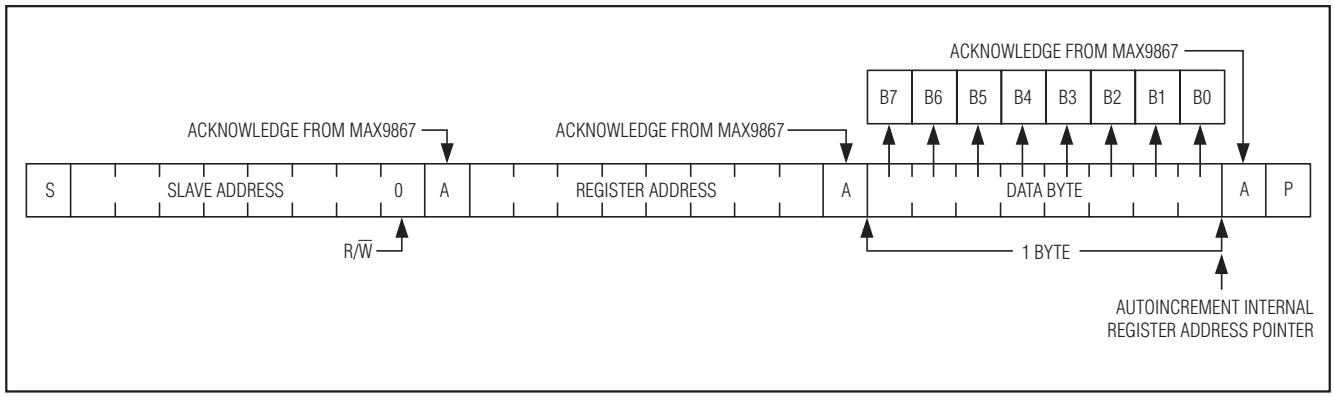


图12. 向MAX9867写入1个数据字节

R/$\overline{W}$位被设置为0的从地址表示主机要向MAX9867写数据。MAX9867在主机产生的第9个SCL脉冲期间应答接收到的地址。

从主机发送的第二字节配置MAX9867的内部寄存器地址指针。指针通知MAX9867写入下一个字节的位置。MAX9867在接收到地址指针数据后发送应答脉冲。

发送到MAX9867的第三字节为写入指定寄存器的数据。MAX9867发送应答脉冲表示接收到数据字节。每次接收数据之后，地址指针自动递增至下一个寄存器地址。自动递增功能使主机能够在一个连续帧内连续地进行寄存器写操作。图13所示给出了在一个帧内写入多个寄存器的时序。主机通过发送STOP条件终止传输。大于0x17的寄存器地址被保留，不要对这些地址进行写操作。

读数据格式

通过发送从地址并将R/$\overline{W}$位置1，启动读操作。MAX9867在第9个SCL时钟脉冲期间拉低SDA，应答接收到的从地址。START条件之后为读命令，将地址指针复位到寄存器0x00。

MAX9867发送的第一个字节是寄存器0x00的内容。发送数据在SCL的上升沿有效。地址指针在每次读取数据字节后都自动递增。这种自动递增功能使得在一个连续帧内能够连续读取全部寄存器内容。读数据字节的任意时刻都可发送STOP条件。如果发送STOP条件后跟随了另一个读操作，则读取的第一个字节为寄存器0x00的数据。

发送读命令之前，可将地址指针预置在一个特定寄存器。主机通过首先发送MAX9867从地址，并将R/$\overline{W}$位置0，然后发送寄存器地址来预置地址指针。随后发送REPEATED START条件，然后发送从地址并将R/$\overline{W}$位置1。MAX9867随后发送指定寄存器的内容。发送完第一个字节后，地址指针自动递增。

主机在应答时钟脉冲期间对每次收到的字节进行应答。主机必须应答除最后一个字节之外所有成功接收的字节。收到最后一个字节后，由主机发送非应答信号，然后是STOP条件。图14给出了从MAX9867读取一个字节的帧格式，图15所示为从MAX9867读取多个字节的帧格式。

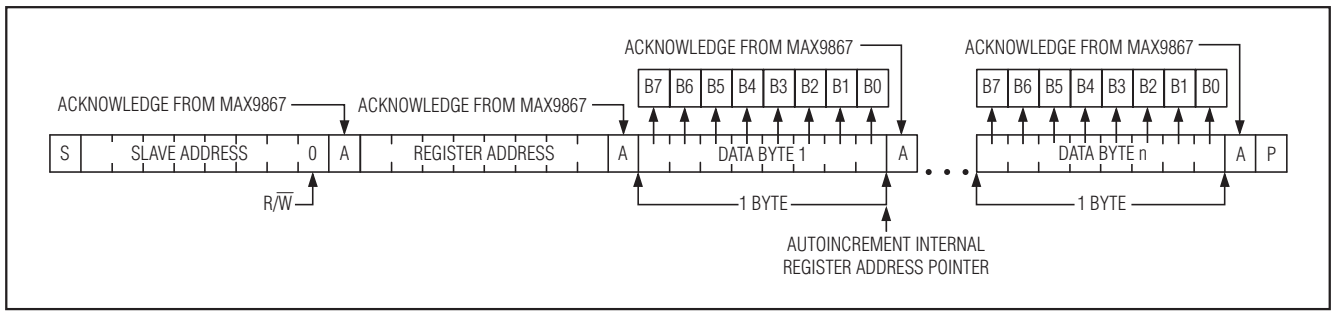


图13. 向MAX9867写入n个字节数据

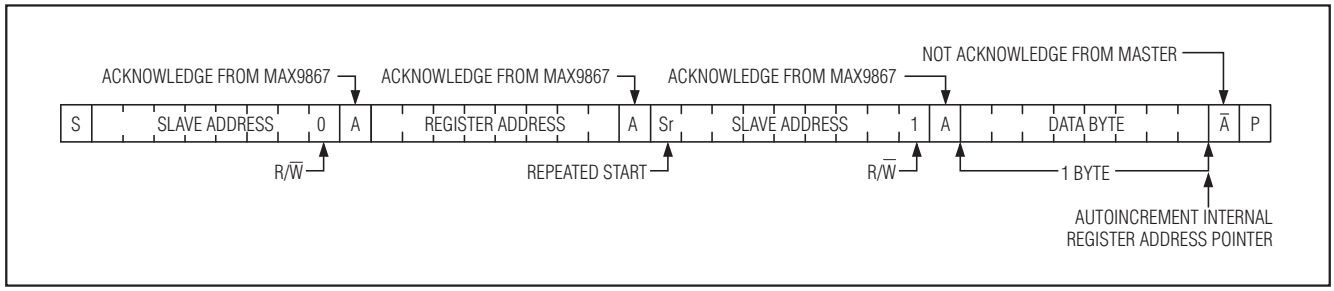


图14. 从MAX9867读取1个字节的数据

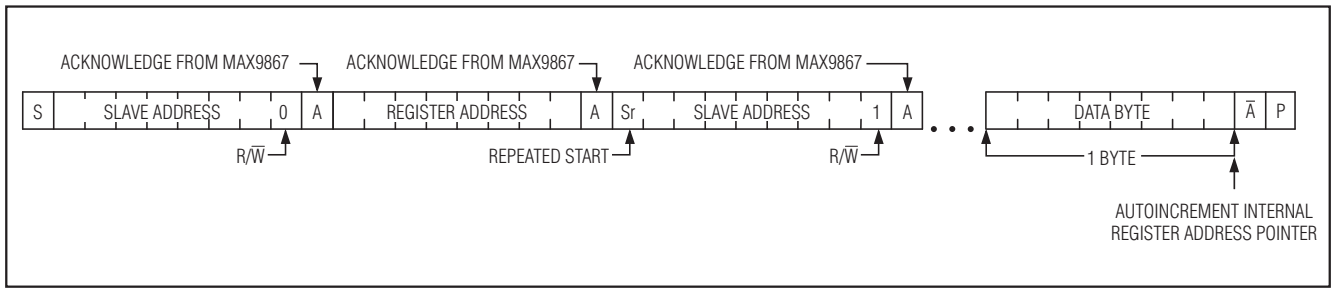


图15. 从MAX9867读取n个字节的数据

应用信息

适当的布局和接地对获得最佳性能至关重要。设计MAX9867 PCB时，需要采用适当的电路隔离，将MAX9867的模拟部分与数字部分分隔开，以保证模拟音频布线不会出现在数字布线附近。

利用PCB的一个专用层布设大面积的连续地层，保持环路面积最小。采用尽可能短的引线将AGND和DGND直接连接至接地面。适当的接地可改善音频性能、最大程度地降低通道间串扰，并可防止数字噪声耦合至模拟音频信号。

通过最短引线将MICBIAS、REG、PREG和REF的旁路电容直接连接至地层。须确保连接至AGND的通路长度最短，将AVDD直接旁路至AGND。

使用连接至DGND的最短通路将所有数字I/O端连接至地平面，将DVDD和DVDDIO直接旁路至DGND。

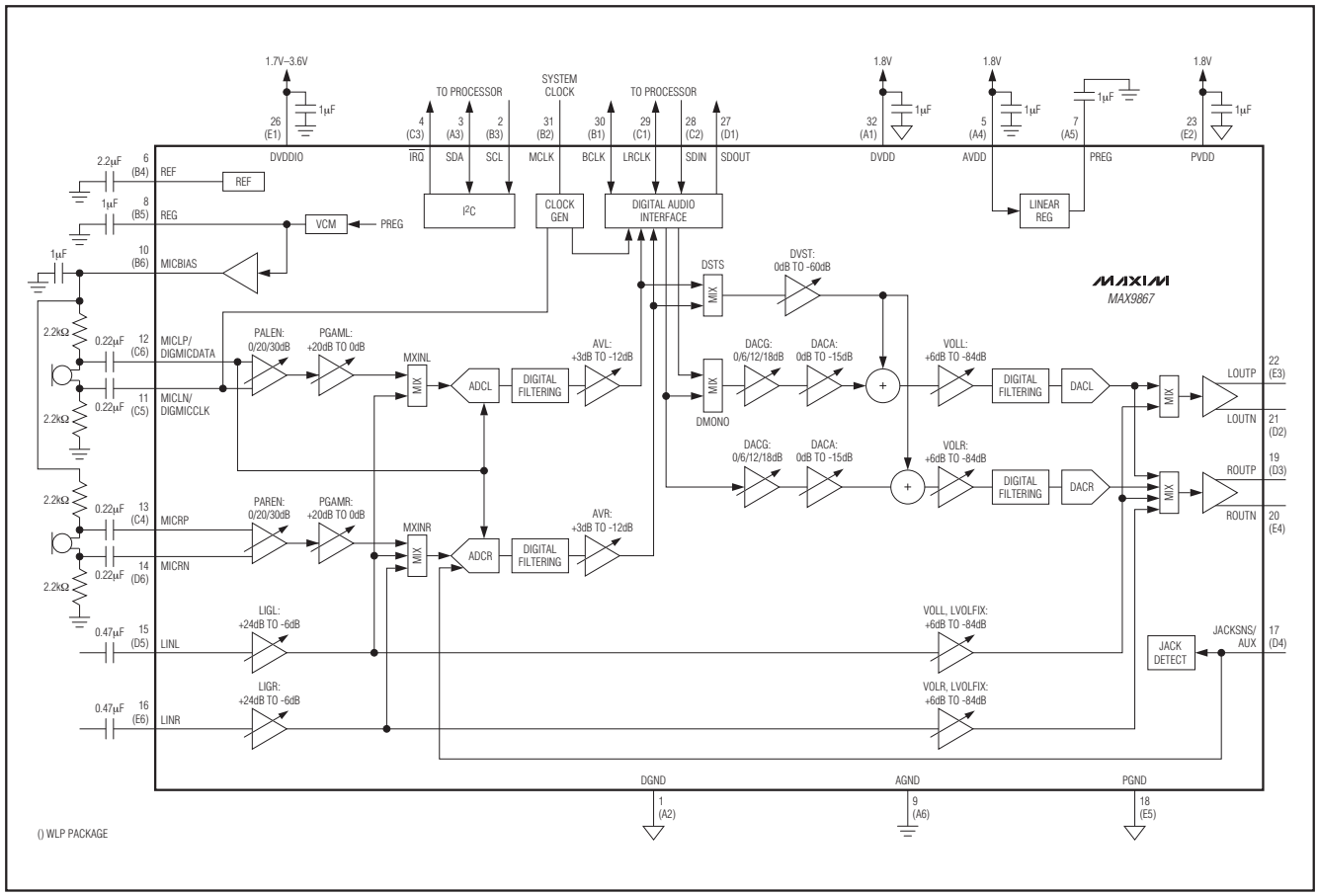
麦克风与MAX9867之间的麦克风信号采用差分方式布线，确保正、负信号尽可能靠近，并具有相同的引线长度。使用单端麦克风或其它单端音频源时，在尽量靠近音频源的位置将麦克风输入负端接地，然后将正端和负端引线作为差分对处理。

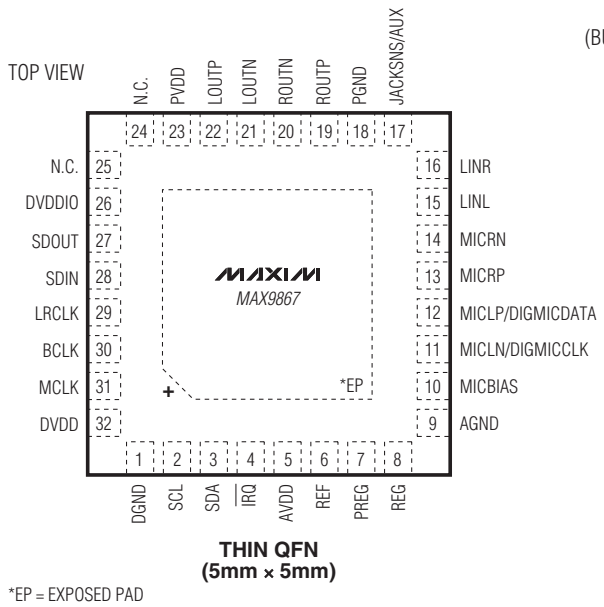
MAX9867 TQFN封装下方有一个裸焊盘，请将该裸焊盘连接到AGND。

提供评估板(EV Kit)，可以作为MAX9867的PCB布局实例。利用该评估板可快速设置MAX9867，并提供易于使用的软件，用于内部寄存器控制。

超低功耗、立体声音频编解码器

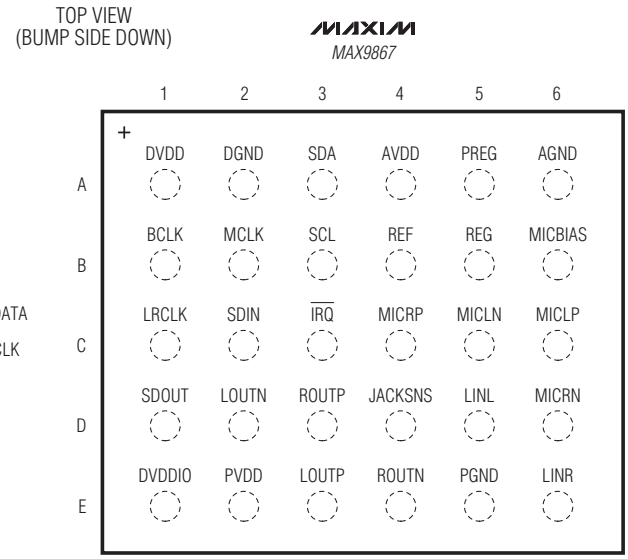
功能框图/典型工作电路





THIN QFN
(5mm × 5mm)

*EP = EXPOSED PAD



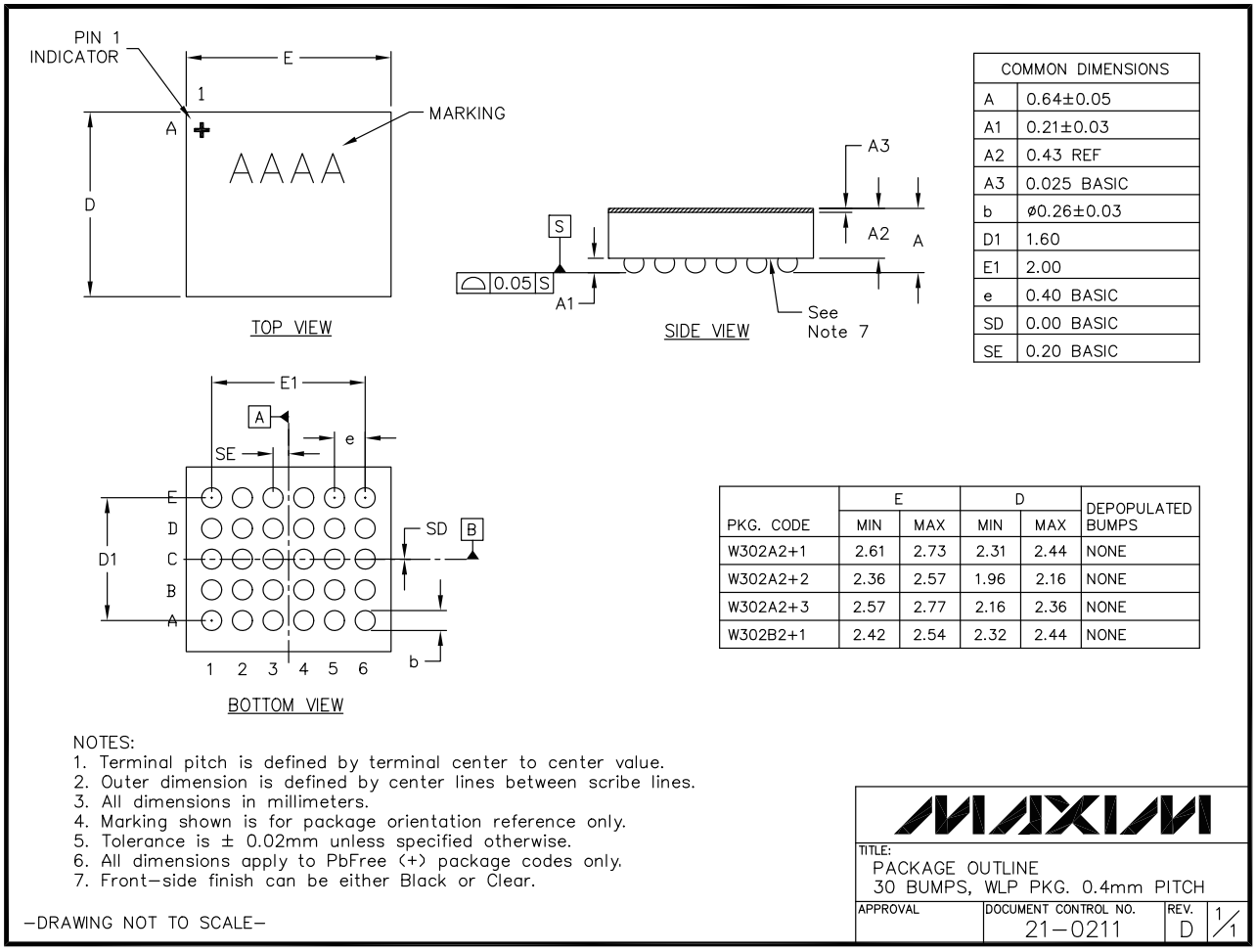
WLP
(2.2mm x 2.7mm)

超低功耗、立体声音频编解码器

封装信息

如需最近的封装外形信息和焊盘布局，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
30 WLP	W302A2+3	21-0211	—
32 TQFN-EP	T3255+4	21-0140	90-0121



COMMON DIMENSIONS	
A	0.64±0.05
A1	0.21±0.03
A2	0.43 REF
A3	0.025 BASIC
b	ø0.26±0.03
D1	1.60
E1	2.00
e	0.40 BASIC
SD	0.00 BASIC
SE	0.20 BASIC

PKG. CODE	E MIN	E MAX	D MIN	D MAX	DEPOPULATED BUMPS
W302A2+1	2.61	2.73	2.31	2.44	NONE
W302A2+2	2.36	2.57	1.96	2.16	NONE
W302A2+3	2.57	2.77	2.16	2.36	NONE
W302B2+1	2.42	2.54	2.32	2.44	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front-side finish can be either Black or Clear.

-DRAWING NOT TO SCALE-

MAXIM

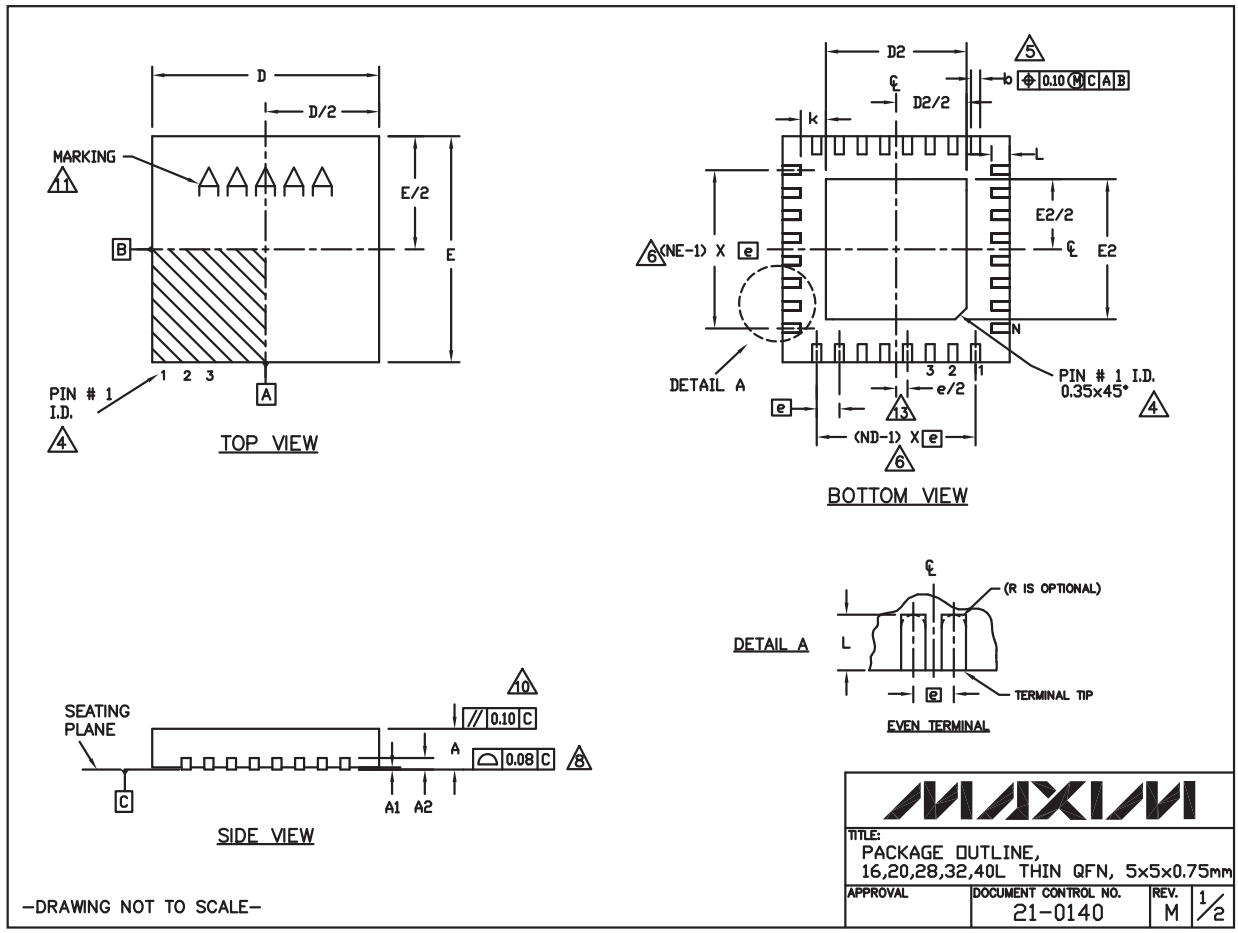
TITLE:
PACKAGE OUTLINE
30 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0211	D	1/1

封装信息(续)

如需最近的封装外形信息和焊盘布局，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

QFN THIN.EPS



封装信息(续)

如需最近的封装外形信息和焊盘布局，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655-4	2.19	2.29	2.39	2.19	2.29	2.39
T165N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055N-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION ‘e’, ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	M	2/2

修订历史

修订号	修订日期	说明	修改页
0	4/09	最初版本。	—
1	5/10	增加了引脚温度及焊接温度信息，更新了V_{OS}指标。	2, 8
2	6/10	更正了*典型工作特性*中图20的错误。	15

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