19-5865; Rev 1; 3/12
备有评估板

MAX98089

低功耗、立体声音频编解码器，集成FlexSound技术

概述

MAX98089功能完备的音频编解码器具有高性能和低功耗优势，理想用于便携式应用。

D类扬声器放大器高效放大两路扬声器信号，低辐射设计允许无滤波器操作。不使用D类放大器时，可选择内部旁路开关将传感器直接连接到外部放大器。

IC提供立体声H类耳机放大器，利用双模电荷泵获得最高效率，此外输出以地为参考的信号，省去了输出耦合电容。

IC还提供单声道差分放大器，可以配置为立体声线出。

器件提供2个差分模拟麦克风输入并支持两个PDM数字麦克风。集成开关允许连接一路额外的麦克风输入，并将麦克风信号连接到外部器件。两路灵活的单端或差分线入可以连接FM收音机或其它信号源。

集成FlexSound™技术，在满足最大失真和输出功率限制的条件下，通过优化信号电平和频率响应改善扩音器性能，防止损坏扬声器。自动增益控制(AGC)和噪声门限设置优化了麦克风输入的信号电平，从而充分利用ADC的动态范围。

器件工作在–40℃至+85℃扩展级温度范围。

FlexSound是Maxim Integrated Products, Inc.的商标。

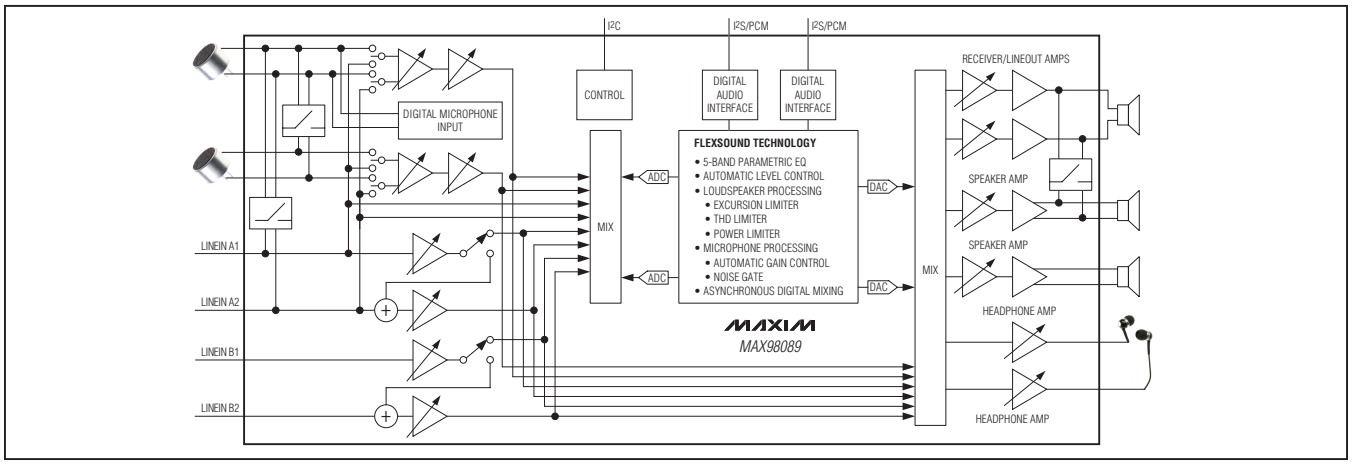
特性

- 5.6mW功耗(DAC至HP，97dB DR)
- 101dB DR立体声DAC (8kHz < f_S < 96kHz)
- 93dB DR立体声ADC (8kHz < f_S < 96kHz)
- 低EMI、立体声D类放大器
  - 1.7W/通道(8Ω，V_{SPK_VDD} = 5.0V)
  - 2.9W/通道(4Ω，V_{SPK_VDD} = 5.0V)
- 高效H类耳机放大器
- 差分接收放大器/立体声线出
- 两路立体声单端线入/单声道差分线入
- 3路差分麦克风输入
- FlexSound技术
  - 5波段参数EQ
  - 自动电平控制(ALC)
  - 失调抑制
  - 扬声器功率限制
  - 扬声器失真抑制
  - 麦克风自动增益控制和噪声门限
- 两路I²S/PCM/TDM数字音频接口
- 异步数字混音
- 支持10MHz至60MHz主时钟频率
- 具有RF抑制的模拟输入和输出
- 全面的咔嗒/噼噗声抑制电路
- 采用63焊球WLP封装(3.80mm x 3.30mm，0.4mm焊球间距)和56引脚TQFN封装(7mm x 7mm x 0.75mm)

定购信息在数据资料的最后给出。

相关型号以及配合该器件使用的推荐产品，请参见：china.maxim-ic.com/MAX98089.related。

简化框图



MAX98089

低功耗、立体声音频编解码器，集成FlexSound技术

目录

概述 1
特性 1
简化框图 1
功能框图 5
Absolute Maximum Ratings 6
Electrical Characteristics 6
Digital Input/Output Characteristics 19
Input Clock Characteristics 21
Audio Interface Timing Characteristics 22
Digital Microphone Timing Characterstics 23
I²C Timing Characteristics 24
功耗 25
典型工作特性 28
- 麦克风至ADC 28
- 线入至ADC 32
- 线入引脚直通ADC 33
- 数字环回 33
- 模拟环回 34
- DAC至接收器 35
- 线入至接收器 37
- DAC至线出 38
- 线入至线出 38
- DAC至扬声器 39
- 线入至扬声器 44
- DAC至耳机 45
- 线入至耳机 52
- 扬声器旁路开关 54

焊球配置 55
焊球/引脚说明 57
详细说明 60
- I²C从地址 61
- 寄存器 61
- 电源管理 67
- 麦克风输入 69
- 线入 71

目录(续)

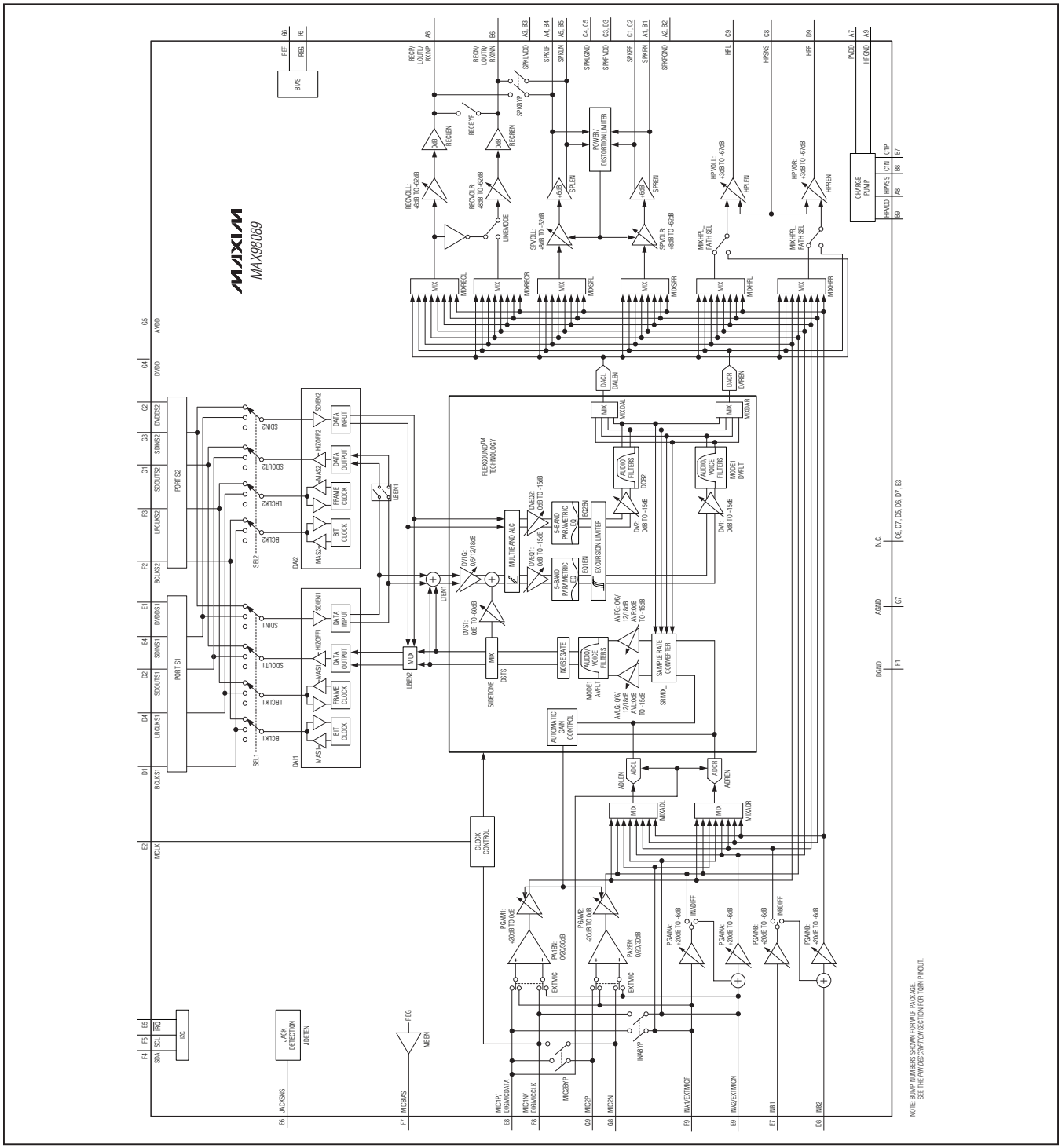
ADC输入混音器 72
录音通路信号处理 73
麦克风AGC 73
噪声门限 73
ADC录音电平控制 76
侧音 77
数字音频接口 78
时钟控制 85
采样率转换器 88
通带滤波 89
回放通路信号处理 92
自动电平控制 92
参数均衡器 93
回放电平控制 95
DAC输入混音器 96
接收放大器 97
接收器输出混音器 98
接收器输出音量 99
扬声器放大器 100
扬声器输出混音器 101
扬声器输出音量 102
扬声器放大器信号处理 102
抑制失调 102
功率抑制器 105
失真抑制 106
耳机 107
DirectDrive耳机放大器 107
电荷泵 107
H类放大器 108
耳机地检测(HPSNS) 108
耳机输出混音器 110
耳机输出音量 111
输出旁路开关 112
咔嗒/噼噗声抑制 113

目录(续)

插孔检测 114
插孔插入检测 114
附件按钮检测 114
插孔拔出检测 114
电池测量 116
器件状态 117
器件版本 118
I²C串行接口 118
位传输 118
START和STOP条件 118
提前STOP条件 118
从地址 119
应答 119
写数据格式 119
读数据格式 120
应用信息 121
典型工作电路 121
无需滤波器的D类放大器 123
RF敏感度 123
启动/关断排序 123
元件选择 124
可选磁珠滤波器 124
输入电容 124
电荷泵电容选择 124
电荷泵飞电容 125
电荷泵保持电容 125
不使用的引脚 125
推荐的PCB布线 126
电源旁路、布局和接地 126
WLP应用信息 127
定购信息 127
封装信息 128
修订历史 131

低功耗、立体声音频编解码器，集成FlexSound技术

功能框图



ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to AGND.)
DVDD, AVDD, PVDD, HPVDD .....-0.3V to +2.2V
SPKLVDD, SPKRVDD, DVDDS1, DVDDS2 .....-0.3V to +6.0V
DGND, HPGND, SPKLGND, SPKRGND .....-0.1V to +0.1V
HPVSS .....(V_{HPGND} - 2.2V) to (V_{HPGND} + 0.3V)
C1N .....(V_{HPVSS} - 0.3V) to (V_{HPGND} + 0.3V)
C1P.....(V_{HPGND} - 0.3V) to (V_{HPVDD} + 0.3V)
REF, MICBIAS .....-0.3V to ($V_{SPKLVDD}$ + 0.3V)
MCLK, SDINS1, SDINS2, JACKSNS,
SDA, SCL, $\overline{IRQ}$ .....-0.3V to +6.0V
LRCLKS1, BCLKS1, SDOUTS1.....-0.3V to (V_{DVDDS1} + 0.3V)
LRCLKS2, BCLKS2, SDOUTS2.....-0.3V to (V_{DVDDS2} + 0.3V)
REG, INA1/EXTMICP, INA2/EXTMICN, INB1, INB2,
MIC1P/DIGMICDATA, MIC1N/DIGMICCLK,
MIC2P, MIC2N.....-0.3V to +2.2V
HPSNS.....(V_{HPGND} - 0.3V) to (V_{HPGND} + 0.3V)
HPL, HPR ..... (V_{HPVSS} - 0.3V) to (V_{HPVDD} + 0.3V)
RECP/LOUTL/RXINP, RECP/LOUTR/
RXINN.....($V_{SPKLGND}$ - 0.3V) to ($V_{SPKLVDD}$ + 0.3V)
SPKLP, SPKLN.....($V_{SPKLGND}$ - 0.3V) to ($V_{SPKLVDD}$ + 0.3V)
SPKRP, SPKRN ..... ($V_{SPKRGND}$ - 0.3V) to ($V_{SPKRVDD}$ + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
63-Bump WLP (derate 25.6mW/°C above +70°C).....2.05W
56-Pin TQFN (derate 40mW/°C above +70°C) 3.2W
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (TQFN only, soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range		Guaranteed by PSRR	$V_{SPKLVDD}$, $V_{SPKRVDD}$	2.8		5.5	V
			V_{DVDD}, V_{AVDD}, V_{PVDD}	1.65	1.8	2	
			V_{DVDDS1}, V_{DVDDS2}	1.65		3.6	
Total Supply Current (Notes 2 and 3)	I_{VDD}	Full-duplex 8kHz mono, receiver output, MAS = 1	Analog		4.5	8	mA
			Speaker		1.6	2.3	
			Digital		1.3	2	
		DAC playback 48kHz stereo, headphone outputs, MAS = 1	Analog		1.9	3	
			Speaker		0.001	0.0058	
			Digital		2.47	3.5	
		DAC playback 48kHz stereo, speaker outputs, MAS = 1	Analog		3.6	6.5	
			Speaker		6.41	8.5	
			Digital		2.49	3.5	
Shutdown Supply Current (Note 2)		T_A = +25°C	Analog		0.2	2	µA
			Speaker		0.01	1	
			Digital		1	5	
REF Voltage					2.5		V
REG Voltage					0.79		V
Shutdown to Full Operation		$\overline{VSEN}$ = 0			30		ms
		$\overline{VSEN}$ = 1			17		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MICROPHONE TO ADC PATH							
Dynamic Range	DR	f_S = 8kHz, MODE = 0 (IIR voice), $AV_{MICPRE\_}$ = 0dB (Note 4)			88		dB
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 0.1V_{P-P}, f_S = 8kHz, f = 1kHz			-78		dB
		$AV_{MICPRE\_}$ = 0dB, V_{IN} = 1V_{P-P}, f = 1kHz			-85		
		$AV_{MICPRE\_}$ = +30dB, V_{IN} = 32mV_{P-P}, f = 1kHz			-71		
Common-Mode Rejection Ratio	CMRR	V_{IN} = 100mV_{P-P}, f = 217Hz			74		dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred, MIC inputs floating		50	62		dB
		f = 217Hz, V_{RIPPLE} = 200mV_{P-P}, input referred			62		
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}, input referred			62		
		f = 10kHz, V_{RIPPLE} = 200mV_{P-P}, input referred			55		
Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from analog input to digital output	MODE = 0 (IIR voice) 8kHz		2.2		ms
			MODE = 0 (IIR voice) 16kHz		1.1		
			MODE = 1 (FIR audio) 8kHz		4.5		
			MODE = 1 (FIR audio) 48kHz		0.76		
MICROPHONE PREAMP							
Full-Scale Input		$AV_{MICPRE\_}$ = 0dB			1.05		V_{P-P}
Preamplifier Gain	$AV_{MICPRE\_}$	(Note 5)	PA1EN/PA2EN = 01		0		dB
			PA1EN/PA2EN = 10	19.5	20	20.5	
			PA1EN/PA2EN = 11	29.5	30	30.5	
PGA Gain	$AV_{MICPGA\_}$	(Note 5)	PGAM1/PGAM2 = 0x00	19	20	21	dB
			PGAM1/PGAM2 = 0x14		0		
MIC Input Resistance	R_{IN_MIC}	All gain settings, measured at MIC1P/MIC1N/MIC2P/MIC2N			50		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MICROPHONE BIAS						
MICBIAS Output Voltage	$V_{MICBIAS}$	I_{LOAD} = 1mA	2.15	2.2	2.25	V
Load Regulation		I_{LOAD} = 1mA to 2mA		0.5	4.5	mV
Line Regulation		$V_{SPKLVDD}$ = 2.8V to 5.5V		110		µV
Ripple Rejection		f = 217Hz, $V_{RIPPLE (SPKLVDD)}$ = 100mV_{P-P}		92		dB
		f = 10kHz, $V_{RIPPLE (SPKLVDD)}$ = 100mV_{P-P}		83		
Noise Voltage		A-weighted, f = 20Hz to 20kHz		3.9		μV_{RMS}
		P-weighted, f = 20Hz to 4kHz		2.1		
		f = 1kHz		50		$nV/\sqrt{Hz}$
MICROPHONE BYPASS SWITCH						
On-Resistance	R_{ON}	$I_{MIC1\_}$ = 100mA, INABYP = MIC2BYP = 1, $V_{MIC2\_}$ = $V_{INA\_}$ = 0V, AVDD, T_A = +25°C		5	30	Ω
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 2V_{P-P}, V_{CM} = 0.9V, R_L = 10kΩ, f = 1kHz, INABYP = MIC2BYP = 1		-80		dB
Off-Isolation		V_{IN} = 2V_{P-P}, V_{CM} = 0.9V, R_L = 10kΩ, f = 1kHz		60		dB
Off-Leakage Current		$V_{MIC1\_}$ = [0V, AVDD], $V_{MIC2\_}/V_{INA\_}$ = [AVDD, 0V]	-1		+1	µA
LINE INPUT TO ADC PATH						
Dynamic Range (Note 4)	DR	INA pin direct, f_S = 48kHz, MODE = 1 (FIR audio)		93		dB
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 1V_{P-P}, f = 1kHz		-82	-74	dB
Gain Error		DC accuracy		1		%
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred, line inputs floating, T_A = +25°C	57	68		dB
		f = 217Hz, V_{RIPPLE} = 200mV_{P-P}, AV_{ADC} = 0dB, input referred		63		
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}, AV_{ADC} = 0dB, input referred		63		
		f = 10kHz, V_{RIPPLE} = 200mV_{P-P}, AV_{ADC} = 0dB, input referred		57		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINE INPUT PREAMP							
Full-Scale Input	V_{IN}	$AV_{PGAIN\_}$ = 0dB			1		V_{P-P}
		$AV_{PGAIN\_}$ = -6dB			1.4		
Level Adjust Gain	$AV_{PGAIN\_}$	T_A = +25°C (Note 5)	PGAINA/PGAINB = 0x0	19	20	21	dB
			PGAINA/PGAINB = 0x1	13	14	15	
			PGAINA/PGAINB = 0x2	2	3	4	
			PGAINA/PGAINB = 0x3		0		
			PGAINA/PGAINB = 0x4	-4	-3	-2	
			PGAINA/PGAINB = 0x5, 0x6, 0x7	-7	-6	-5	
Input Resistance	R_{IN}	$AV_{PGAIN\_}$ = +20dB		14.5	21	28	kΩ
		$AV_{PGAIN\_}$ = +14dB			20		
		$AV_{PGAIN\_}$ = +3dB			20		
		$AV_{PGAIN\_}$ = 0dB		7.5	10	14	
		$AV_{PGAIN\_}$ = -3dB			20		
		$AV_{PGAIN\_}$ = -6dB			20		
Feedback Resistance	R_{IN_FB}	INAEXT/INBEXT = 1	T_A = +25°C	18	20	22	kΩ
			T_A = T_{MIN} to T_{MAX}	16		24	
ADC LEVEL CONTROL							
ADC Level Adjust Range	AV_{ADCLVL}	AVL/AVR = 0xF to 0x0 (Note 5)		-12		+3	dB
ADC Level Step Size					1		dB
ADC Gain Adjust Range	$AV_{ADCGAIN}$	AVLG/AVRG = 00 to 11 (Note 5)		0		18	dB
ADC Gain Adjust Step Size					6		dB
ADC DIGITAL FILTERS							
VOICE MODE IIR LOWPASS FILTER (MODE1 = 0)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff		0.441 x fs			Hz
		-3dB cutoff		0.449 x fs			
Passband Ripple		f < f_{PLP}		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}					0.47 x f_S	Hz
Stopband Attenuation (Note 6)		f > f_{SLP}		74			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOICE MODE IIR HIGHPASS FILTER (MODE1 = 0)						
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1 (Elliptical tuned for f_S = 16kHz + 217Hz notch)			0.0161 x f_S	Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)			0.0319 x f_S	
		AVFLT = 0x3 (Elliptical tuned for f_S = 8kHz + 217Hz notch)			0.0321 x f_S	
		AVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)			0.0632 x f_S	
		AVFLT = 0x5 (f_S/240 Butterworth)			0.0043 x f_S	
Stopband Cutoff (-30dB from Peak)	f_{AHPSB}	AVFLT = 0x1 (Elliptical tuned for f_S = 16kHz + 217Hz notch)	0.0139 x f_S			Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)	0.0156 x f_S			
		AVFLT = 0x3 (Elliptical tuned for f_S = 8kHz + 217Hz notch)	0.0279 x f_S			
		AVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)	0.0312 x f_S			
		AVFLT = 0x5 (f_S/240 Butterworth)	0.0018 x f_S			
DC Attenuation	DC_{ATTEN}	AVFLT ≠ 000		90		dB
STEREO AUDIO MODE FIR LOWPASS FILTER (MODE1 = 1, DHF1 = 0, LRCLK < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.48 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation (Note 6)		f < f_{SLP}	60			dB
ADC STEREO AUDIO MODE FIR LOWPASS FILTER (MODE1 = 1, DHF1 = 1, LRCLK > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.208 x f_S			Hz
		-3dB cutoff	0.28 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.417 x f_S	Hz
Stopband Attenuation		f < f_{SLP}	60			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEREO AUDIO MODE DC BLOCKING HIGHPASS FILTER (MODE1 = 1)							
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT ≠ 000				0.000125 x f_S	Hz
DC Attenuation	DC_{Atten}	AVFLT ≠ 000			90		dB
MICROPHONE AUTOMATIC GAIN CONTROL							
AGC Hold Duration		AGCHLD = 01			50		ms
		AGCHLD = 11			400		
AGC Attack Time		AGCATK = 00			2		ms
		AGCATK = 11			123		
AGC Release Time		AGCRLS = 000			0.078		s
		AGCRLS = 111			10		
AGC Threshold Level		AGCTH = 0x0 to 0xF		-3		+18	dB
AGC Threshold Step Size					1		dB
AGC Gain		(Note 5)		0		20	dB
ADC NOISE GATE							
NG Threshold Level		ANTH = 0x3 to 0xF, referred to 0dBFS		-64		-16	dB
NG Attenuation		(Note 5)		0		12	dB
ADC-TO-DAC DIGITAL SIDETONE (MODE = 0)							
Sidetone Gain Adjust Range	AV_{STGA}	DVST = 0x01			-0.5		dB
		DVST = 0x1F			-60.5		
Sidetone Gain Adjust Step Size					2		dB
Sidetone Path Phase Delay		1kHz, 0dB input, highpass filter disabled	8kHz		2.2		ms
			16kHz		1.1		
ADC-TO-DAC DIGITAL LOOP-THROUGH PATH							
Dynamic Range (Note 4)	DR	f_S = 48kHz, MCLK = 12.288MHz, MODE = 1 (FIR audio), MIC to HP output, T_A = +25°C		83	93		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, f_S = 48kHz, MCLK = 12.288MHz, MODE = 1 (FIR audio), MIC to HP output			81		dB
DAC LEVEL CONTROL							
DAC Attenuation Range	$AV_{DACATTN}$	DV_ = 0xF to 0x0 (Note 5)		-15		0	dB
DAC Attenuation Step Size					1		dB
DAC Gain Adjust Range	$AV_{DACGAIN}$	DV1G = 00 to 11 (Note 5)		0		18	dB
DAC Gain Adjust Step Size					6		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC DIGITAL FILTERS						
VOICE MODE IIR LOWPASS FILTER (MODE1 = 0)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.448 x f_S			Hz
		-3dB cutoff	0.451 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.476 x f_S	Hz
Stopband Attenuation (Note 6)		f > f_{SLP}	75			dB
VOICE MODE IIR HIGHPASS FILTER (MODE1 = 0)						
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT = 0x1 (Elliptical tuned for f_S = 16kHz + 217Hz notch)			0.0161 x f_S	Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)			0.0312 x f_S	
		DVFLT = 0x3 (Elliptical tuned for f_S = 8kHz + 217Hz notch)			0.0321 x f_S	
		DVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)			0.0625 x f_S	
		DVFLT = 0x5 (fs/240 Butterworth)			0.0042 x f_S	
Stopband Cutoff (-30dB from Peak)	f_{DHPSB}	DVFLT = 0x1 (Elliptical tuned for f_S = 16kHz + 217Hz notch)	0.0139 x f_S			Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)	0.0156 x f_S			
		DVFLT = 0x3 (Elliptical tuned for f_S = 8kHz + 217Hz notch)	0.0279 x f_S			
		DVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)	0.0312 x f_S			
		DVFLT = 0x5 (f_S/240 Butterworth)	0.0021 x f_S			
DC Attenuation	DC_{ATTEN}	DVFLT ≠ 000		85		dB
STEREO AUDIO MODE FIR LOWPASS FILTER (MODE1 = 1, DHF1/DHF2 = 0, LRCLK < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.47 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation (Note 6)		f > f_{SLP}	60			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STEREO AUDIO MODE FIR LOWPASS FILTER (MODE1 = 1, DHF1/DHF2 = 1 for LRCLK > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.24 x f_S			Hz
		-3dB cutoff	0.31 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.477 x f_S	Hz
Stopband Attenuation (Note 6)		f < f_{SLP}	60			dB
STEREO AUDIO MODE DC BLOCKING HIGHPASS FILTER						
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT ≠ 000 (DAI1), DCB2 = 1 (DAI2)			0.000104 x f_S	Hz
DC Attenuation	DC_{ATTEN}	DVFLT ≠ 000 (DAI1), DCB2 = 1 (DAI2)		90		dB
AUTOMATIC LEVEL CONTROL						
Dual Band Lowpass Corner Frequency		ALCMB = 1		5		kHz
Dual Band Highpass Corner Frequency		ALCMB = 1		5		kHz
Gain Range			0		12	dB
Low-Signal Threshold		ALCTH = 111 to 001	-48		-12	dBFS
Release Time		ALCRLS = 101		0.25		s
		ALCRLS = 000		8		
PARAMETRIC EQUALIZER						
Number of Bands				5		Bands
Per Band Gain Range			-12		+12	dB
Preattenuator Gain Range		(Note 5)	-15		0	dB
Preattenuator Step Size				1		dB
DAC TO RECEIVER AMPLIFIER PATH						
Dynamic Range	DR	f_S = 48kHz, f = 1kHz (Note 4)		96		dB
Output Offset Voltage	V_{OS}	$AV_{REC\_}$ = -62dB, T_A = +25°C, WLP package only		±0.5	±4	mV
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 15mW, R_{REC} = 32Ω		-70	-63	dB
Power-Supply Rejection Ratio	PSRR	$V_{SPKLVDD}$ = 2.8V to 5.5V, T_A = +25°C	64	75		dB
		f = 217Hz, V_{RIPPLE} = 200mV_{P-P}		80		
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}		80		
		f = 10kHz, V_{RIPPLE} = 200mV_{P-P}		77		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, AV_{REC} = 0dB	Into shutdown		-68		dBV
			Out of shutdown		-72		
LINE INPUT TO RECEIVER AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	Referenced to full-scale output level			94		dB
Total Harmonic Distortion + Noise	THD+N				-64		dB
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, AV_{REC} = 0dB	Into shutdown		-51		dBV
			Out of shutdown		-49		
RECEIVER AMPLIFIER							
Output Power	P_{OUT}	R_{REC} = 32Ω, f = 1kHz, THD = 1%			92		mW
Full-Scale Output		(Note 7)			1		V_{RMS}
Volume Control (Note 5)	AV_{REC}	RECVOL = 0x00			-62		dB
		RECVOL = 0x1F			8		
Volume Control Step Size		+8dB to +6dB			0.5		dB
		+6dB to +0dB			1		
		0dB to -14dB			2		
		-14dB to -38dB			3		
		-38dB to -62dB			4		
Mute Attenuation		f = 1kHz			88		dB
Capacitive Drive Capability		No sustained oscillations	R_{REC} = 32Ω		500		pF
			R_{REC} = ∞		100		
DAC TO LINE OUT AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	f_S = 48kHz, f = 1kHz		83	96		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, R_L = 1kΩ			-78	-72	dB
LINE INPUT TO LINE OUT AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	Referenced to full-scale output level			92		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, R_L = 10kΩ			76		dB
Full-Scale Output		(Note 7)			2		V_{P-P}
Mute Attenuation		f = 1kHz			85		dB
Output Offset Voltage	V_{OS}	$AV_{REC\_}$ = -62dB, TQFN package only			±0.5	±4	mV
Capacitive Drive Capability		No sustained oscillations, R_L = 1kΩ			500		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC TO SPEAKER AMPLIFIER PATH							
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 200mW, Z_{SPK} = 8Ω + 68µH			-68		dB
Crosstalk		SPKL to SPKR and SPKR to SPKL, P_{OUT} = 640mW, f = 1kHz			-88		dB
Output Noise					53		µVRMS
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{SPK\_}$ = 0dB	Into shutdown		65		dBV
			Out of shutdown		66		
MIC INPUT TO SPEAKER AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	Referenced to full-scale output level, $AV_{SPK\_}$ = 0dB			82		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 200mW, R_L = 8Ω + 68µH			71		dB
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{SPK\_}$ = 0dB	Into shutdown		55		dBV
			Out of shutdown		52		
SPEAKER AMPLIFIER							
Output Power	P_{OUT}	f = 1kHz, THD = 10%, Z_{SPK} = 4Ω + 33µH	$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 5.0V		2950		mW
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 4.2V		2060		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V		1570		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.0V		1000		
		f = 1kHz, THD = 1%, Z_{SPK} = 4Ω + 33µH	$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 5.0V		2320		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 4.2V		1620		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V		1240		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.0V		785		
		f = 1kHz, THD = 10%, Z_{SPK} = 8Ω + 68µH	$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 5.0V		1730		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 4.2V		1210		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V		930		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.0V		600		
		f = 1kHz, THD = 1%, Z_{SPK} = 8Ω + 68µH	$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 5.0V		1365		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 4.2V		955		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V		735		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.0V		475		
Full-Scale Output		(Note 7)			2		VRMS
Volume Control	$AV_{SPK\_}$	(Note 5)	SPVOLL/SPVOLR = 0x00		-62		dB
			SPVOLL/SPVOLR = 0x1F		+8		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Volume Control Step Size		+8dB to +6dB			0.5		dB
		+6dB to +0dB			1		
		0dB to -14dB			2		
		-14dB to -38dB			3		
		-38dB to -64dB			4		
Mute Attenuation		f = 1kHz			86		dB
Output Offset Voltage	V_{OS}	$AV_{SPK\_}$ = -61dB, T_A = +25°C			±0.5	±3	mV
EXCURSION LIMITER							
Upper Corner Frequency Range		DHPUCF = 001 to 100		400		1000	Hz
Lower Corner Frequency		DHPLCF = 01 to 10			400		Hz
Biquad Minimum Corner Frequency		DHPUCF = 000 (fixed mode)			100		Hz
		DHPUCF = 001			200		
		DHPUCF = 010			300		
		DHPUCF = 011			400		
		DHPUCF = 100			500		
Threshold Voltage		Z_{SPK} = 8Ω + 68µH, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 5.5V, $AV_{SPK\_}$ = 8dB	DHPTH = 000		0.34		V_P
			DHPTH = 111		0.95		
Release Time		ALCRLS = 101			0.25		s
		ALCRLS = 000			4		
POWER LIMITER							
Attenuation					-64		dB
Threshold		Z_{SPK} = 8Ω + 68µH, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 5.5V, $AV_{SPK\_}$ = 8dB	PWRTH = 0x1		0.08		W
			PWRTH = 0xF		1.23		
Time Constant 1	t_{PWR1}	PWRT1 = 0x1			0.5		s
		PWRT1 = 0xF			8.7		
Time Constant 2	t_{PWR2}	PWRT2 = 0x1 to 0xF			0.5		min
		PWRT2 = 0xF			8.7		
Weighting Factor	k_{PWR}	PWRK = 000 to 111		12.5		100	%
DISTORTION LIMITER							
Distortion Limit		THDCLP = 0x1			< 1		%
		THDCLP = 0xF			24		
Release Time Constant		THDT1 = 000			0.76		s
		THDT1 = 111			6.2		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC TO HEADPHONE AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	f_S = 48kHz	Master or slave mode		101		dB
			Slave mode	97			
			Low power mode, T_A = +25°C	95	97		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 20mW	R_{HP} = 16Ω		-84	-64	dB
			R_{HP} = 32Ω		-85		
Crosstalk		HPL to HPR and HPR to HPL, P_{OUT} = 5mW, f = 1kHz, R_{HP} = 32Ω			-92		dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 2.0V		46	54		dB
		f = 217Hz, V_{RIPPLE} = 200mV$_{P-P}$, $AV_{HP\_}$ = 0dB			72		
		f = 1kHz, V_{RIPPLE} = 200mV$_{P-P}$, $AV_{HP\_}$ = 0dB			63		
		f = 10kHz, V_{RIPPLE} = 200mV$_{P-P}$, $AV_{HP\_}$ = 0dB			43		
DAC Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from digital input to analog output	MODE = 0 (voice) 8kHz		2.2		ms
			MODE = 0 (voice) 16kHz		1.1		
			MODE = 1 (music) 8kHz		4.5		
			MODE = 1 (music) 48kHz		0.76		
Gain Error					1	5	%
Channel Gain Mismatch					1		%
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{HP\_}$ = 0dB	Into shutdown		-62		dBV
			Out of shutdown		-63		
LINE INPUT TO HEADPHONE AMPLIFIER PATH							
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 1V$_{P-P}$, f =1kHz, R_{HP} = 32Ω			81		dB
Dynamic Range (Note 4)					92.5		dB
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{HP\_}$ = 0dB	Into shutdown		-62		dBV
			Out of shutdown		-63		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
HEADPHONE AMPLIFIER							
Output Power	P_{OUT}	f = 1kHz, THD = 1%	R_{HP} = 32Ω		30		mW
			R_{HP} = 16Ω		38		
Positive Charge-Pump Output Voltage	HPVDD	$V_{OUT} \le V_{PVDD}$ x 0.2V, R_{HP} = ∞			PVDD/2		V
		$V_{OUT} > V_{PVDD}$ x 0.2V, R_{HP} = ∞			PVDD		
Negative Charge-Pump Output Voltage	HPVSS	$V_{OUT} \le V_{PVDD}$ x 0.2V, R_{HP} = ∞			-PVDD/2		V
		$V_{OUT} > V_{PVDD}$ x 0.2V, R_{HP} = ∞			-PVDD		
Output Voltage Threshold (Output Voltage at which the Charge Pump Switches Modes; VOUT Rising; Transition from Split to Invert Mode)	V_{TH}	RL = ∞			±PVDD x 0.2		V
Full-Scale Output		(Note 7)			1		V_{RMS}
Volume Control	$AV_{HP\_}$	(Note 5)	HPVOL_ = 0x00		-67		dB
			HPVOL_ = 0x1F		+3		
Volume Control Step Size		+3dB to +1dB			0.5		dB
		+1dB to -5dB			1		
		-5dB to -19dB			2		
		-19dB to -43dB			3		
		-43dB to -67dB			4		
Mute Attenuation		f = 1kHz			100		dB
Output Offset Voltage	V_{OS}	$AV_{HP\_}$ = -67dB	T_A = +25°C		±0.1	±1	mV
			T_A = T_{MIN} to T_{MAX}			±3	
Capacitive Drive Capability		No sustained oscillations	R_{HP} = 32Ω		500		pF
			R_{HP} = ∞		100		
SPEAKER BYPASS SWITCH							
On-Resistance	R_{ON}	$I_{SPKL\_}$ = 100mA, SPKBYP = 1, $V_{RXIN\_}$ = [0V, $V_{SPKLVDD}$]			2.8		Ω
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $2V_{P-P}$, V_{CM} = $V_{SPKLVDD}$/2, Z_{SPK} = 8Ω + 68µH, f = 1kHz, SPKBYP = 1	R_S = 10Ω		60		dB
			R_S = 0Ω		60		
Off-Isolation		V_{IN} = $2V_{P-P}$, V_{CM} = $V_{SPKLVDD}$/2, Z_{SPK} = 8Ω + 68µH, f = 1kHz			96		dB
Off-Leakage Current		$V_{RXIN\_}$ = [0V, $V_{SPKLVDD}$], $V_{SPKL\_}$ = [$V_{SPKLVDD}$, 0V]		-20		+20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out loads (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND. R_{LOAD} = R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER BYPASS SWITCH						
On-Resistance	R_{ON}	I_{RECP} = 100mA, RECBYP = 1, V_{RECN} = [0V, $V_{SPKLVDD}$]		2		Ω
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $2V_{P-P}$, V_{CM} = $V_{SPKLVDD}$/2, Z_{SPK} = 8Ω + 68µH, f = 1kHz, RECBYP = 1, R_S = 0Ω		60		%
Off-Isolation		V_{IN} = $2V_{P-P}$, V_{CM} = $V_{SPKLVDD}$/2, Z_{SPK} = 8Ω + 68µH, f = 1kHz		84		dB
Off-Leakage Current		V_{RECP} = [0V, $V_{SPKLVDD}$], V_{RECN} = [$V_{SPKLVDD}$, 0V]	-15		+15	µA
JACK DETECTION						
JACKSNS High Threshold	V_{TH1}	MICBIAS enabled	0.92 x $V_{MICBIAS}$	0.95 x $V_{MICBIAS}$	0.98 x $V_{MICBIAS}$	V
		MICBIAS disabled	0.92 x $V_{SPKLVDD}$	0.95 x $V_{SPKLVDD}$	0.98 x $V_{SPKLVDD}$	
JACKSNS Low Threshold	V_{TH2}	MICBIAS enabled	0.06 x $V_{MICBIAS}$	0.10 x $V_{MICBIAS}$	0.17 x $V_{MICBIAS}$	V
		MICBIAS disabled	0.06 x $V_{SPKLVDD}$	0.10 x $V_{SPKLVDD}$	0.17 x $V_{SPKLVDD}$	
JACKSNS Sense Voltage		MICBIAS disabled, JDWK = 1	3.65	3.7		
JACKSNS Sense Resistance	R_{SENSE}	MICBIAS disabled, JDWK = 0	1.6	2.4	2.9	kΩ
JACKSNS Weak Pullup Current	I_{WPU}	MICBIAS disabled, JDWK = 1	2	5	9.5	µA
JACKSNS Deglitch Period	t_{GLITCH}	JDEB = 00		25		ms
		JDEB = 11		200		
BATTERY ADC						
Input Voltage Range			2.6		5.6	V
LSB Size				0.1		V

DIGITAL INPUT/OUTPUT CHARACTERISTICS

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MCLK						
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}				0.6	V
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 5.5V; T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF

DIGITAL INPUT/OUTPUT CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDINS1, BCLKS1, LRCLKS1—INPUT						
Input High Voltage	V_{IH}		0.7 x DVDDS1			V
Input Low Voltage	V_{IL}				0.29 x DVDDS1	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDS1} = 3.6V, V_{IN} = 0V, 3.6V; T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
BCLKS1, LRCLKS1, SDOUTS1—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDDS1} = 1.65V, I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDDS1} = 1.65V, I_{OH} = 3mA	DVDDS1 - 0.4			V
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 5.5V; T_A = +25°C, high-impedance state	-1		+1	µA
SDINS2, BCLKS2, LRCLKS2—INPUT						
Input High Voltage	V_{IH}		0.7 x DVDDS2			V
Input Low Voltage	V_{IL}				0.29 x DVDDS2	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDS2} = 3.6V, V_{IN} = 0V, 3.6V; T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
BCLKS2, LRCLKS2, SDOUTS2—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDDS2} = 1.65V, I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDDS2} = 1.65V, I_{OH} = 3mA	DVDDS2 - 0.4			V
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 5.5V; T_A = +25°C, high-impedance state	-1		+1	µA
SDA, SCL—INPUT						
Input High Voltage	V_{IH}		0.7 x DVDD			V
Input Low Voltage	V_{IL}				0.3 x DVDD	V
Input Hysteresis				210		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 5.5V; T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
SDA, $\overline{IRQ}$—OUTPUT						
Output High Current	I_{OH}	V_{OUT} = 5.5V, T_A = +25°C			1	mA
Output Low Voltage	V_{OL}	V_{DVDD} = 1.65V, I_{OL} = 3mA			0.2 x DVDD	V

DIGITAL INPUT/OUTPUT CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGMICDATA—INPUT						
Input High Voltage	V_{IH}		0.65 x DVDD			V
Input Low Voltage	V_{IL}				0.35 x DVDD	V
Input Hysteresis				125		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 2.0V; T_A = +25°C	-25		+25	µA
Input Capacitance				10		pF
DIGMICCLK—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDD} = 1.65V, I_{OL} = 1mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDD} = 1.65V, I_{OH} = 1mA	DVDD - 0.4			V

INPUT CLOCK CHARACTERISTICS

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MCLK Input Frequency	f_{MCLK}		10		60	MHz
MCLK Input Duty Cycle		PSCLK = 01	40	50	60	%
		PSCLK = 10 or 11	30		70	
Maximum MCLK Input Jitter				100		ps_{RMS}
LRCLK Sample Rate (Note 8)		DHF_ = 0	8		48	kHz
		DHF_ = 1	48		96	
DAI1 LRCLK Average Frequency Error (Note 9)		FREQ1 = 0x8 to 0xF	0		0	%
		FREQ1 = 0x0	-0.025		+0.025	
DAI2 LRCLK Average Frequency Error (Note 9)			-0.025		+0.025	%
PLL Lock Time		Rapid lock mode		2	7	ms
		Nonrapid lock mode		12	25	
Maximum LRCLK Jitter to Maintain PLL Lock					100	ns
Soft-Start/Stop Time				10		ms

AUDIO INTERFACE TIMING CHARACTERISTICS

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BCLK Cycle Time	t_{BCLK}	Slave mode		90			ns
BCLK High Time	t_{BCLKH}	Slave mode		20			ns
BCLK Low Time	t_{BCLKL}	Slave mode		20			ns
BCLK or LRCLK Rise and Fall Time	t_R, t_F	Master mode, C_L = 15pF			5		ns
SDIN to BCLK Setup Time	t_{SETUP}			20			ns
LRCLK to BCLK Setup Time	$t_{SYNCSET}$	Slave mode		20			ns
SDIN to BCLK Hold Time	t_{HOLD}			20			ns
LRCLK to BCLK Hold Time	$t_{SYNCHOLD}$	Slave mode		20			ns
Minimum Delay Time from LSB BCLK Falling Edge to High-Impedance State	t_{HIZOUT}	Master mode, TDM_ = 1			42		ns
LRCLK Rising Edge to SDOUT MSB Delay	t_{SYNCTX}	C_L = 30pF, TDM_ = 1, FSW_ = 1				50	ns
BCLK to SDOUT Delay	t_{CLKTX}	C_L = 30pF	TDM_ = 1, BCLK rising edge			50	ns
			TDM_ = 0			50	
Delay Time from BCLK to LRCLK	$t_{CLKSYNC}$	Master mode	TDM_ = 1	-15		+15	ns
			TDM_ = 0			0.8 x t_{BCLKL}	
Delay Time from LRCLK to BCLK After LSB	$t_{ENDSYNC}$	Master mode	TDM_ = 1, FSW_ = 1	20			ns

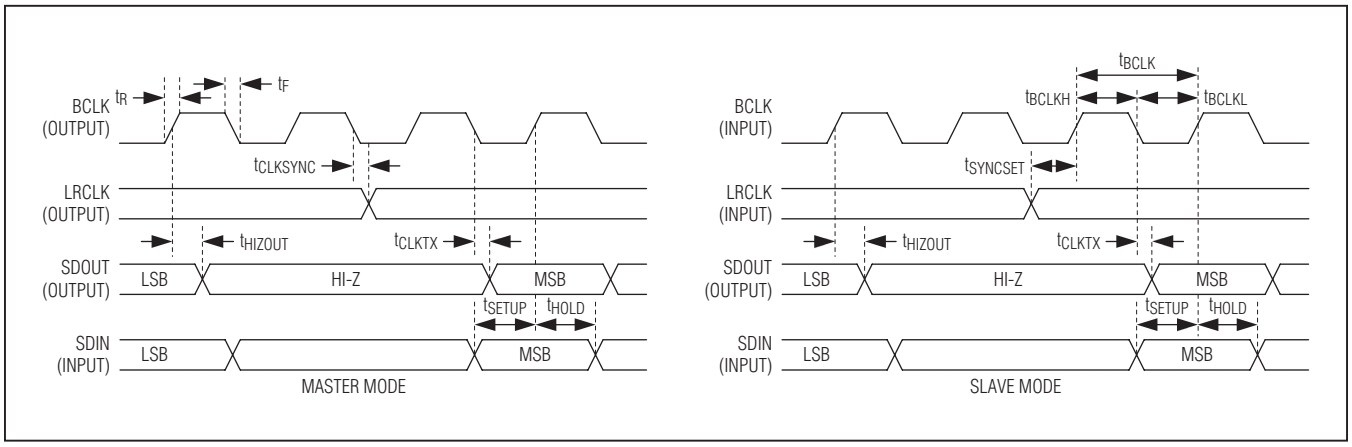


图1. Non–TDM音频接口时序图(TDM_ = 0)

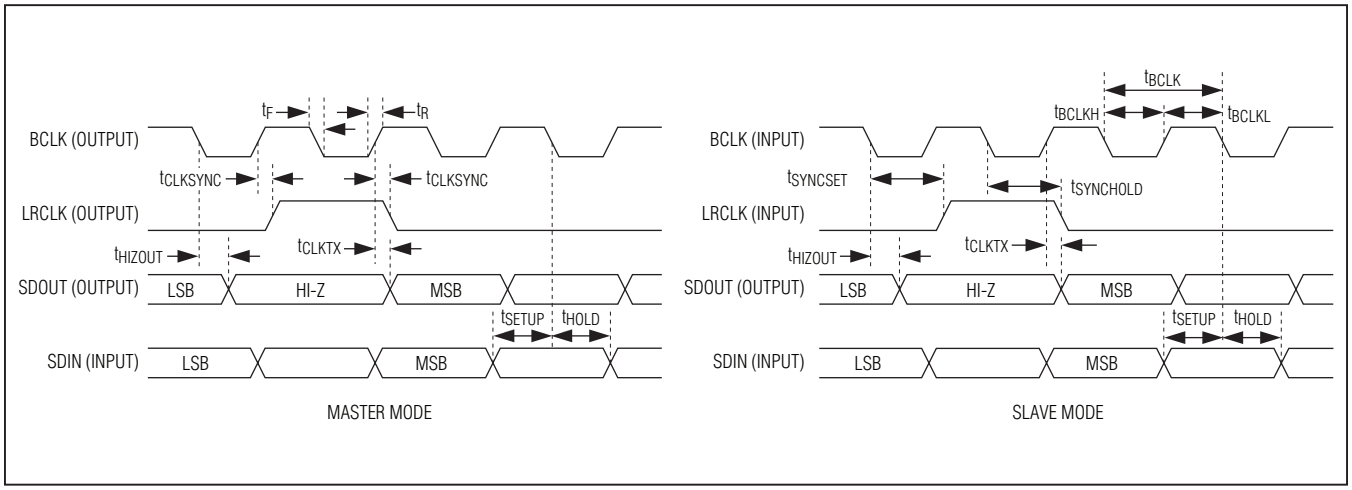


图2. TDM音频接口时序图(TDM_ = 1，FSW_ = 0)

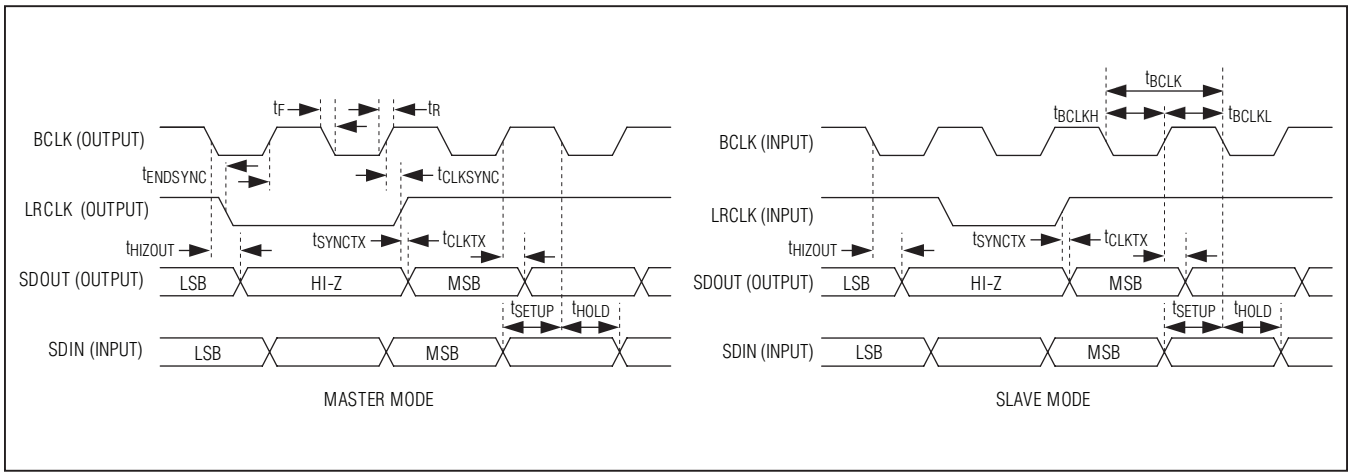


图3. TDM音频接口时序图(TDM_ = 1，FSW_ = 1)

DIGITAL MICROPHONE TIMING CHARACTERSTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGMICCLK Frequency	f_{MICCLK}	MICCLK = 00		PCLK/8		MHz
		MICCLK = 01		PCLK/6		
		MICCLK = 10		64 x f_{LRCLK}		
DIGMICDATA to DIGMICCLK Setup Time	$t_{SU,MIC}$	Either clock edge	20			ns
DIGMICDATA to DIGMICCLK Hold Time	$t_{HD,MIC}$	Either clock edge	0			ns

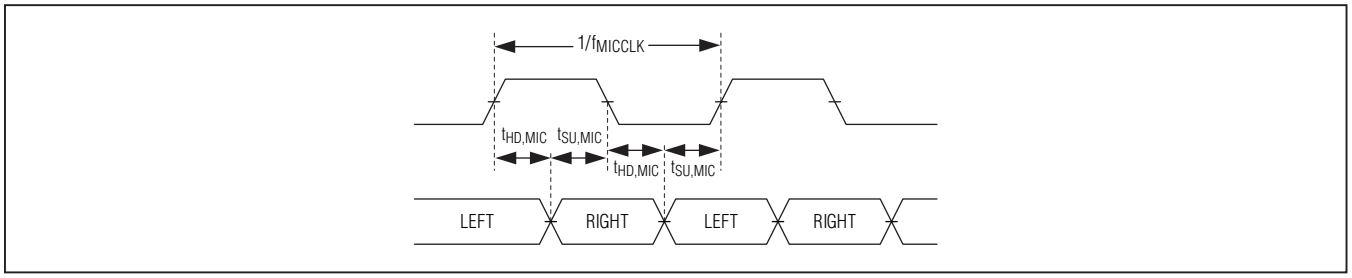


图4. 数字麦克风时序图

I²C TIMING CHARACTERISTICS

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}	Guaranteed by SCL pulse-width low and high	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	R_{PU} = 475Ω, CB = 100pF, 400pF	0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 10)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 10)	20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	R_{PU} = 475Ω, C_B = 100pF, 400pF (Note 10)	20 + 0.05C_B		250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B	Guaranteed by SDA transmitting fall time			400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

I²C TIMING CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

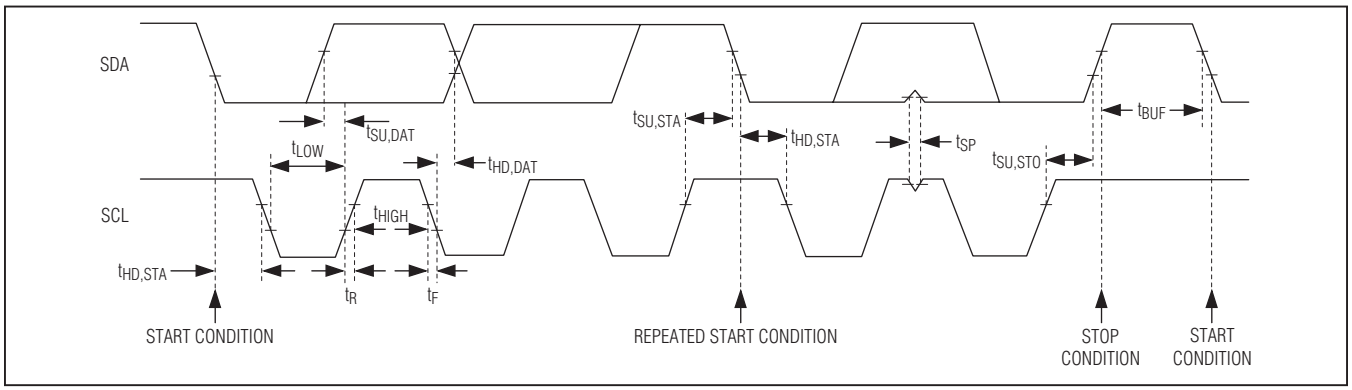


图5. I²C接口时序图

Note 1: The IC is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Analog supply current = I_{AVDD} + I_{HPVDD}. Speaker supply current = $I_{SPKLVDD}$ + $I_{SPKRVDD}$. Digital supply current = I_{DVDD} + I_{DVDDS1} + I_{DVDDS2}.
Note 3: Clocking all zeros into the DAC.
Note 4: Dynamic range measured using the EIAJ method. -60dBFS, 1kHz output signal, A-weighted and normalized to 0dBFS. f = 20Hz to 20kHz.
Note 5: Gain measured relative to the 0dB setting.
Note 6: The filter specification is accurate only for synchronous clocking modes, where NI is a multiple of 0x1000.
Note 7: 0dBFS for DAC input. $1V_{P-P}$ for INA/INB inputs.
Note 8: LRCLK may be any rate in the indicated range. Asynchronous or noninteger MCLK/LRCLK ratios may exhibit some full-scale performance degradation compared to synchronous integer related MCLK/LRCLK ratios.
Note 9: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.
Note 10: C_B is in pF.

功耗

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, MAS = 0.)

MODE	I_{AVDD} (mA)	I_{PVDD} (mA)	I_{SPKVDD} + $I_{SPKLVDD}$ (mA)	I_{DVDD} (mA)	I_{DVDDS1} + I_{DVDDS2} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
Playback to Headphone Only							
DAC Playback 48kHz Stereo HP DAC ➞ HP Low power mode, 24-bit, music filters, 256Fs	**1.25**	**0.47**	**0.00**	**1.35**	**0.01**	**5.55**	**97**
DAC Playback 48kHz Stereo HP DAC ➞ HP Low power mode, 24-bit, music filters, 256Fs, 0.1mW/channel, R_{HP} = 32Ω	**1.25**	**1.81**	**0.00**	**1.56**	**0.01**	**8.32**	**97**

功耗(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, MAS = 0.)

MODE	I_{AVDD} (mA)	I_{PVDD} (mA)	I_{SPKVDD} + $I_{SPKLVDD}$ (mA)	I_{DVDD} (mA)	I_{DVDDS1} + I_{DVDDS2} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
DAC Playback to Headphone							
DAC Playback 48kHz Stereo HP DAC ➞ HP 24-bit, music filters, 256Fs	**2.04**	**1.27**	**0.00**	**1.53**	**0.01**	**8.72**	**101**
DAC Playback 48kHz Stereo HP DAC ➞ HP 24-bit, music filters, 256Fs, 0.1mW/channel, R_{HP} = 32Ω	**2.04**	**2.11**	**0.00**	**1.74**	**0.01**	**10.63**	**101**
DAC Playback 44.1kHz Stereo HP DAC ➞ HP 24-bit, music filters	**2.03**	**1.27**	**0.00**	**1.41**	**0.01**	**8.46**	**101**
DAC Playback 44.1kHz Stereo HP DAC ➞ HP Low power mode, 24-bit, music filters	**1.25**	**0.47**	**0.00**	**1.25**	**0.01**	**5.34**	**98**
DAC Playback 8kHz Stereo HP DAC ➞ HP 16-bit, voice filters	**2.04**	**1.27**	**0.00**	**1.07**	**0.00**	**7.89**	**96**
DAC Playback 8kHz Stereo HP DAC ➞ HP 16-bit, low power mode, voice filters	**1.26**	**0.47**	**0.00**	**0.90**	**0.00**	**4.72**	**96**
DAC Playback 8kHz Mono HP DAC ➞ HP 16-bit, low power mode, voice filters	**0.77**	**0.29**	**0.00**	**0.79**	**0.00**	**3.33**	**98**
Line Playback Stereo HP INA ➞ HP Single-ended inputs	**2.40**	**1.27**	**0.00**	**0.02**	**0.00**	**6.67**	**95**
DAC Playback to Class D Speaker							
DAC Playback 48kHz Stereo SPK DAC ➞ SPK 24-bit, music filters	**2.31**	**0.00**	**6.33**	**2.14**	**0.01**	**31.44**	**92**

功耗(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, MAS = 0.)

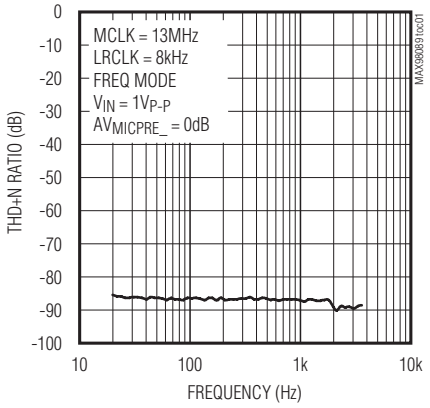
MODE	I_{AVDD} (mA)	I_{PVDD} (mA)	I_{SPKVDD} + $I_{SPKLVDD}$ (mA)	I_{DVDD} (mA)	I_{DVDDS1} + I_{DVDDS2} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
DAC Playback 48kHz Mono SPK DAC ➞ SPK 24-bit, music filters	**1.35**	**0.00**	**3.23**	**1.84**	**0.01**	**17.69**	**92**
Line Playback Mono SPK INA ➞ SPKL Differential inputs	**1.01**	**0.00**	**3.24**	**0.03**	**0.00**	**13.83**	**93**
Full Duplex							
Full-Duplex 8kHz Mono RCV MIC1 ➞ ADC DAC ➞ REC 16-bit, voice filters	**6.32**	**0.00**	**1.54**	**1.24**	**0.01**	**19.33**	**Record = 93** **Playback = 94**
Full-Duplex 8kHz Stereo HP MIC1/2 ➞ ADC DAC ➞ HP 16-bit, mixer, voice filters	**11.19**	**1.27**	**0.48**	**1.28**	**0.01**	**26.43**	**Record = 93** **Playback = 96**
Full-Duplex 8kHz Stereo HP MIC1/2 ➞ ADC DAC ➞ HP 16-bit, low power mode, voice filters	**7.12**	**0.47**	**0.48**	**1.10**	**0.02**	**17.44**	**Record = 93** **Playback = 96**
Line Record							
Line Stereo Record 48kHz INA ➞ ADC 24-bit, low power, music filters	**6.19**	**0.00**	**0.20**	**1.31**	**0.15**	**14.47**	**91**
Line Stereo Record 48kHz INA ➞ ADC Direct pin input, 24bit, low power, music filters	**5.69**	**0.00**	**0.20**	**1.31**	**0.12**	**13.53**	**93**

典型工作特性

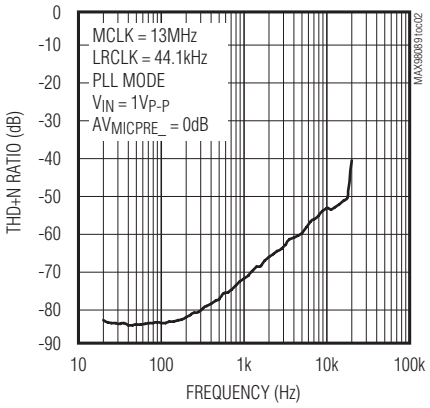
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

麦克风至ADC

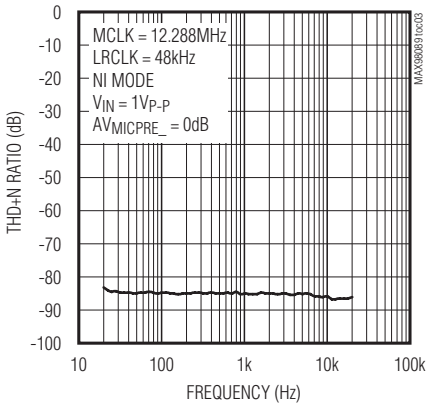
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



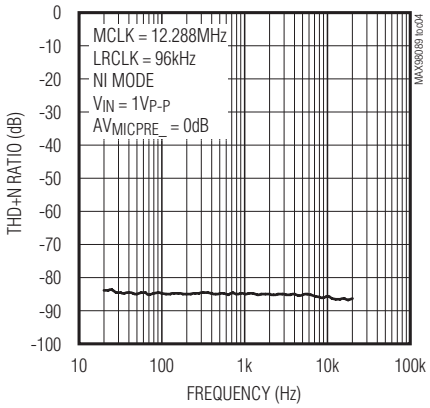
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



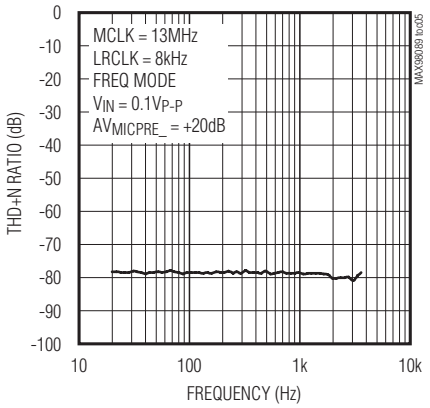
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



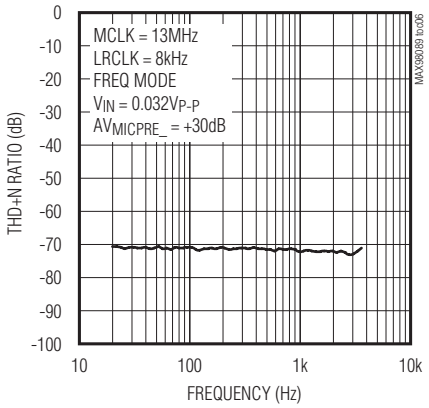
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



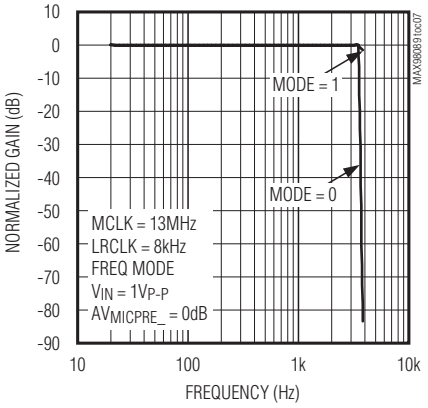
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



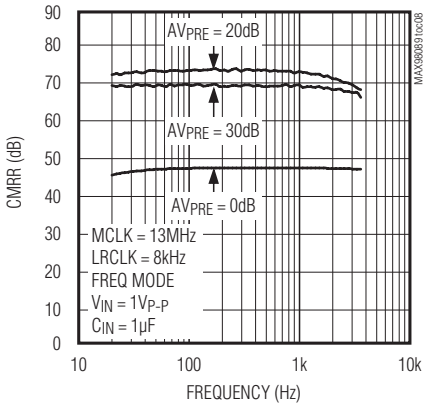
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

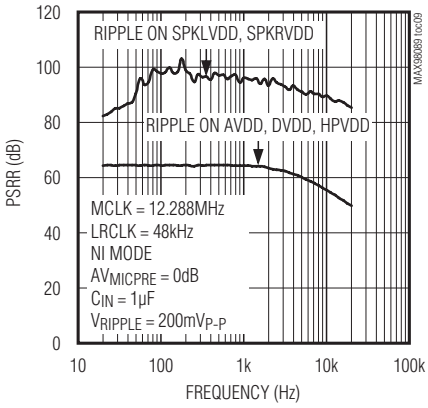
GAIN vs. FREQUENCY (MIC TO ADC)



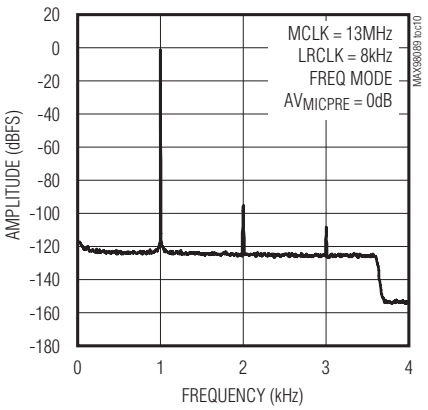
COMMON-MODE REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



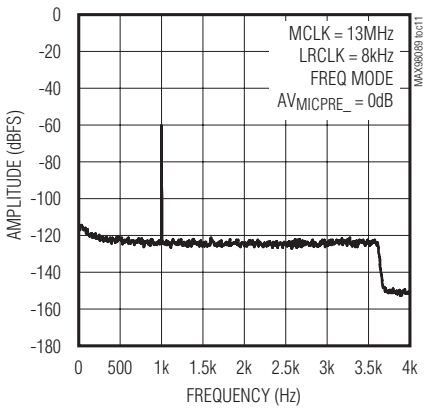
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



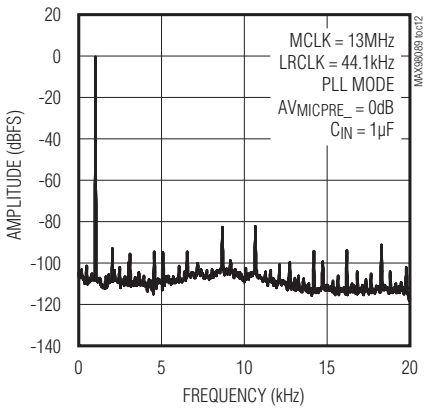
FFT, 0dBFS (MIC TO ADC)



FFT, -60dBFS (MIC TO ADC)



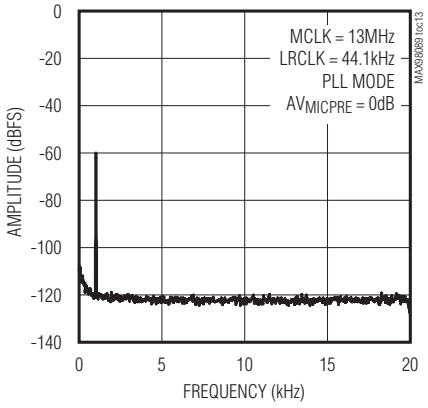
FFT, 0dBFS (MIC TO ADC)



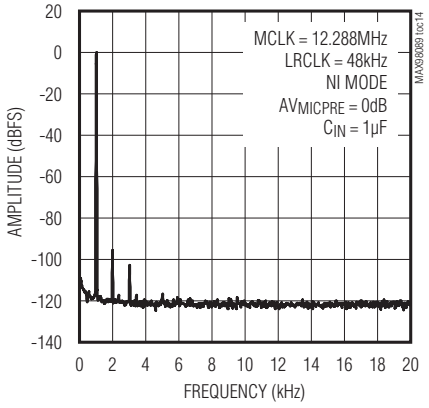
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

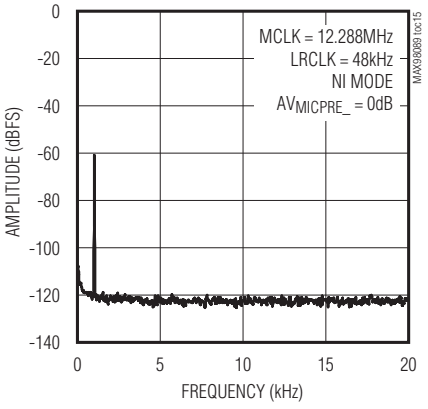
FFT, -60dBFS (MIC TO ADC)



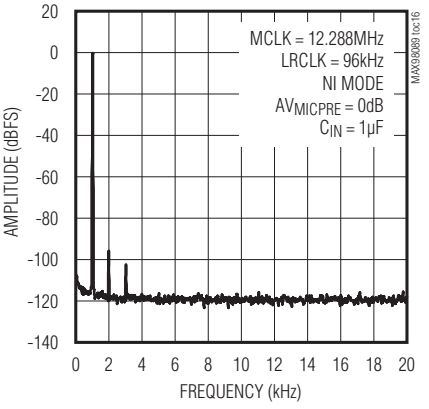
FFT, 0dBFS (MIC TO ADC)



FFT, -60dBFS (MIC TO ADC)



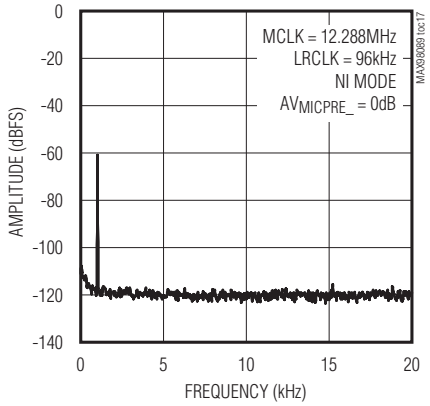
FFT, 0dBFS (MIC TO ADC)



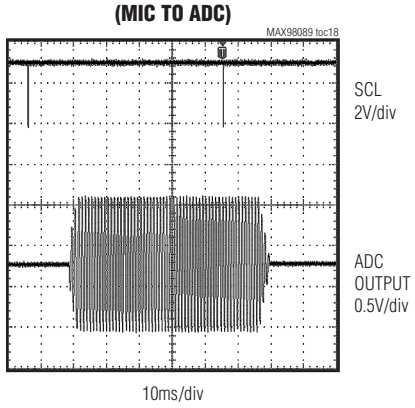
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

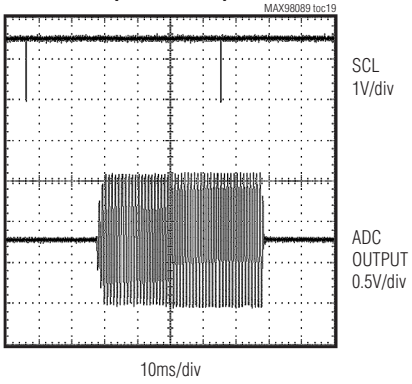
FFT, -60dBFS (MIC TO ADC)



ADC ENABLE/DISABLE RESPONSE (MIC TO ADC)



SOFTWARE TURN-ON/OFF RESPONSE (MIC TO ADC)

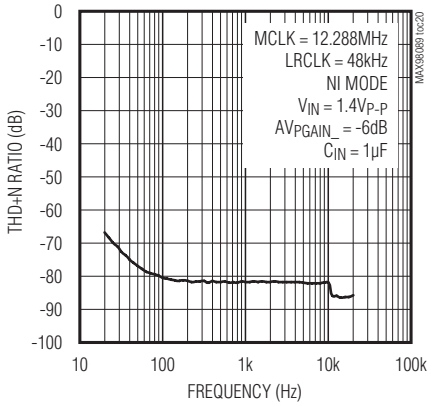


典型工作特性(续)

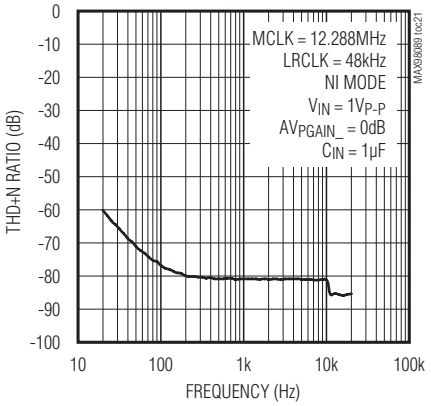
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

线入至ADC

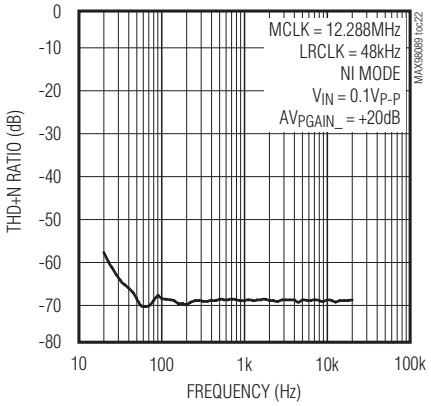
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



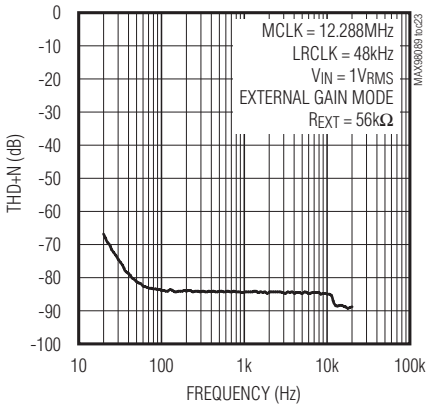
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



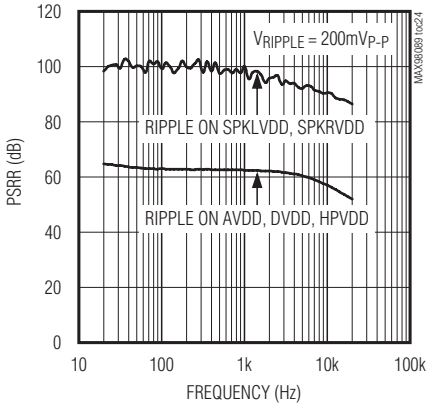
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE-IN TO ADC)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO ADC)

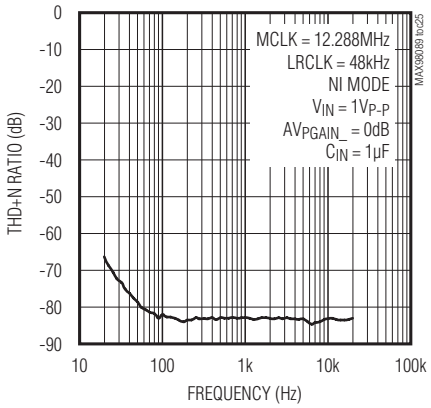


典型工作特性(续)

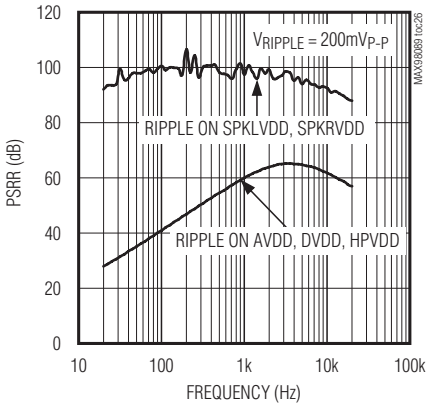
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

线入引脚直通ADC

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC PIN DIRECT)

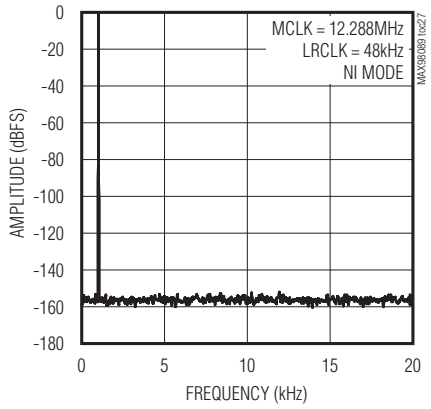


POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO ADC PIN DIRECT)

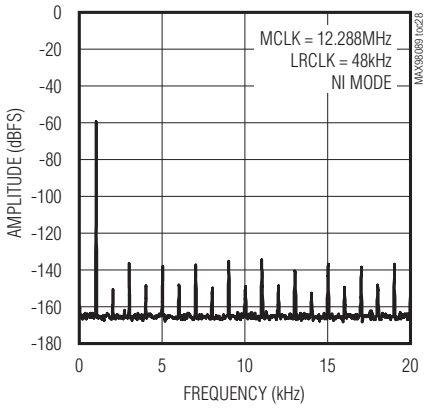


数字环回

FFT, 0dBFS (SDINS1 TO SDINS2 DIGITAL LOOPBACK)



FFT, -60dBFS (SDINS1 TO SDINS2 DIGITAL LOOPBACK)

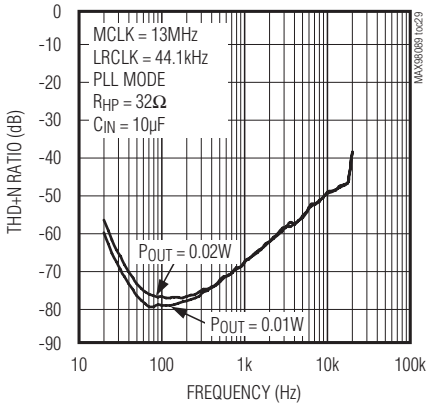


典型工作特性(续)

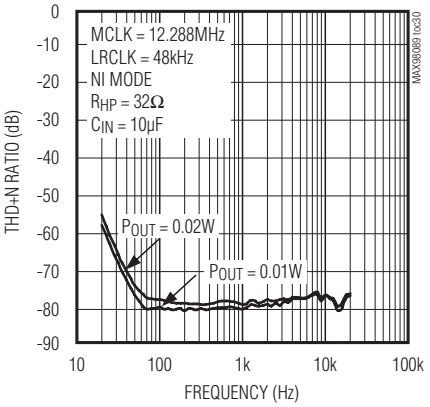
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

模拟环回

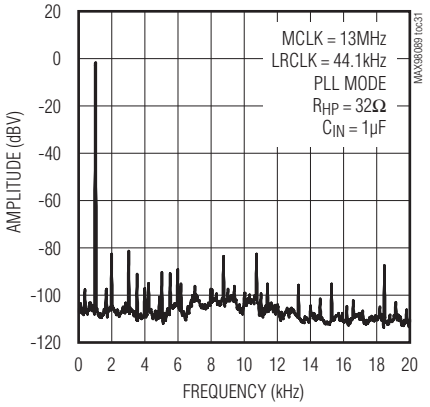
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)



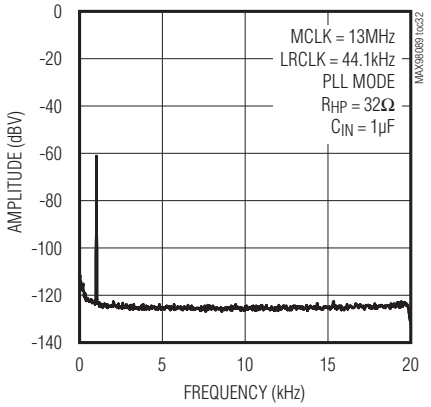
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)



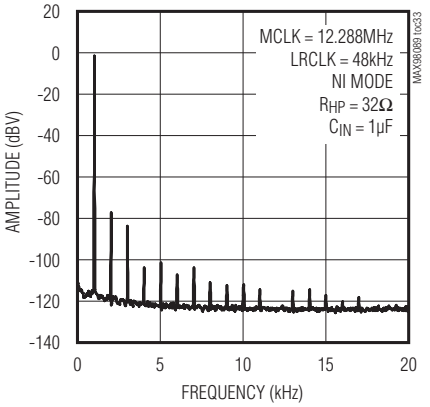
FFT, 0dBFS (LINE TO ADC TO DAC TO HEADPHONE)



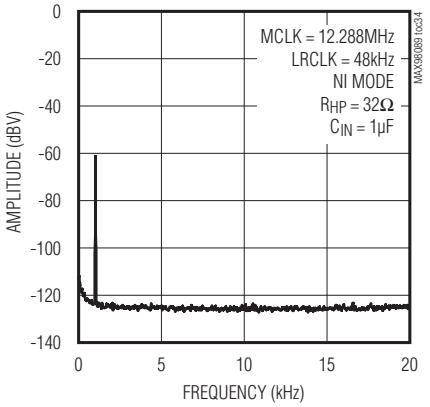
FFT, -60dBFS (LINE TO ADC TO DAC TO HEADPHONE)



FFT, 0dBFS (LINE TO ADC TO DAC TO HEADPHONE)



FFT, -60dBFS (LINE TO ADC TO DAC TO HEADPHONE)

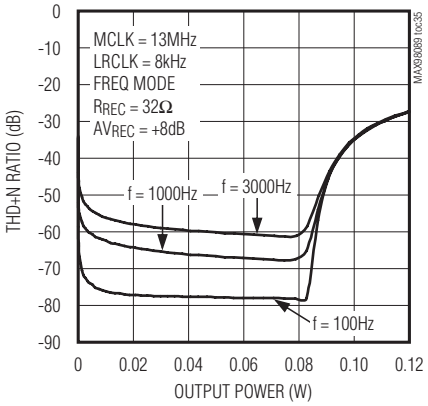


典型工作特性(续)

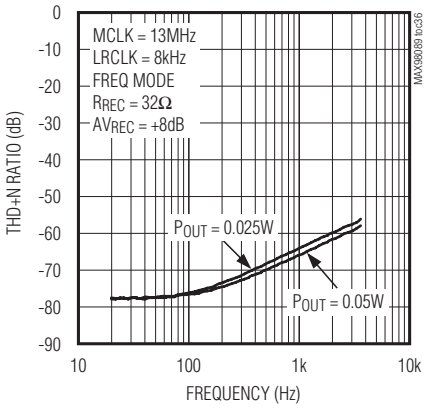
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

DAC至接收器

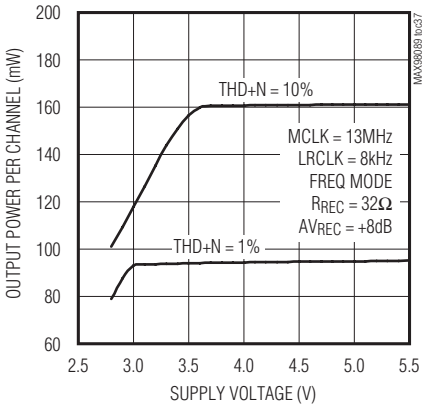
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER (DAC TO RECEIVER)



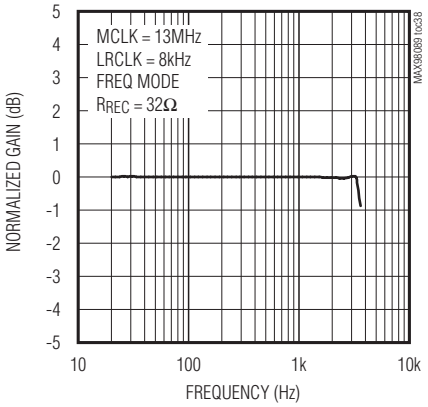
TOTAL HARMONIC DISTORTION vs. FREQUENCY (DAC TO RECEIVER)



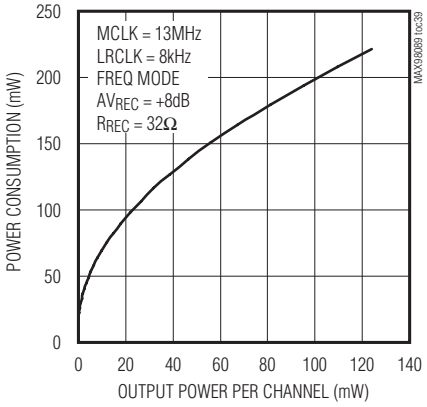
OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO RECEIVER)



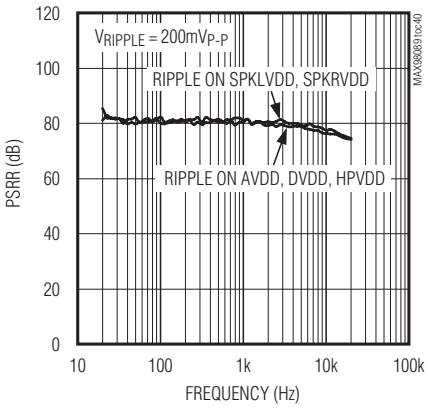
GAIN vs. FREQUENCY (DAC TO RECEIVER)



POWER CONSUMPTION vs. OUTPUT POWER (DAC TO RECEIVER)



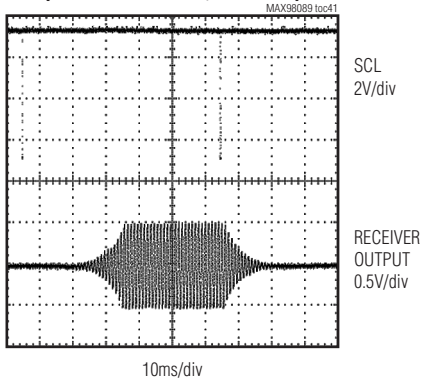
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO RECEIVER)



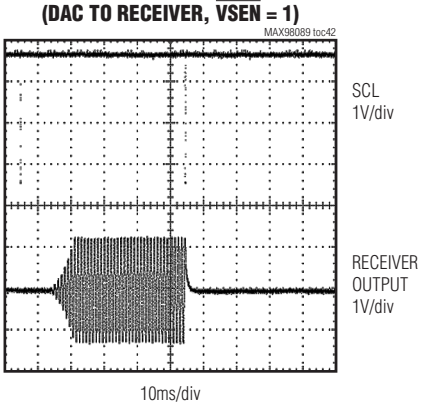
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

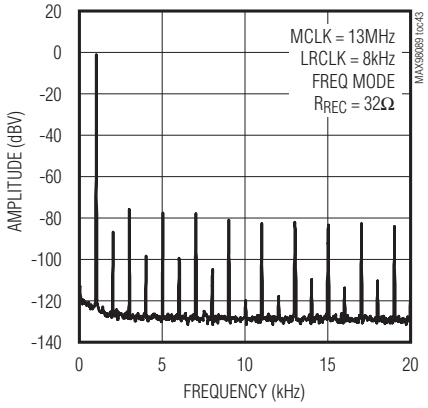
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO RECEIVER, $\overline{VSEN}$ = 0)



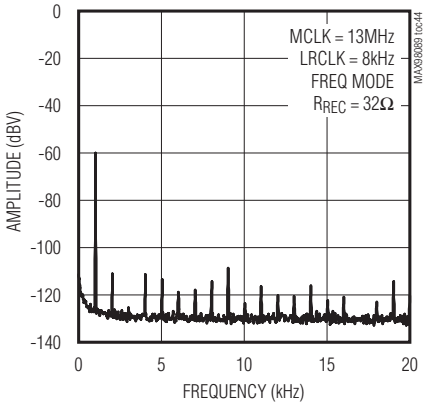
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO RECEIVER, $\overline{VSEN}$ = 1)



FFT, 0dBFS (DAC TO RECEIVER)



FFT, -60dBFS (DAC TO RECEIVER)

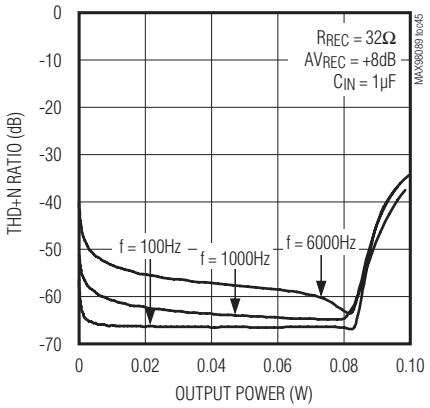


典型工作特性(续)

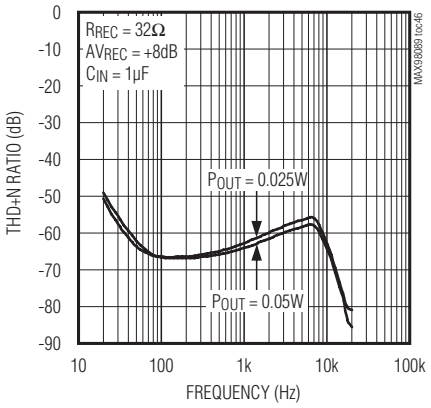
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

线入至接收器

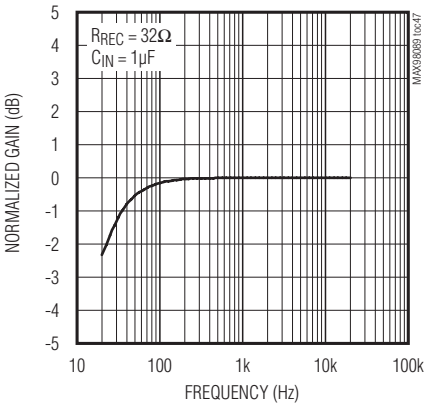
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO RECEIVER)



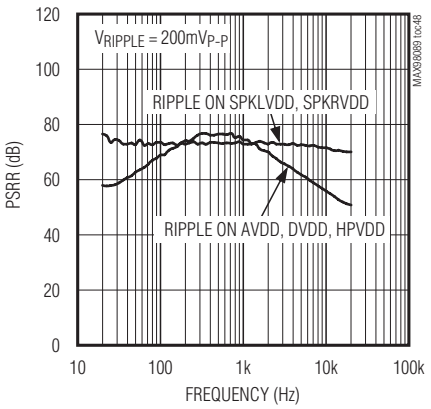
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO RECEIVER)



GAIN vs. FREQUENCY (LINE TO RECEIVER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO RECEIVER)

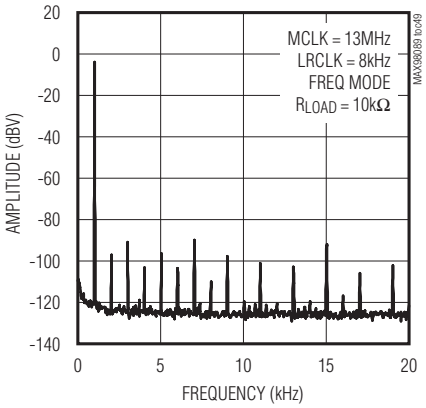


典型工作特性(续)

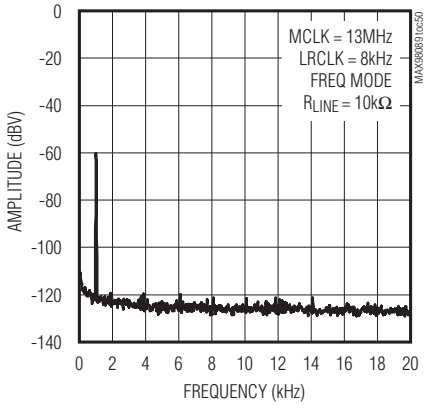
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

DAC至线出

INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO LINE)

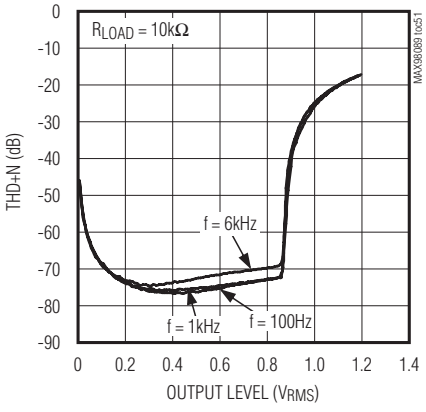


INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO LINE)

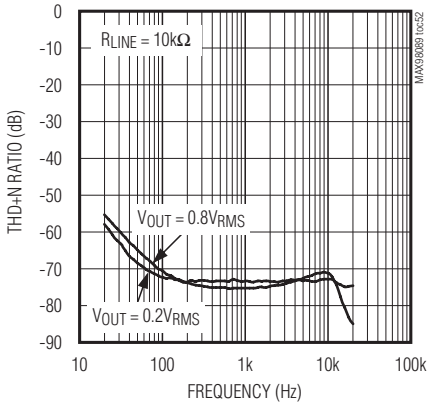


线入至线出

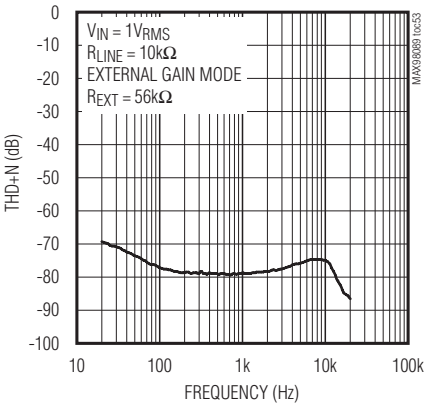
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT LEVEL (LINE-IN TO LINE-OUT)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE IN TO LINE OUT)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE-IN TO LINE-OUT)

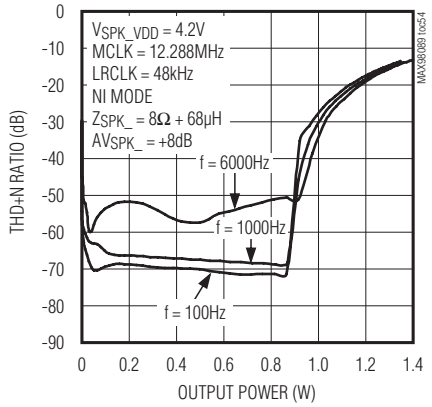


典型工作特性(续)

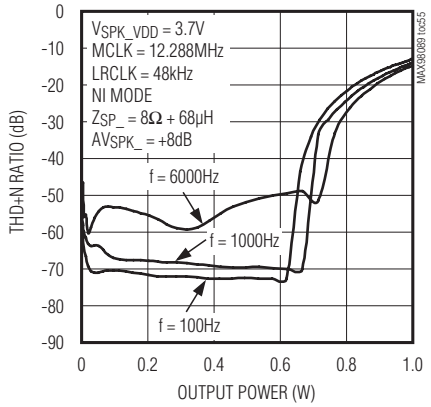
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

DAC至扬声器

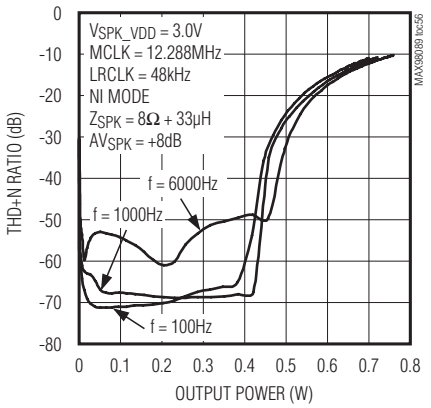
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



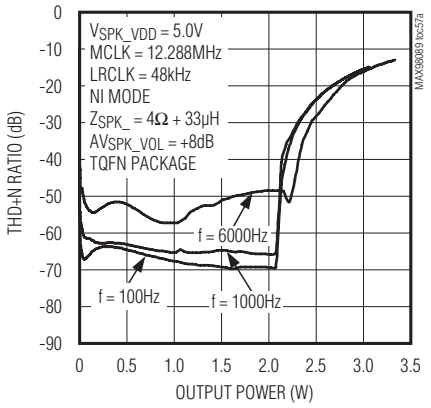
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



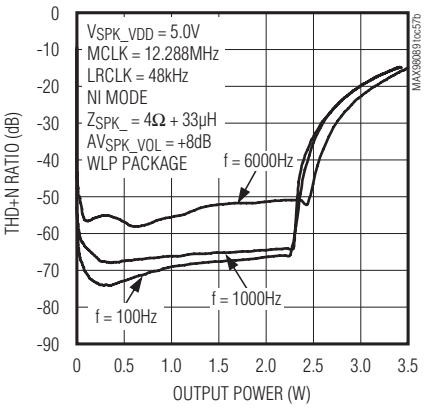
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



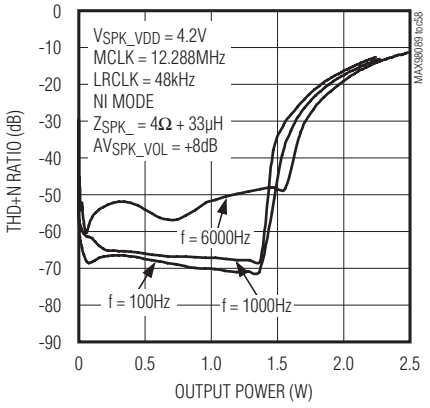
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



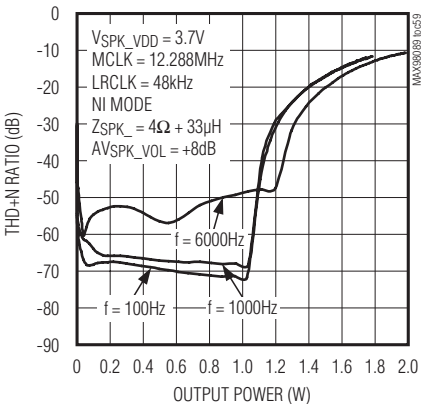
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

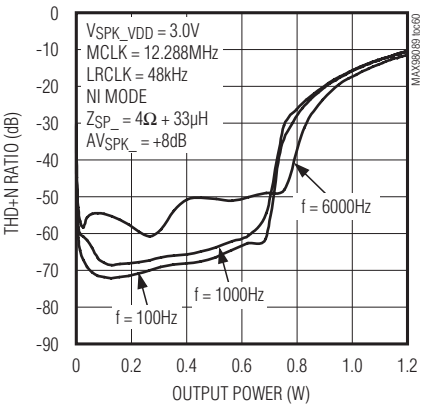
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



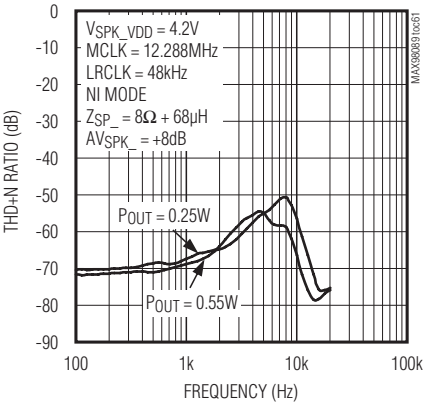
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



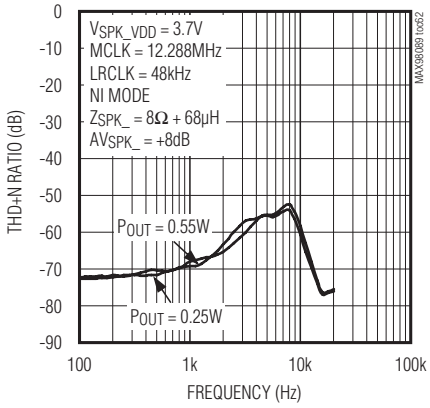
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



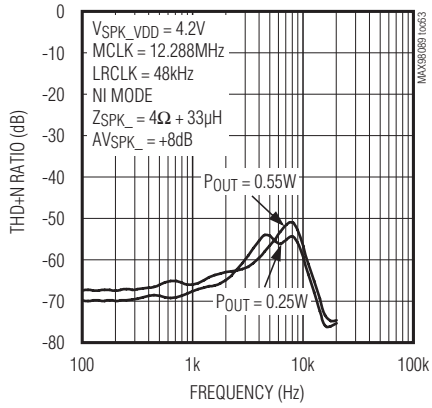
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



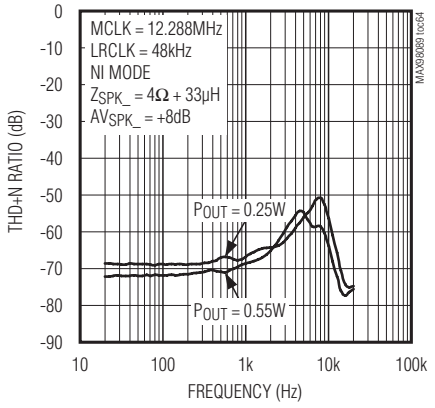
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



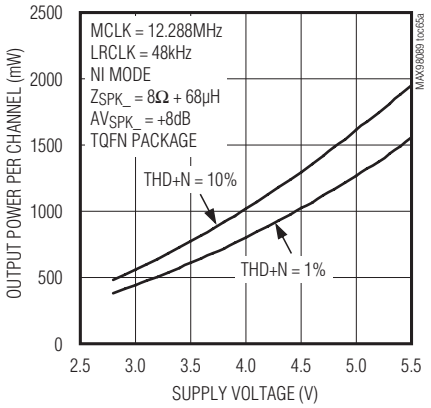
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

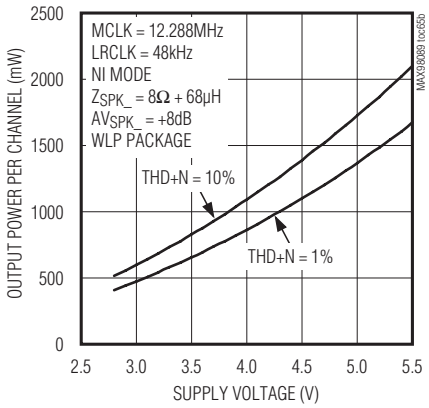
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



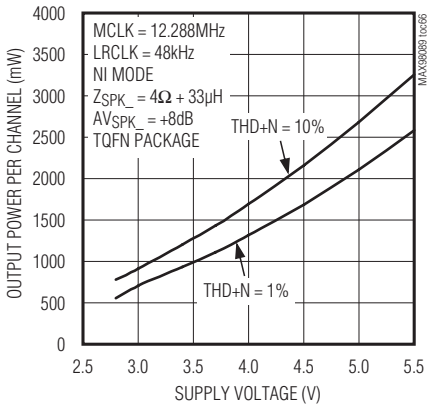
OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



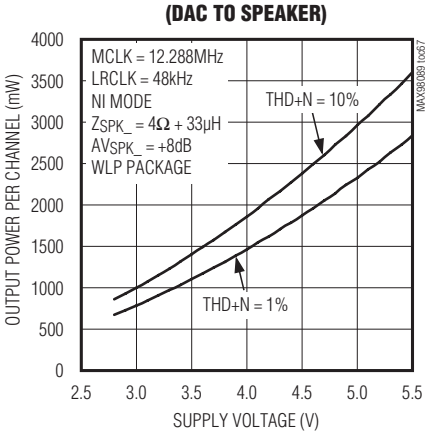
OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



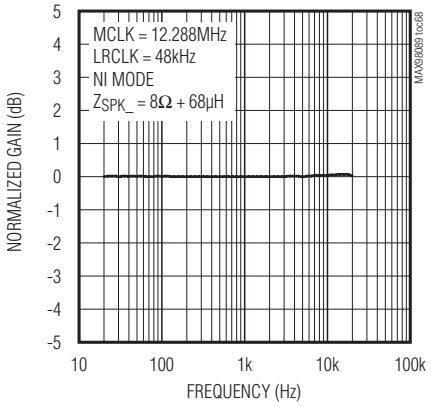
OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



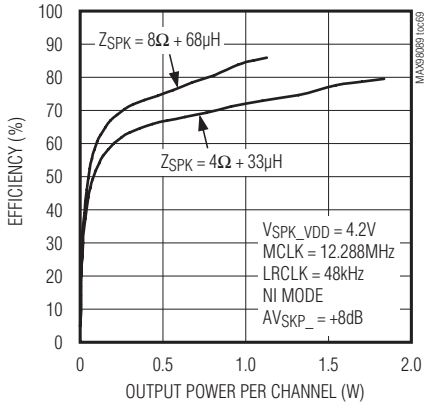
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

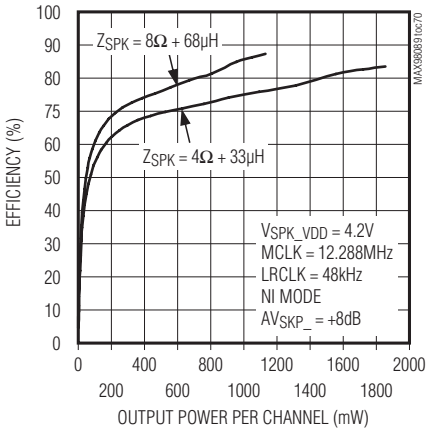
GAIN vs. FREQUENCY (DAC TO SPEAKER)



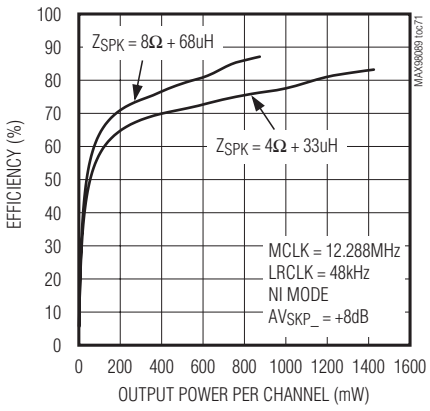
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



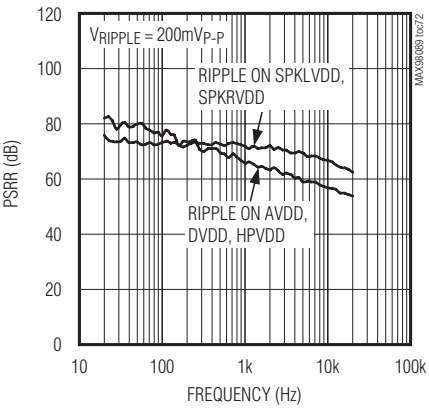
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



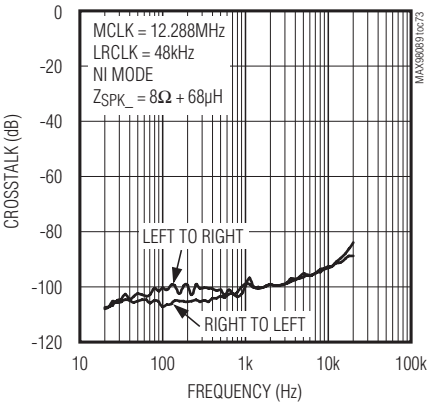
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO SPEAKER)



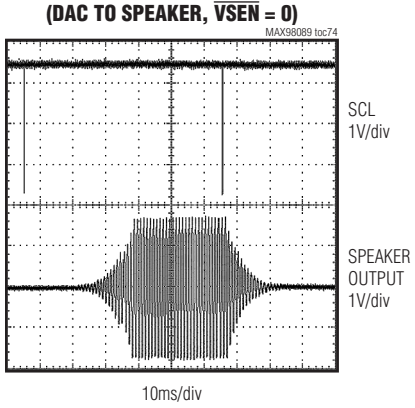
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

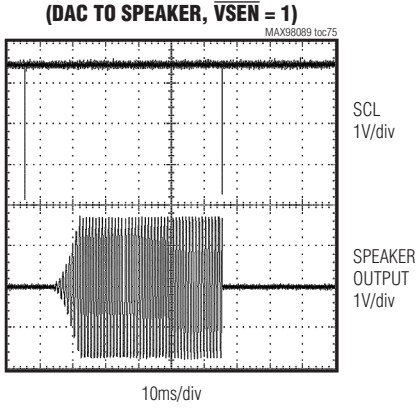
CROSSTALK vs. FREQUENCY (DAC TO SPEAKER)



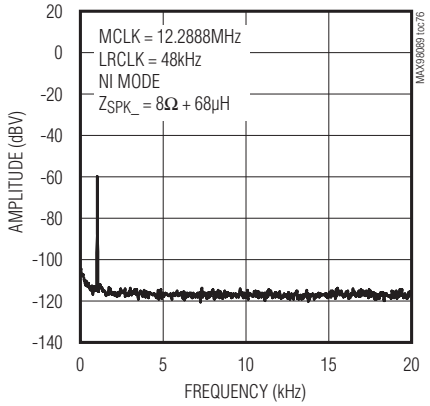
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO SPEAKER, $\overline{VSEN}$ = 0)



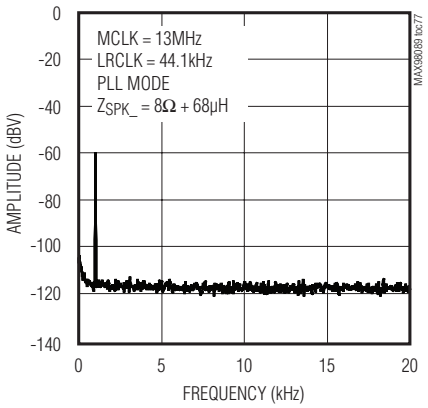
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO SPEAKER, $\overline{VSEN}$ = 1)



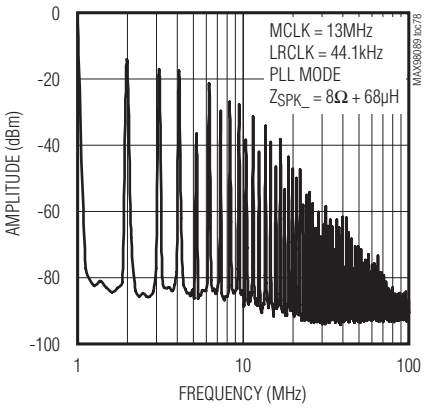
FFT, -60dBFS (DAC TO SPEAKER)



FFT, -60dBFS (DAC TO SPEAKER)



WIDEBAND FFT (DAC TO SPEAKER)

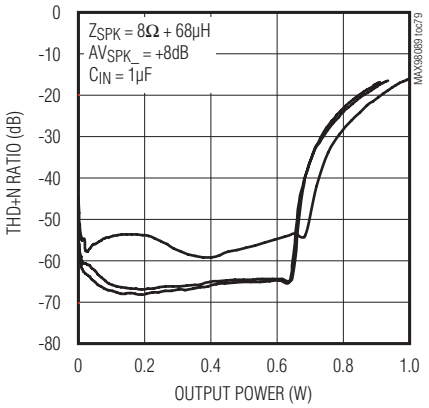


典型工作特性(续)

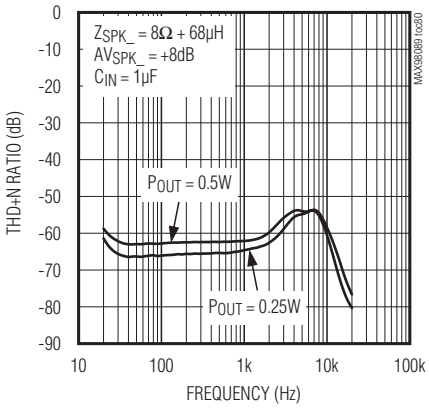
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

线入至扬声器

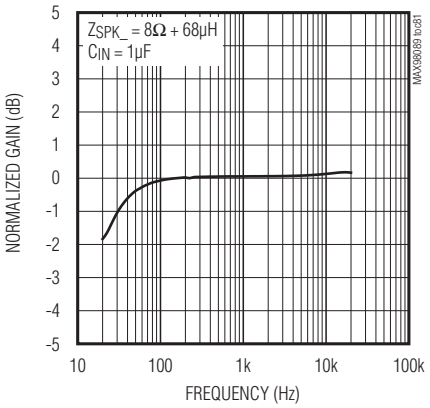
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO SPEAKER)



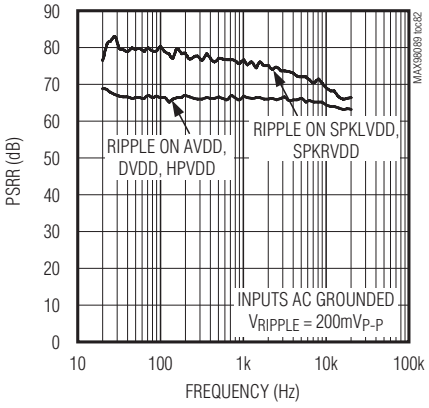
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO SPEAKER)



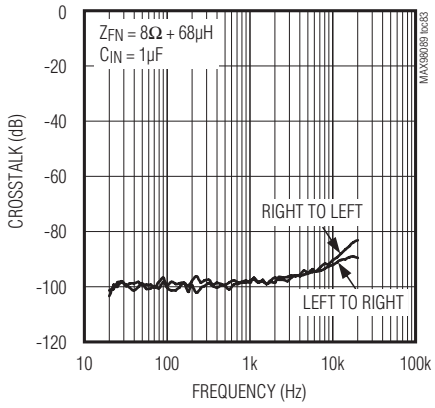
GAIN vs. FREQUENCY (LINE TO SPEAKER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO SPEAKER)



CROSSTALK vs. FREQUENCY (LINE TO SPEAKER)

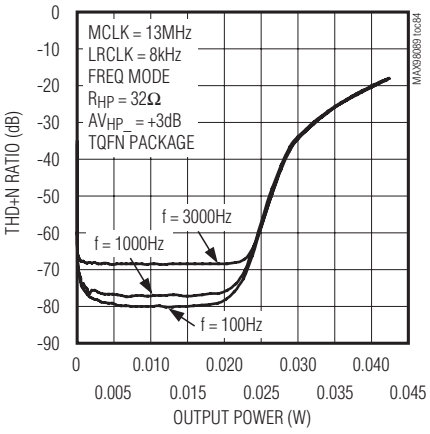


典型工作特性(续)

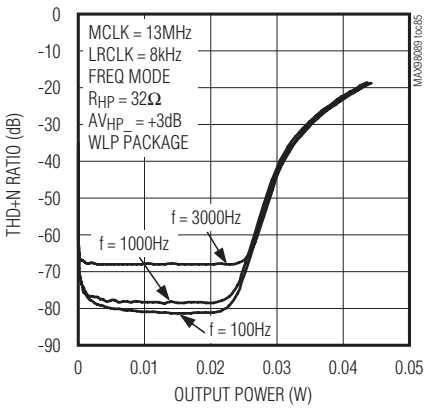
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

DAC至耳机

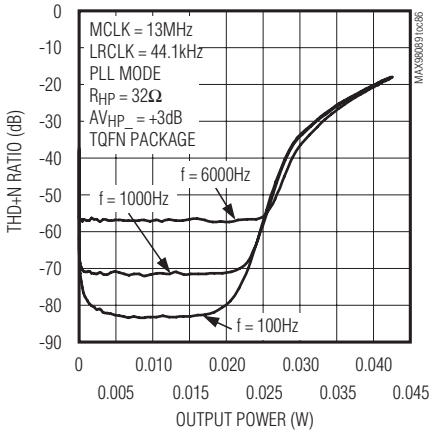
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



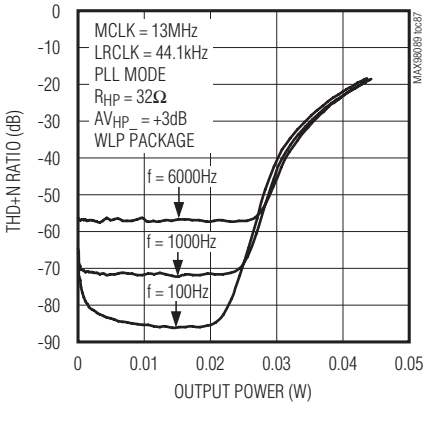
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



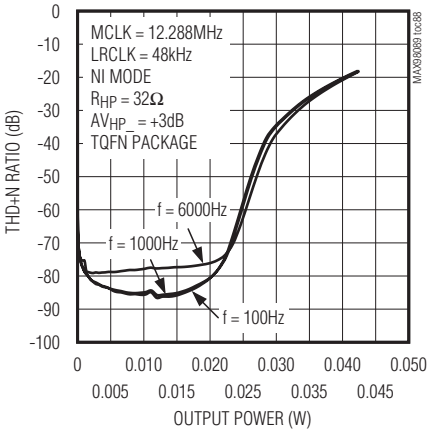
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



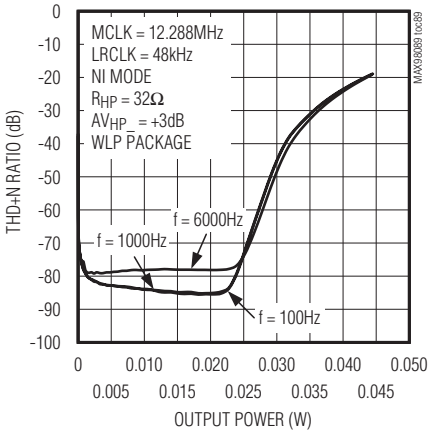
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



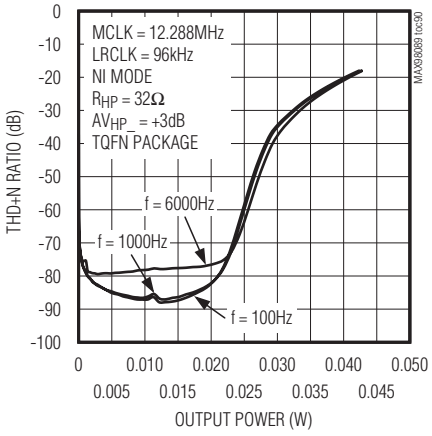
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

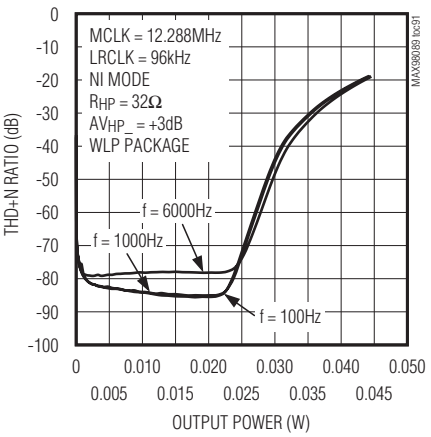
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



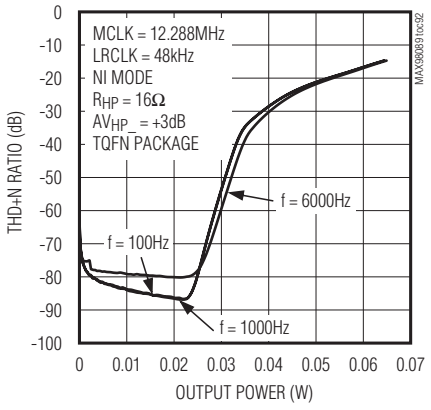
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



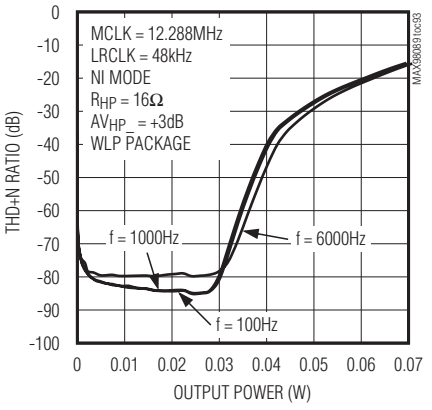
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



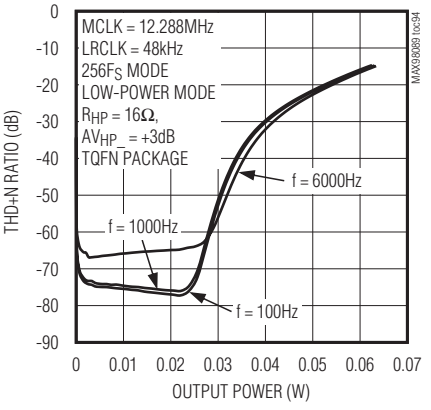
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



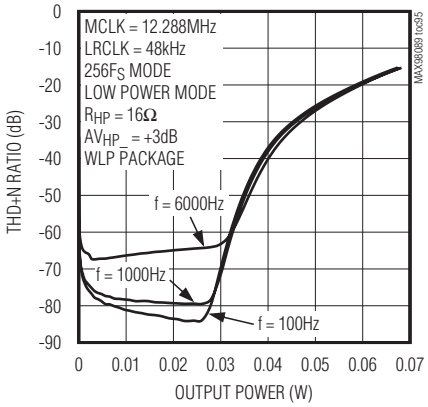
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



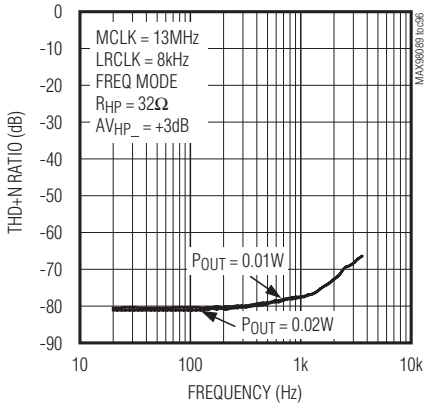
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

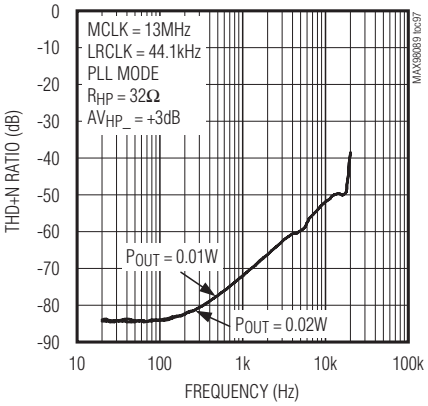
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



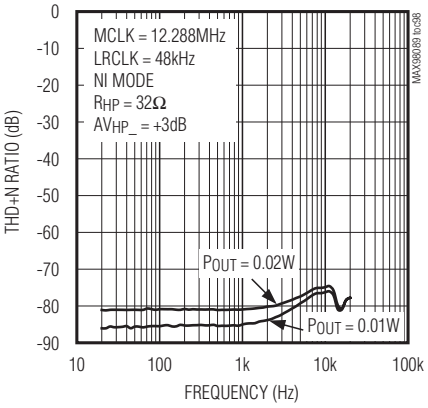
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



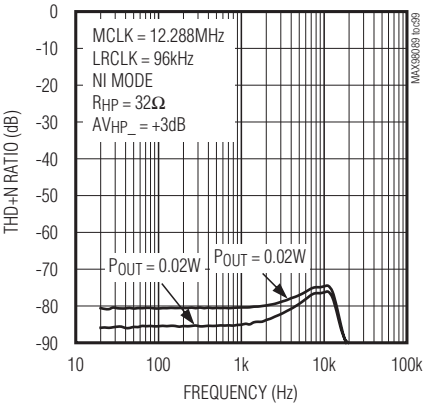
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



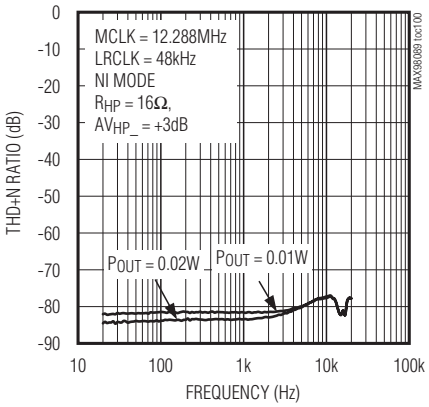
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



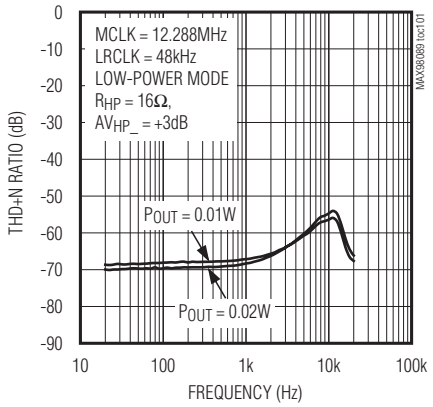
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

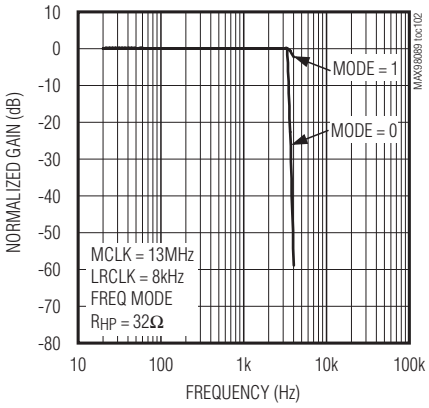
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



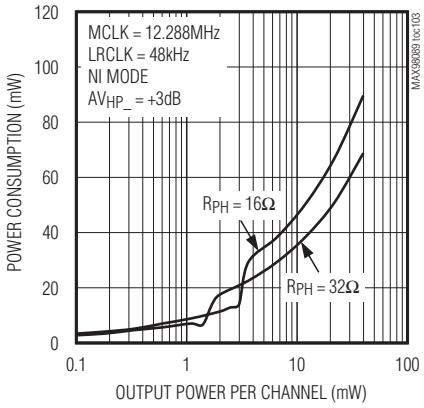
GAIN vs. FREQUENCY (DAC TO HEADPHONE)



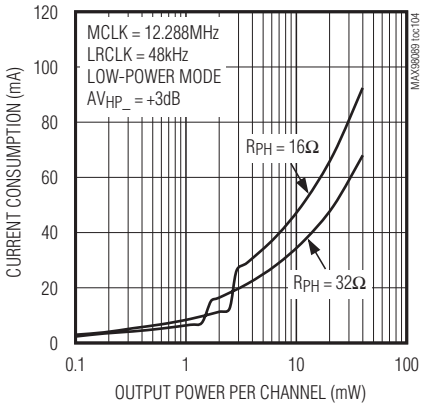
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

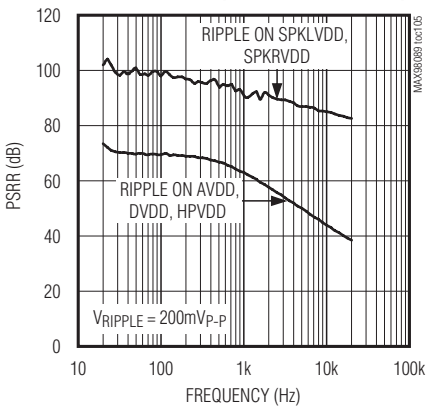
POWER CONSUMPTION vs. OUTPUT POWER (DAC TO HEADPHONE)



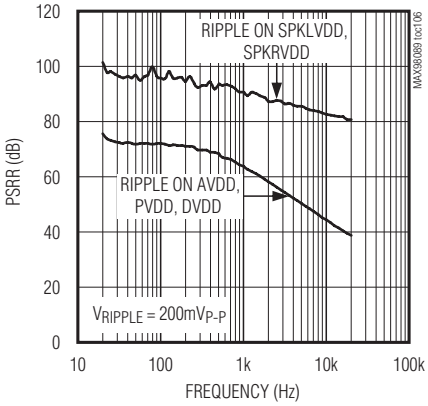
CURRENT CONSUMPTION vs. OUTPUT POWER (DAC TO HEADPHONE)



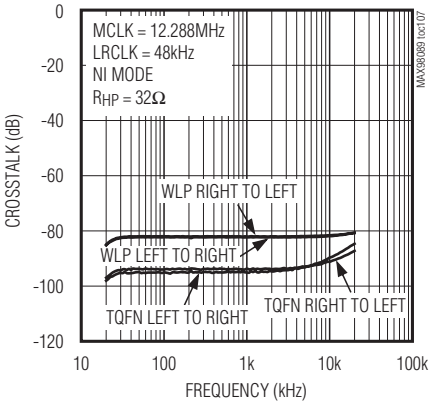
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



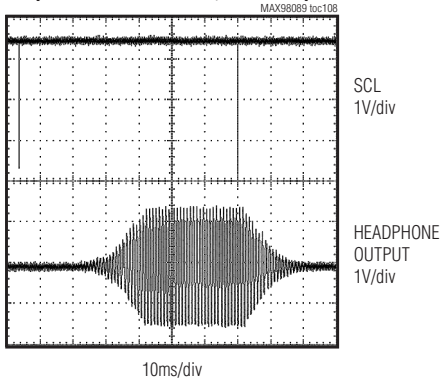
CROSSTALK vs. FREQUENCY (DAC TO HEADPHONE)



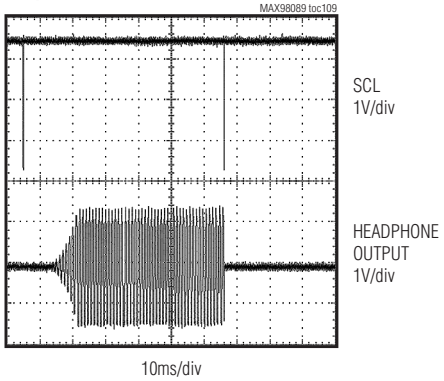
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

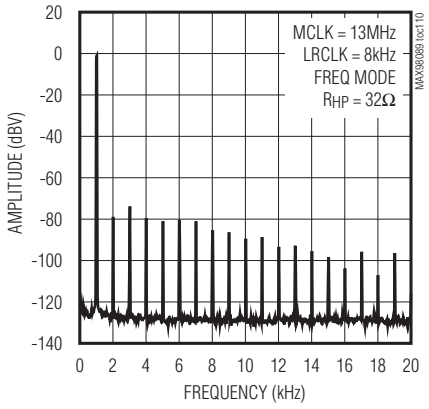
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO HEADPHONE, $\overline{VSEN}$ = 0)



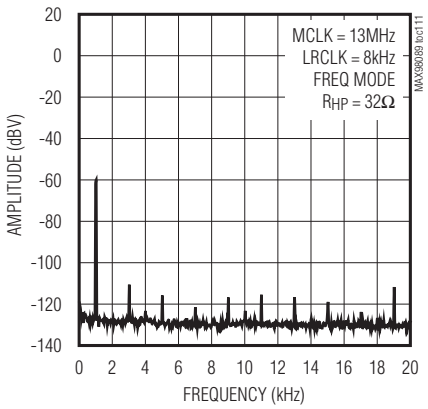
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO HEADPHONE, $\overline{VSEN}$ = 1)



FFT, 0dBFS (DAC TO HEADPHONE)



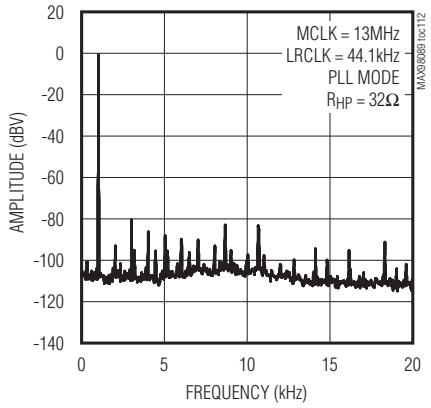
FFT, -60dBFS (DAC TO HEADPHONE)



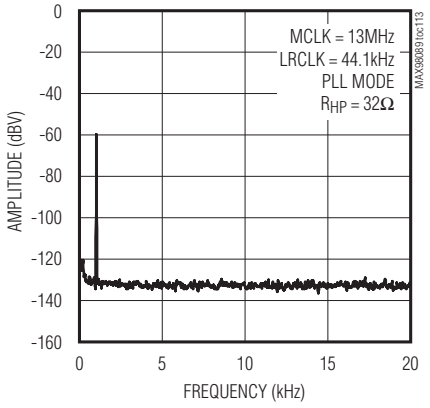
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

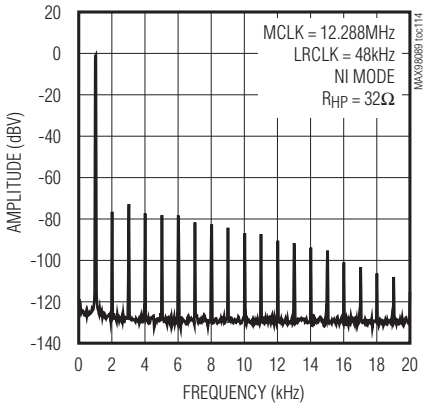
INBAND FREQUENCY SPECTRUM, 0dBFS (DAC TO HEADPHONE)



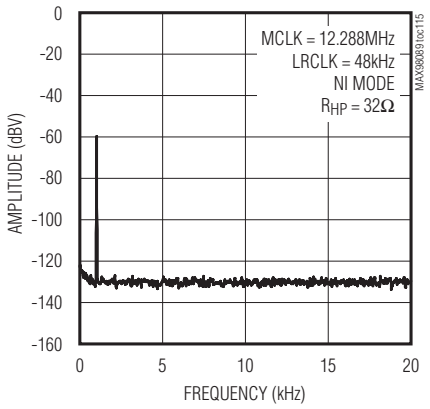
FFT, -60dBFS (DAC TO HEADPHONE)



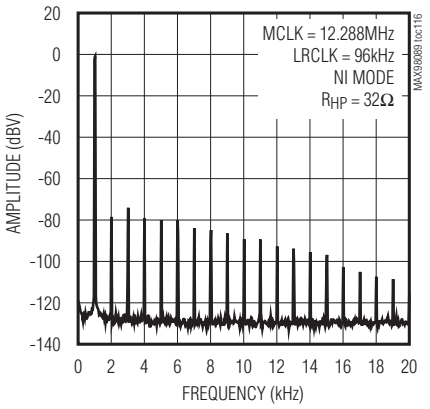
FFT, 0dBFS (DAC TO HEADPHONE)



FFT, -60dBFS (DAC TO HEADPHONE)



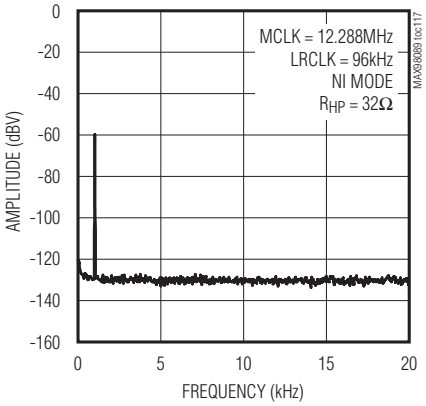
FFT, 0dBFS (DAC TO HEADPHONE)



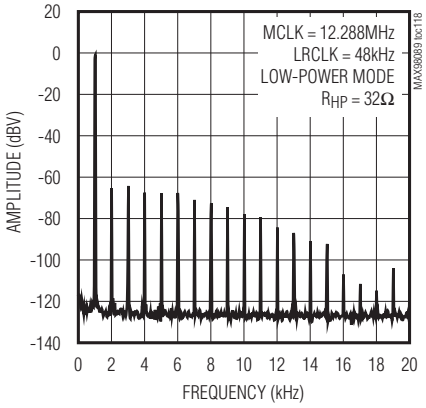
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

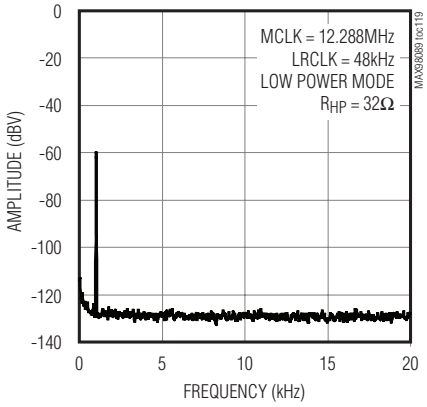
FFT, -60dBFS (DAC TO HEADPHONE)



FFT, 0dBFS (DAC TO HEADPHONE)

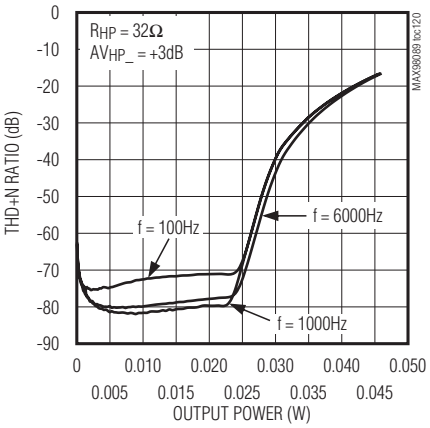


FFT, -60dBFS (DAC TO HEADPHONE)

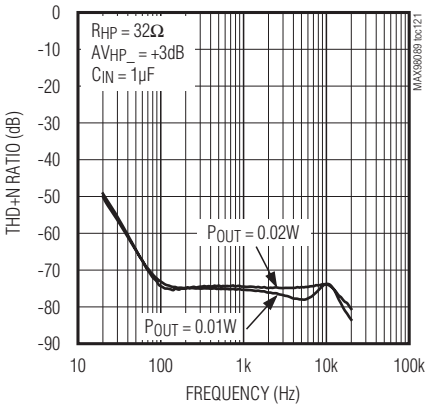


线入至耳机

TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO HEADPHONE)



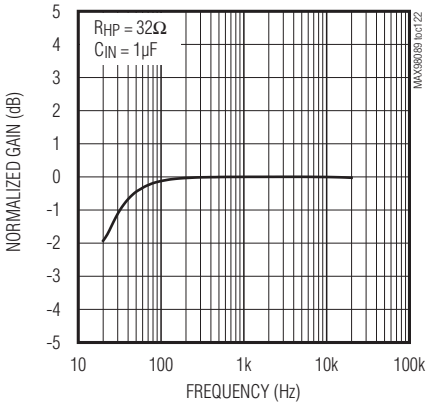
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO HEADPHONE)



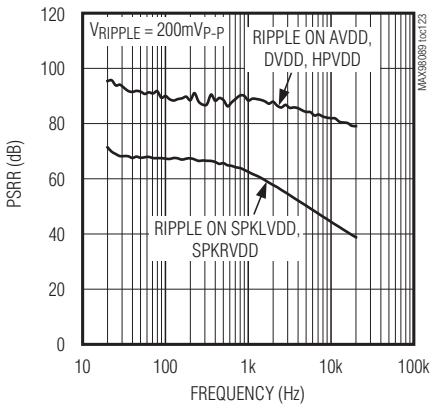
典型工作特性(续)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

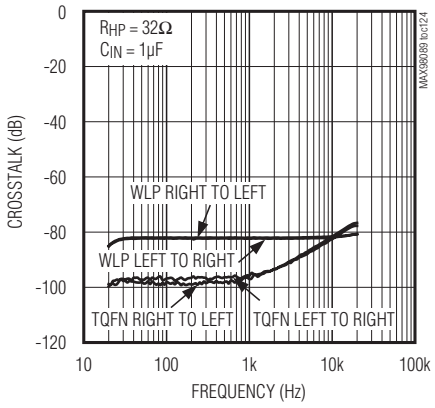
GAIN vs. FREQUENCY (LINE TO HEADPHONE)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONE)



CROSSTALK vs. FREQUENCY (LINE TO HEADPHONE)

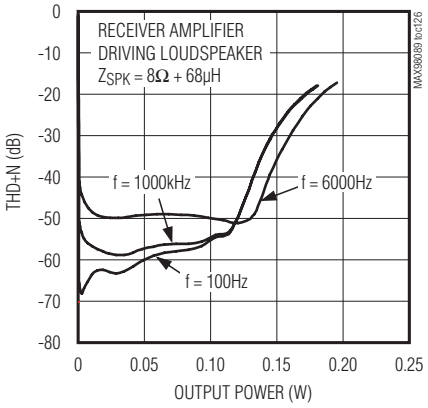


典型工作特性(续)

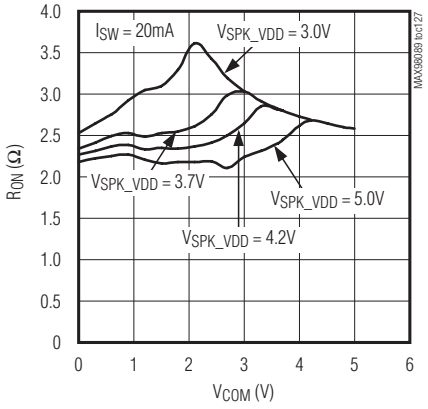
(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to HPGND. Line out (R_{LOUT}) connected from LOUTL or LOUTR to SPKLGND, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVDD} = C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

扬声器旁路开关

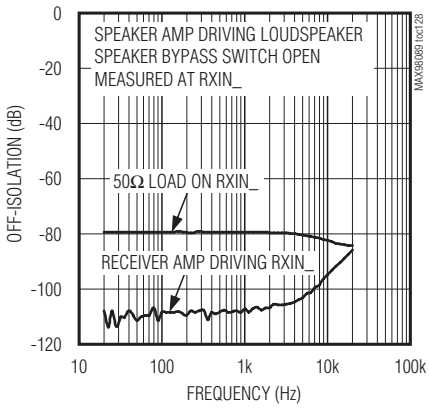
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER BYPASS SWITCH)



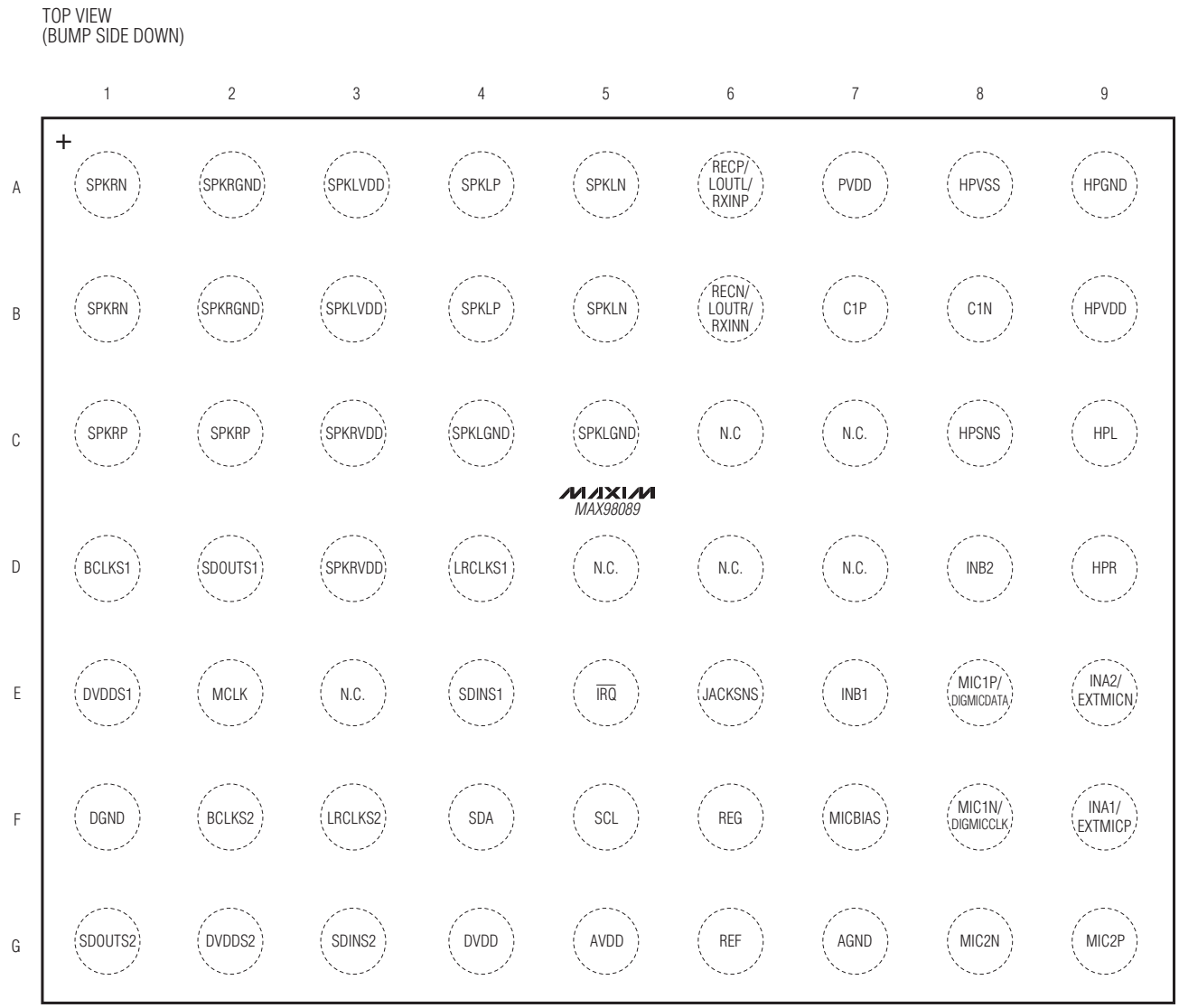
ON-RESISTANCE vs. VCOM (SPEAKER BYPASS SWITCH)



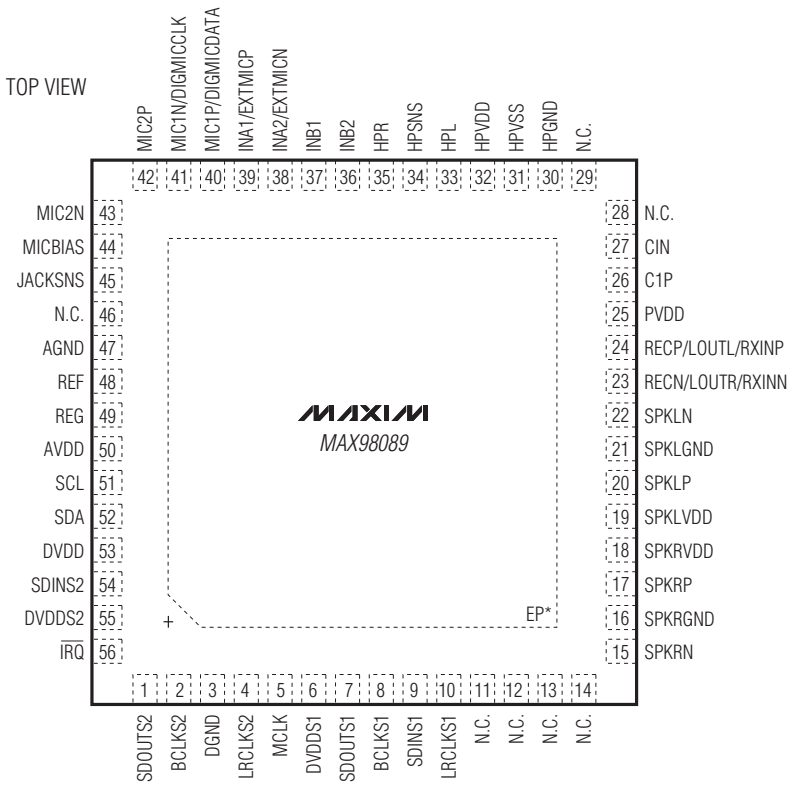
OFF-ISOLATION vs. FREQUENCY (SPEAKER BYPASS SWITCH)



焊球配置


TOP VIEW
(BUMP SIDE DOWN)
1 2 3 4 5 6 7 8 9
A SPKRN SPKRGND SPKLVDD SPKLP SPKLN RECP/ LOUTL/ RXINP PVDD HPVSS HPGND
B SPKRN SPKRGND SPKLVDD SPKLP SPKLN RECN/ LOUTR/ RXINN C1P C1N HPVDD
C SPKRP SPKRP SPKRVDD SPKLGND SPKLGND N.C N.C. HPSNS HPL
D BCLKS1 SDOUTS1 SPKRVDD LRCLKS1 N.C. N.C. N.C. INB2 HPR
E DVDDS1 MCLK N.C. SDINS1 IRQ JACKSNS INB1 MIC1P/ DIGMICDATA INA2/ EXTMICN
F DGND BCLKS2 LRCLKS2 SDA SCL REG MICBIAS MIC1N/ DIGMICCLK INA1/ EXTMICP
G SDOUTS2 DVDDS2 SDINS2 DVDD AVDD REF AGND MIC2N MIC2P
MAXIM
MAX98089

引脚配置



TQFN
(7mm x 7mm x 0.75mm)

*EP = EXPOSED PAD. CONNECT TO GROUND PLANE.

焊球/引脚说明

焊球 (WLP)	引脚 (TQFN-EP)	名称	功能
A1, B1	15	SPKRN	右声道D类扬声器输出负端。
A2, B2	16	SPKRGND	右声道扬声器地。
A3, B3	19	SPKLVDD	左声道扬声器、REF、接收放大器电源。通过1µF和10µF电容旁路至SPKLGND。
A4, B4	20	SPKLP	左声道D类扬声器输出正端。
A5, B5	22	SPKLN	左声道D类扬声器输出负端。
A6	24	RECP/LOUTL/ RXINP	接收放大器输出正端或左声道线出。接收放大器关断时，可以作为旁路开关正端。
A7	25	PVDD	耳机电源，利用1µF和10µF电容旁路至HPGND。
A8	31	HPVSS	电荷泵反相输出，利用1µF陶瓷电容旁路至HPGND。
A9	30	HPGND	耳机地。
B6	23	RECN/LOUTR/ RXINN	接收放大器输出负端或右声道线出。接收放大器关断时，可以作为旁路开关负端。
B7	26	C1P	电荷泵飞电容正端，在C1N和C1P之间连接1µF陶瓷电容。
B8	27	C1N	电荷泵飞电容负端，在C1N和C1P之间连接1µF陶瓷电容。
B9	32	HPVDD	电荷泵同相输出，利用1µF陶瓷电容旁路至HPGND。
C1, C2	17	SPKRP	右声道D类扬声器输出正端。
C3, D3	18	SPKRVDD	右声道扬声器电源，利用1µF的电容旁路至SPKRGND。
C4, C5	21	SPKLGND	左声道扬声器地。
C6, C7, D5, D6, D7, E3	11–14, 28, 29, 46	N.C.	浮空。
C8	34	HPSNS	耳机放大器地检测，连接至耳机插孔地端子以优化性能，或连接至PCB地。
C9	33	HPL	左声道耳机输出。
D1	8	BCLKS1	S1数字音频的位时钟输入/输出。BCLKS1在IC处于从模式时作为输入，在主模式下作为输出。输入/输出电压以DVDDS1为参考。
D2	7	SDOUTS1	S1数字音频串行数据ADC输出，输出电压以DVDDS1为参考。
D4	10	LRCLKS1	S1数字音频左、右声道的时钟输入/输出。LRCLKS1为音频采样率时钟，决定S1音频数据是否送至左、右声道。TDM模式下，LRCLKS1为帧同步脉冲。LRCLKS1在IC处于从模式时为输入，在主模式下作为输出。
D8	36	INB2	单端线入B2，也是差分线入B的正端。
D9	35	HPR	右声道耳机输出。

焊球/引脚说明(续)

焊球 (WLP)	引脚 (TQFN-EP)	名称	功能
E1	6	DVDDS1	S1数字音频接口的电源输入，利用一个1µF电容旁路至DGND。
E2	5	MCLK	主机时钟输入，可接受的输入频率范围为10MHz至60MHz。
E4	9	SDINS1	S1数字音频串行数据DAC输入，输入/输出电压以DVDDS1为参考。
E5	56	$\overline{IRQ}$	硬件中断输出，$\overline{IRQ}$可设置为在状态寄存器0x00改变状态时拉低。读取状态寄存器0x00时，清除$\overline{IRQ}$设置。重复性故障不会影响$\overline{IRQ}$，只能通过读取I²C状态寄存器0x00清除。通过10kΩ上拉电阻接至DVDD，实现满幅输出。
E6	45	JACKSNS	插孔检测，检测插孔的插入和拔出。典型应用中，将JACKSNS连接到插孔的MIC极，参见*插孔检测*部分。
E7	37	INB1	单端线入B1，也是差分线入B的负端。
E8	40	MIC1P/ DIGMICDATA	麦克风1的差分输入正端，串联一个1µF电容对麦克风交流耦合。可重新配置为数字麦克风数据输入。
E9	38	INA2/ EXTMICN	单端线入A2，也可以作为差分线入A的正端或外部麦克风差分输入的负端。
F1	3	DGND	数字地。
F2	2	BCLKS2	S2数字音频的位时钟输入/输出。BCLKS2在IC处于从模式时为输入，在主模式下作为输出。输入/输出电压以DVDDS2为参考。
F3	4	LRCLKS2	S2数字音频左、右声道的时钟输入/输出。LRCLKS2为音频采样率时钟，决定S2音频数据是否送入左声道或右声道。TDM模式下，LRCLKS2为帧同步脉冲。LRCLKS2在IC处于从模式时为输入，在主模式下作为输出。输入/输出电压以DVDDS2为参考。
F4	52	SDA	I²C串行数据输入/输出，通过一个上拉电阻连接到DVDD，实现满幅输出。
F5	51	SCL	I²C串行时钟输入，通过一个上拉电阻连接到DVDD，实现满幅输出。
F6	49	REG	共模电压基准，利用1µF电容旁路至AGND。
F7	44	MICBIAS	低噪声偏置，输出2.2V麦克风偏压。应在MICBIAS和麦克风输出之间安装2.2kΩ电阻。
F8	41	MIC1N/ DIGMICCLK	麦克风1的差分输入负端，串联一个1µF电容对麦克风交流耦合。可重新配置为数字麦克风时钟输出。
F9	39	INA1/ EXTMICP	单端线入A1，也可以作为差分线入A的负端或外部麦克风差分输入的正端。

焊球/引脚说明(续)

焊球 (WLP)	引脚 (TQFN-EP)	名称	功能
G1	1	SDOUTS2	S2数字音频串行数据ADC输出，输出电压以DVDDS2为参考。
G2	55	DVDDS2	S2数字音频接口电源输入，利用一个1µF电容旁路至DGND。
G3	54	SDINS2	S2数字音频串行数据DAC输入，输入电压以DVDDS2为参考。
G4	53	DVDD	数字电源，为数字核心电路和I^2C接口供电。利用一个1µF电容旁路至DGND。
G5	50	AVDD	模拟电源，利用1µF电容旁路至AGND。
G6	48	REF	转换器基准，利用一个2.2µF电容旁路至AGND。
G7	47	AGND	模拟地。
G8	43	MIC2N	麦克风2的差分输入负端，串联一个1µF电容对麦克风交流耦合。
G9	42	MIC2P	麦克风2的差分输入正端，串联一个1µF电容对麦克风交流耦合。
—	—	EP	裸焊盘(TQFN封装)，将裸焊盘连接至PCB接地区域。

详细说明

MAX98089为完全集成的立体声音频编解码器，采用FLEXSOUND技术，内置各种音频放大器。

两个差分麦克风放大器可从三路模拟输入接收信号，一路输入可重新配置用于支持两个数字麦克风。可以同时对两个任意组合的麦克风(模拟或数字)进行录音。将模拟信号放大50dB，由立体声ADC录音。数字录音通路支持语音滤波，提供可选择的高通滤波器，在$f_S/2$处具有较高的阻带衰减。自动增益控制(AGC)电路监测数字转换后的信号，并自动调节模拟麦克风的增益，充分利用ADC的动态范围。噪声门限对低于用户定义门限的信号进行衰减，将ADC噪声输出降至最小。

IC包括两路模拟线入，一路线入可以重新配置成第三路模拟麦克风的输入。两路线入均支持立体声单端输入信号或单声道差分信号。线入信号经过前置放大，然后送入ADC进行录音，并且/或者馈送到输出放大器回放。来自INA1和INA2的单端线入信号可以旁路PGA，并直接连接至ADC输入，以提供最佳动态范围。

集成模拟开关允许两路差分麦克风信号连接到第三路外部设备的麦克风输入。对于两台设备从同一麦克风录制信号的应用，可以省去一个外部模拟开关。

器件通过两个数字音频接口能够以各种格式发送一路立体声音频信号、接收两路立体声音频信号，包括I^2S、PCM及四个单声道时隙的TDM。每个接口均可连接到两个音频端口(S1和S2)之一，与外部设备通信。两个音频接口均支持8kHz至96kHz采样率。每路输入信号均通过5波段参数均衡器分别进行均衡。多波段自动电平控制(ALC)电路可以把信号电平提升12dB。一路附加的信号通路可以支持与ADC通路相同的语音滤波。

IC集成了立体声D类扬声器放大器、高效H类立体声耳机放大器和可配置成单端立体声线出的差分接收放大器。

禁止接收放大器时，模拟开关允许RECP/RXINP和RECN/RXINN重新用于信号切换。系统中，如果一个传感器同时用于扩音器和接收器，外部接收放大器可通过RECP/RXINP和RECN/RXINN连接到左声道扬声器，旁路D类放大器。如果使用内部接收放大器，则将RECP/RXINP和RECN/RXINN浮空。当外部放大器驱动接收器和MAX98089线入时，如果不需要某一路差分信号，可通过模拟开关将其旁路(RECP/RXINP连接至RECN/RXINN)，断开与接收器的连接。

立体声D类放大器为两个扬声器提供高效放大。放大器包括有源辐射抑制电路，有效降低D类放大器的EMI辐射。大多数系统需要利用输出滤波器才能满足EMI的限制指标。

为改善扬声器音质，IC内部集成了抑制失调、失真和功率的相关电路。失调抑制采用动态调节的高通滤波器，截止频率随着响应信号电平的增大而增大。信号较强时，低频能量通常会比有用的音频信号引入更大的失真，对低频信号进行衰减有助于扬声器在没有失真、不损坏的前提下发出更大音量。信号电平相对较弱时，降低滤波器的截止频率，在扬声器的有效工作范围内通过更多的低频能量。输出信号超过预先设置的失真水平时，失真抑制器会降低音量，确保在任何输入信号强度、电池供电电压下，用户都不会听到过大的失真。功率抑制器则对扩音器的连续功率进行监测，如果扬声器存在过热的危险，则立即降低信号电平。

立体声H类耳机放大器采用了双模电荷泵，以获得最高效率。输出以地为参考的信号，从而省去了隔直流电容或者是耳机插孔地回路的中心电压偏置。接地检测可以降低地回路电流引入的输出噪声。

IC集成了插孔检测，允许检测附件的插入和拔出，以及是否按下按钮。

I²C从地址

通过I²C控制总线配置MAX98089，对IC进行写操作时，从地址为0x20或00100000；对IC进行读操作时，从地址为0x21或00100001。详细的接口说明请参考*I²C串口*部分。

寄存器

表1列出了全部寄存器及其地址和上电复位状态，寄存器0x00至0x03和0xFF为只读，其它所有寄存器可读/写。除非另外说明，更新表中任何寄存器时，向未使用的位写入0。

表1. 寄存器

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
STATUS												
Status	CLD	SLD	ULK	—	—	—	JDET	—	0x00	—	R	117
Microphone AGC/NG	NG			AGC					0x01	—	R	74
Jack Status	JKSNS		—	—	—	—	—	—	0x02	—	R	115
Battery Voltage	—	—	—	VBAT					0x03	—	R/W	116
Interrupt Enable	ICLD	ISLD	IULK	0	0	0	IJDET	0	0x0F	0x00	R/W	117
MASTER CLOCK CONTROL												
Master Clock	0	0	PSCLK		0	0	0	0	0x10	0x00	R/W	85
DAI1 CLOCK CONTROL												
Clock Mode	SR1				FREQ1				0x11	0x00	R/W	85, 86
Any Clock Control	PLL1	NI1[14:8]							0x12	0x00	R/W	86
	NI1[7:1]							NI1[0]	0x13	0x00	R/W	86
DAI1 CONFIGURATION												
Format	MAS1	WCI1	BCI1	DLY1	0	TDM1	FSW1	WS1	0x14	0x00	R/W	80
Clock	ADC_OSR1		DAC_ORS1	0	0	BSEL1			0x15	0x00	R/W	81
I/O Configuration	SEL1		LTEN1	LBEN1	DMONO1	HIZOFF1	SDOEN1	SDIEN1	0x16	0x00	R/W	81, 82
Time-Division Multiplex	SLOTL1		SLOTR1		SLOTDLY1				0x17	0x00	R/W	82
Filters	MODE1	AVFLT1			DHF1	DVFLT1			0x18	0x00	R/W	90
DAI2 CLOCK CONTROL												
Clock Mode	SR2				0	0	0	0	0x19	0x00	R/W	85
Any Clock Control	PLL2	NI2[14:8]							0x1A	0x00	R/W	86
	NI2[7:1]							NI2[0]	0x1B	0x00	R/W	86
DAI2 CONFIGURATION												
Format	MAS2	WCI2	BCI2	DLY2	0	TDM2	FSW2	WS2	0x1C	0x00	R/W	80
Clock	0	0	DAC_ ORS2	0	0	BSEL2			0x1D	0x00	R/W	81
I/O Configuration	SEL2		0	LBEN2	DMONO2	HIZOFF2	SDOEN2	SDIEN2	0x1E	0x00	R/W	81, 82

表1. 寄存器(续)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
Time-Division Multiplex	SLOTL2		SLOTR2		SLOTDLY2				0x1F	0x00	R/W	82
Filters	0	0	0	0	DHF2	0	0	DCB2	0x20	0x00	R/W	96
SRC												
Sample Rate Converter	0	0	0	SRMIX_ MODE	SRMIX_ ENL	SRMIX_ ENR	SRC_ ENL	SRC_ ENR	0x21	0x00	R/W	89
MIXERS												
DAC Mixer	MIXDAL				MIXDAR				0x22	0x00	R/W	96
Left ADC Mixer	MIXADL								0x23	0x00	R/W	73
Right ADC Mixer	MIXADR								0x24	0x00	R/W	73
Left Headphone Amplifier Mixer	MIXHPL								0x25	0x00	R/W	110
Right Headphone Amplifier Mixer	MIXHPR								0x26	0x00	R/W	110
Headphone Amplifier Mixer Control	0	0	MIXHPR_ PATHSEL	MIXHPL_ PATHSEL	MIXHPR_GAIN		MIXHPL_GAIN		0x27	0x00	R/W	110
Left Receiver Amplifier Mixer	MIXRECL								0x28	0x00	R/W	98
Right Receiver Amplifier Mixer	MIXRECR								0x29	0x00	R/W	98
Receiver Amplifier Mixer Control	LINE_ MODE	0	0	0	MIXRECR_GAIN		MIXRECL_GAIN		0x2A	0x00	R/W	98
Left Speaker Amplifier Mixer	MIXSPL								0x2B	0x00	R/W	101
Right Speaker Amplifier Mixer	MIXSPR								0x2C	0x00	R/W	101
Speaker Amplifier Mixer Control	0	0	0	0	MIXSPR_GAIN		MIXSPL_GAIN		0x2D	0x00	R/W	101

表1. 寄存器(续)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
LEVEL CONTROL												
Sidetone	DSTS		0	DVST					0x2E	0x00	R/W	78
DAI1 Playback Level	DV1M	0	DV1G		DV1				0x2F	0x00	R/W	95
DAI1 Playback Level	0	0	0	$\overline{EQCLP1}$	DVEQ1				0x30	0x00	R/W	94
DAI2 Playback Level	DV2M	0	0	0	DV2				0x31	0x00	R/W	95
DAI2 Playback Level	0	0	0	$\overline{EQCLP2}$	DVEQ2				0x32	0x00	R/W	94
Left ADC Level	0	0	AVLG		AVL				0x33	0x00	R/W	77
Right ADC Level	0	0	AVRG		AVR				0x34	0x00	R/W	77
Microphone 1 Input Level	0	PA1EN		PGAM1					0x35	0x00	R/W	70
Microphone 2 Input Level	0	PA2EN		PGAM2					0x36	0x00	R/W	70
INA Input Level	0	INAEXT	0	0	0	PGAINA			0x37	0x00	R/W	72
INB Input Level	0	INBEXT	0	0	0	PGAINB			0x38	0x00	R/W	72
Left Headphone Amplifier Volume Control	HPLM	0	0	HPVOLL					0x39	0x00	R/W	111
Right Headphone Amplifier Volume Control	HPRM	0	0	HPVOLR					0x3A	0x00	R/W	111
Left Receiver Amplifier Volume Control	RECLM	0	0	RECVOLL					0x3B	0x00	R/W	99
Right Receiver Amplifier Volume Control	RECRM	0	0	RECVOLR					0x3C	0x00	R/W	99

表1. 寄存器(续)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
Left Speaker Amplifier Volume Control	SPLM	0	0	SPVOLL					0x3D	0x00	R/W	102
Right Speaker Amplifier Volume Control	SPRM	0	0	SPVOLR					0x3E	0x00	R/W	102
MICROPHONE AGC												
Configuration	AGCSRC	AGCRLS			AGCATK		AGCHLD		0x3F	0x00	R/W	74, 75
Threshold	ANTH				AGCTH				0x40	0x00	R/W	75
SPEAKER SIGNAL PROCESSING												
Excursion Limiter Filter	0	DHPUCF			0	0	DHPLCF		0x41	0x00	R/W	104
Excursion Limiter Threshold	0	0	0	0	0	DHPTH			0x42	0x00	R/W	104
ALC	ALCEN	ALCRLS			ALCMB	ALCTH			0x43	0x00	R/W	93, 104
Power Limiter	PWRTH				0	PWRK			0x44	0x00	R/W	105
Power Limiter	PWRT2				PWRT1				0x45	0x00	R/W	106
Distortion Limiter	THDCLP				0	0	0	THDT1	0x46	0x00	R/W	107
CONFIGURATION												
Audio Input	INADIFF	INBDIFF	0	0	0	0	0	0	0x47	0x00	R/W	72
Microphone	MICCLK		DIGMICL	DIGMICR	0	0	EXTMIC		0x48	0x00	R/W	70
Level Control	$\overline{VS2EN}$	$\overline{VSEN}$	$\overline{ZDEN}$	0	0	0	EQ2EN	EQ1EN	0x49	0x00	R/W	94, 113
Bypass Switches	INABYP	0	0	MIC2BYP	0	0	RECBYP	SPKBYP	0x4A	0x00	R/W	71, 112
Jack Detection	JDETEN	0	0	0	0	0	JDEB		0x4B	0x00	R/W	115
POWER MANAGEMENT												
Input Enable	INAEN	INBEN	0	0	MBEN	0	ADLEN	ADREN	0x4C	0x00	R/W	67
Output Enable	HPLEN	HPREN	SPLEN	SPREN	RECLEN	RECREN	DALEN	DAREN	0x4D	0x00	R/W	68
Top-Level Bias Control	BGEN	SPREGEN	VCMEN	BIASEN	0	0	0	JDWK	0x4E	0xF0	R/W	68
DAC Low Power Mode 1	DAI2_DAC_LP				DAI1_DAC_LP				0x4F	0x00	R/W	87
DAC Low Power Mode 2	0	0	0	0	DAC2_IP_DITH_EN	DAC1_IP_DITH_EN	CGM2_EN	CGM1_EN	0x50	0x0F	R/W	87
System Shutdown	$\overline{SHDN}$	VBATEN	0	0	PERFMODE	HPPLYBACK	PWRSV8K	PWRSV	0x51	0x00	R/W	67, 116

表1. 寄存器(续)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
DSP COEFFICIENTS												
EQ Band 1 (DAI1/DAI2)	K_1[15:8]								0x52/0x84	0xXX	R/W	93
	K_1[7:0]								0x53/0x85	0xXX	R/W	93
	K1_1[15:8]								0x54/0x86	0xXX	R/W	93
	K1_1[7:0]								0x55/0x87	0xXX	R/W	93
	K2_1[15:8]								0x56/0x88	0xXX	R/W	93
	K2_1[7:0]								0x57/0x89	0xXX	R/W	93
	c1_1[15:8]								0x58/0x8A	0xXX	R/W	93
	c1_1[7:0]								0x59/0x8B	0xXX	R/W	93
	c2_1[15:8]								0x5A/0x8C	0xXX	R/W	93
	c2_1[7:0]								0x5B/0x8D	0xXX	R/W	93
EQ Band 2 (DAI1/DAI2)	K_2[15:8]								0x5C/0x8E	0xXX	R/W	93
	K_2[7:0]								0x5D/0x8F	0xXX	R/W	93
	K1_2[15:8]								0x5E/0x90	0xXX	R/W	93
	K1_2[7:0]								0x5F/0x91	0xXX	R/W	93
	K2_2[15:8]								0x60/0x92	0xXX	R/W	93
	K2_2[7:0]								0x61/0x93	0xXX	R/W	93
	c1_2[15:8]								0x62/0x94	0xXX	R/W	93
	c1_2[7:0]								0x63/0x95	0xXX	R/W	93
	c2_2[15:8]								0x64/0x96	0xXX	R/W	93
	c2_2[7:0]								0x65/0x97	0xXX	R/W	93
EQ Band 3 (DAI1/DAI2)	K_3[15:8]								0x66/0x98	0xXX	R/W	93
	K_3[7:0]								0x67/0x99	0xXX	R/W	93
	K1_3[15:8]								0x68/0x9A	0xXX	R/W	93
	K1_3[7:0]								0x69/0x9B	0xXX	R/W	93
	K2_3[15:8]								0x6A/0x9C	0xXX	R/W	93
	K2_3[7:0]								0x6B/0x9D	0xXX	R/W	93
	c1_3[15:8]								0x6C/0x9E	0xXX	R/W	93
	c1_3[7:0]								0x6D/0x9F	0xXX	R/W	93
	c2_3[15:8]								0x6E/0xAE	0xXX	R/W	93
	c2_3[7:0]								0x6F/0xA1	0xXX	R/W	93
EQ Band 4 (DAI1/DAI2)	K_4[15:8]								0x70/0xA2	0xXX	R/W	93
	K_4[7:0]								0x71/0xA3	0xXX	R/W	93
	K1_4[15:8]								0x72/0xA4	0xXX	R/W	93
	K1_4[7:0]								0x73/0xA5	0xXX	R/W	93
	K2_4[15:8]								0x74/0xA6	0xXX	R/W	93
	K2_4[7:0]								0x75/0xA7	0xXX	R/W	93
	c1_4[15:8]								0x76/0xA8	0xXX	R/W	93
	c1_4[7:0]								0x77/0xA9	0xXX	R/W	93
	c2_4[15:8]								0x78/0xAA	0xXX	R/W	93
	c2_4[7:0]								0x79/0xAB	0xXX	R/W	93

表1. 寄存器(续)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
EQ Band 5 (DAI1/DAI2)	K_5[15:8]								0x7A/0xAC	0xXX	R/W	93
	K_5[7:0]								0x7B/0xAD	0xXX	R/W	93
	K1_5[15:8]								0x7C/0xAE	0xXX	R/W	93
	K1_5[7:0]								0x7D/0xAF	0xXX	R/W	93
	K2_5[15:8]								0x7E/0xB0	0xXX	R/W	93
	K2_5[7:0]								0x7F/0xB1	0xXX	R/W	93
	c1_5[15:8]								0x80/0xB2	0xXX	R/W	93
	c1_5[7:0]								0x81/0xB3	0xXX	R/W	93
	c2_5[15:8]								0x82/0xB4	0xXX	R/W	93
	c2_5[7:0]								0x83/0xB5	0xXX	R/W	93
Excursion Limiter Biquad (DAI1/DAI2)	a1[15:8]								0xB6/0xC0	0xXX	R/W	93
	a1[7:0]								0xB7/0xC1	0xXX	R/W	93
	a2[15:8]								0xB8/0xC2	0xXX	R/W	93
	a2[7:0]								0xB9/0xC3	0xXX	R/W	93
	b0[15:8]								0xBA/0xC4	0xXX	R/W	93
	b0[7:0]								0xBB/0xC5	0xXX	R/W	93
	b1[15:8]								0xBC/0xC6	0xXX	R/W	93
	b1[7:0]								0xBD/0xC7	0xXX	R/W	93
	b2[15:8]								0xBE/0xC8	0xXX	R/W	93
	b2[7:0]								0xBF/0xC9	0xXX	R/W	93
REVISION ID												
Rev ID	REV								0xFF	0x40	R	118

IC提供全面的电源管理模式，允许禁用任何不使用的电路，将电源电流降至最小。

表2. 电源管理寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x51	7	$\overline{SHDN}$	**Global Shutdown.** Disables everything except the headset detection circuitry, which is controlled separately. 0 = Device Shutdown 1 = Device Enabled
	6	VBATEN	See the *Battery Measurement* section.
	3	PERFMODE	**Performance Mode.** Selects DAC to headphone playback performance mode. 0 = High performance playback mode. 1 = Low power playback mode.
	2	HPPLYBCK	**Headphone Only Playback Mode.** Configures System Bias Control register bits for low power playback when using DAC to headphone playback path only. When enabled, this bit overrides the System Bias Control register settings. When disabled, the System Bias Control register is used to enable system bias blocks. Set both HPPLYBCK and PERFMODE for lowest power consumption when using DAC to headphone playback path only. 0 = Disabled 1 = Enabled
	1	PWRSV8K	**8kHz Power Save Mode.** PWRSV8K configures the ADC for reduced power consumption when f_S = 8kHz. PWRSV8K can be used in conjunction with PWRSV when f_S = 8kHz for more power savings. 0 = Normal, high-performance mode. 1 = Low power mode.
	0	PWRSV	**Power Save Mode.** PWRSV configures the ADC for reduced power consumption for all sample rates. PWRSV can be used in conjunction with PWRSV8K for more power savings. 0 = Normal, high-performance mode. 1 = Low-power mode.
0x4C	7	INAEN	**Line Input A Enable** 0 = Disabled 1 = Enabled
	6	INBEN	**Line Input B Enable** 0 = Disabled 1 = Enabled
	3	MBEN	**Microphone Bias Enable** 0 = Disabled 1 = Enabled
	1	ADLEN	**Left ADC Enable** 0 = Disabled 1 = Enabled
	0	ADREN	**Right ADC Enable** 0 = Disabled 1 = Enabled

表2. 电源管理寄存器(续)

REGISTER	BIT	NAME	DESCRIPTION
0x4D	7	HPLEN	**Left Headphone Enable** 0 = Disabled 1 = Enabled
	6	HPREN	**Right Headphone Enable** 0 = Disabled 1 = Enabled
	5	SPLEN	**Left Speaker Enable** 0 = Disabled 1 = Enabled
	4	SPREN	**Right Speaker Enable** 0 = Disabled 1 = Enabled
	3	RECLEN	**Receiver/Left Line Output Enable.** Use this bit to enable the differential receiver output or left line output. 0 = Disabled 1 = Enabled
	2	RECREN	**Right Line Output Enable.** Use this bit to enable the right line output. 0 = Disabled 1 = Enabled
	1	DALEN	**Left DAC Enable** 0 = Disabled 1 = Enabled
	0	DAREN	**Right DAC Enable** 0 = Disabled 1 = Enabled
0x4E	7	BGEN	**Bandgap Enable.** Must be enabled for proper operation of the 2.5V regulator and associated circuitry. 0 = Disabled 1 = Enabled
	6	SPREGEN	**2.5V Regulator Enable.** SPREGEN enables a 2.5V internal regulator required for the ADC, speaker and receiver/line out amplifier. The 2.5V regulator is powered by SPKLVDD. 0 = Disabled 1 = Enabled
	5	VCMEN	**Common-Mode Voltage Resistor String Enable.** VCMEN enables the common mode voltage for the input and output amplifiers in the codec. 0 = Disabled 1 = Enabled
	4	BIASEN	**Chip Bias Enable.** BIASEN needs to be set for the codec amplifiers to be enabled. 0 = Disabled 1 = Enabled
	0	JDWK	See the *Jack Detection* section.

麦克风输入

器件包括三路差分麦克风输入和用于麦克风供电的低噪声麦克风偏压(图6)。一路麦克风输入也可配置为数字麦克风输入，接收两个数字麦克风的信号。可同时对任意组合的两个麦克风(模拟或数字)进行录音。

典型应用中，一路麦克风输入用于手持麦克风，另一路作为麦克风附件。系统需要利用背景噪声时，INA可以重新配置成另一路麦克风输入。

当编解码器不是唯一的麦克风信号录音装置时，可以将麦克风连接到MIC2P/MIC2N和EXTMICP/EXTMICN。MIC1P/MIC1N成为输出，必要时将麦克风信号连接到外部设备，由两台设备同时录制麦克风的信号，无需外部模拟开关。

模拟麦克风信号经过两级增益放大，然后送入ADC。第一级提供0dB、20dB或30dB增益设置；第二级为可编程增益放大器(PGA)，增益从0dB至20dB可调，步长为1dB。为获得最高的信噪比，尽可能充分利用第一级放大器的增益。PGA提供过零检测功能，从而抑制增益改变时的噪声。

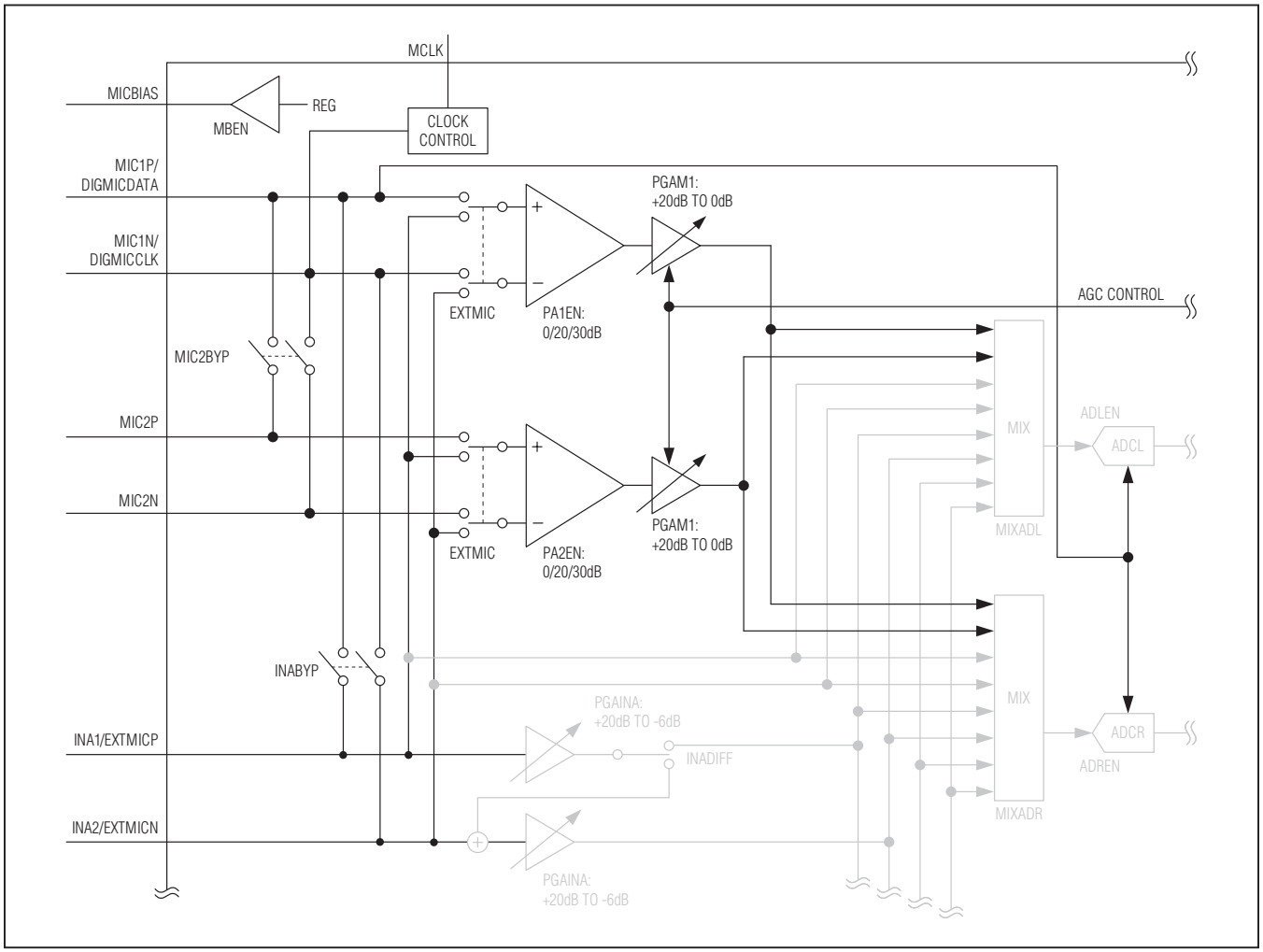


图6. 麦克风输入框图

表3. 麦克风输入寄存器

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="13">0x35/0x36</td><td>6</td><td rowspan="2">PA1EN/PA2EN</td><td colspan="4">MIC1/MIC2 Preamplifier Gain
Course microphone gain adjustment.
00 = Preamplifier disabled
01 = 0dB
10 = 20dB
11 = 30dB</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td><td rowspan="11">PGAM1/PGAM2</td><td colspan="4">MIC1/MIC2 PGA
Fine microphone gain adjustment.</td></tr>
<tr><td rowspan="2">3</td><td>VALUE</td><td>GAIN (dB)</td><td>VALUE</td><td>GAIN (dB)</td></tr>
<tr><td>0x00</td><td>+20</td><td>0x0B</td><td>+9</td></tr>
<tr><td rowspan="2">2</td><td>0x01</td><td>+19</td><td>0x0C</td><td>+8</td></tr>
<tr><td>0x02</td><td>+18</td><td>0x0D</td><td>+7</td></tr>
<tr><td rowspan="2">1</td><td>0x03</td><td>+17</td><td>0x0E</td><td>+6</td></tr>
<tr><td>0x04</td><td>+16</td><td>0x0F</td><td>+5</td></tr>
<tr><td rowspan="2">0</td><td>0x05</td><td>+15</td><td>0x10</td><td>+4</td></tr>
<tr><td>0x06</td><td>+14</td><td>0x11</td><td>+3</td></tr>
<tr><td>0x07</td><td>+13</td><td>0x12</td><td>+2</td></tr>
<tr><td>0x08</td><td>+12</td><td>0x13</td><td>+1</td></tr>
<tr><td>0x09</td><td>+11</td><td>0x14 to 0x1F</td><td>0</td></tr>
<tr><td>0x0A</td><td>+10</td><td colspan="2"></td></tr>
<tr><td rowspan="6">0x48</td><td>7</td><td rowspan="2">MICCLK</td><td colspan="4">Digital Microphone Clock Frequency
Select a frequency that is within the digital microphone’s clock frequency range. Set OSR1 = 1 when using a digital microphone.
00 = PCLK/8
01 = PCLK/6
10 = 64 x LRCLK
11 = Reserved</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td><td>DIGMICL</td><td colspan="4">Left Digital Microphone Enable
Set PA1EN = 00 for proper operation.
0 = Disabled
1 = Enabled</td></tr>
<tr><td>4</td><td>DIGMICR</td><td colspan="4">Right Digital Microphone Enable
Set PA1EN = 00 for proper operation.
0 = Disabled
1 = Enabled</td></tr>
<tr><td>1</td><td rowspan="2">EXTMIC</td><td colspan="4">External Microphone Connection
Routes INA_/EXTMIC_ to the microphone preamplifiers. Set INAEN = 0 when using INA_/EXTMIC_ as a microphone input.
00 = Disabled
01 = MIC1 input
10 = MIC2 input
11 = Reserved</td></tr>
<tr><td>0</td></tr>
</table>

表3. 麦克风输入寄存器(续)

REGISTER	BIT	NAME	DESCRIPTION
0x4A	7	INABYP	**INA_/EXTMIC_ to MIC1_ Bypass Switch** 0 = Disabled 1 = Enabled
	4	MIC2BYP	**MIC1_ to MIC2_ Bypass Switch** 0 = Disabled 1 = Enabled
	1	RECBYP	See the *Output Bypass Switches* section.
	0	SPKBYP	

线入

器件包括两组线入(图7)，每组可配置成立体声单端输入或单声道差分输入。每路输入包括可调增益，以支持各种输入信号的电平。如果需要自定义增益，外部增益模式提供反馈电阻调整。选择适当的输入电阻，利用下式计算增益设置：

$$AV_{PGAIN} = 20 \times \log (20k\Omega/R_{IN})$$

外部增益模式还允许通过多个输入电阻对多路输入信号求和，输入到单个通路(如图8所示)，并且/或者将20kΩ/R_{IN}比值调整到小于1，以允许输入大于1V_{P-P}的信号。

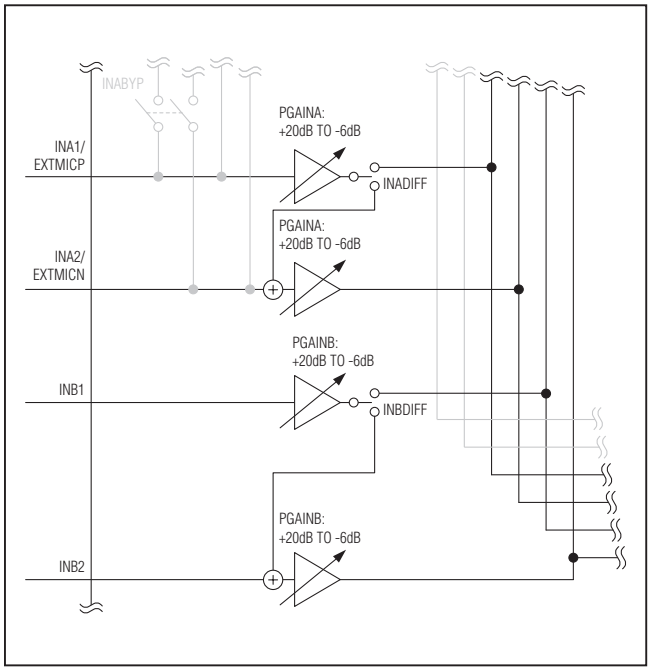


图7. 线入框图

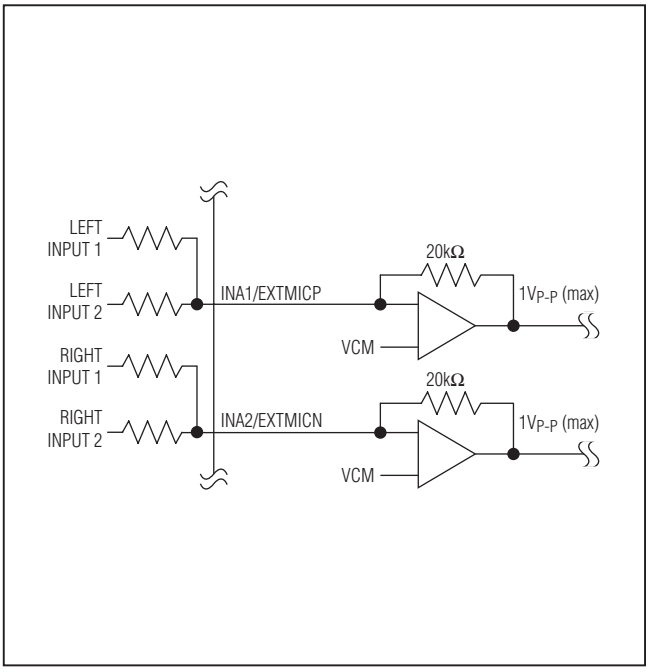


图8. 将多路输入信号求和送至INA/INB

表4. 线入寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x37/0x38	6	INAEXT/INBEXT	**Line Input A/B External Gain** Switches out the internal input resistor and selects a trimmed 20kΩ feedback resistor. Use an external input resistor to set the gain of the line input. 0 = Disabled 1 = Enabled
	2	PGAINA/PGAINB	**Line Input A/B Internal Gain Settings** 000 = +20dB 001 = +14dB 010 = +3dB 011 = 0dB 100 = -3dB 101 = -6dB 110 = -6dB 111 = -6dB
	1		
	0		
0x47	7	INADIFF	**Line Input A Differential Enable** 0 = Stereo single-ended input 1 = Mono differential input
	6	INBDIFF	**Line Input B Differential Enable** 0 = Stereo single-ended input 1 = Mono differential input

ADC输入混音器

IC的立体声ADC接收来自麦克风放大器、线入放大器或直接来自INA1和INA2的输入信号。ADC混音器将八路音频输入的任意组合送入左声道和右声道ADC (图9)。

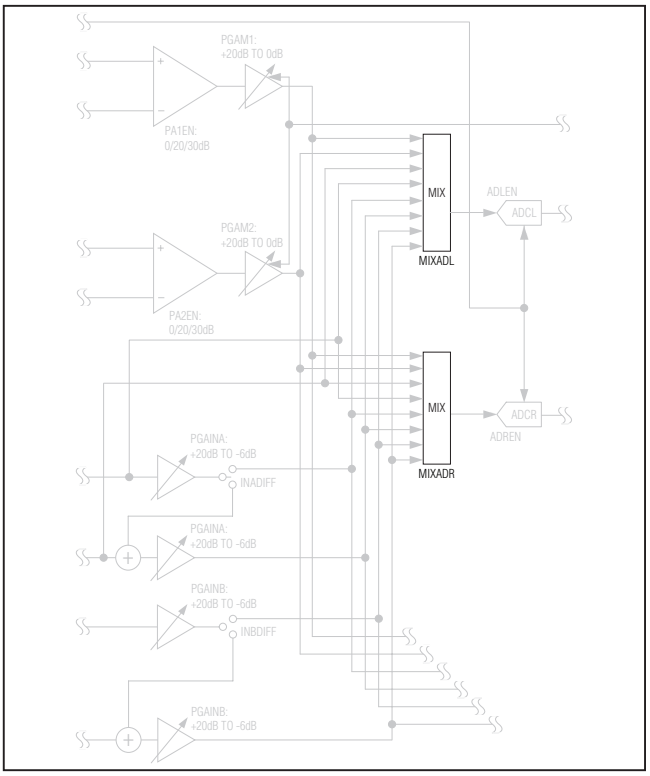


图9. ADC输入混音器框图

表5. ADC输入混音器寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x23/0x24	7	MIXADL/MIXADR	**Left/Right ADC Input Mixer** Selects which analog inputs are recorded by the left/right ADC. 1xxxxxxx = MIC1 x1xxxxxx = MIC2 xx1xxxxx = INA1 pin direct xxx1xxxx = INA2 pin direct xxxx1xxx = INA1 xxxxx1xx = INA2 (INADIFF = 0) or INA2 - INA1 (INADIFF = 1) xxxxxx1x = INB1 xxxxxxx1 = INB2 (INBDIFF = 0) or INB2 - INB1 (INBDIFF = 1)
	6		
	5		
	4		
	3		
	2		
	1		
	0		

录音通路信号处理

器件录音通路包括麦克风输入的自动增益控制器(AGC)和ADC输出端的数字噪声门限(图10)。

麦克风AGC

IC的AGC监测ADC输出信号电平，自动调节MIC1和MIC2模拟PGA设置。信号电平低于预设门限时，提高增益，可以达到最大增益值(20dB)。如果信号超过门限，则减小增益，以防输出信号超出门限。AGC使能时，麦克风PGA不能由用户编程。AGC能够保持更稳定的信号电平，改善ADC的动态范围。

噪声门限

由于AGC放大了所有用户自定义电平以下的信号，使得噪底增大20dB。为了解决这一问题，可以设置噪声门限来减小弱信号的增益。IC内部建立的噪声门限是向下扩展架构，而不是简单地从根本上消除低于规定电平的信号输出。信号每低于噪声门限2dB，器件将对其衰减1dB，最大衰减为12dB。

噪声门限既可以配合AGC使用，也可以独立使用。使能AGC时，噪声门限只有在AGC达到最大增益设置时才开始减小输出电平，图11所示为使用AGC和噪声门限调整时得到的增益响应。

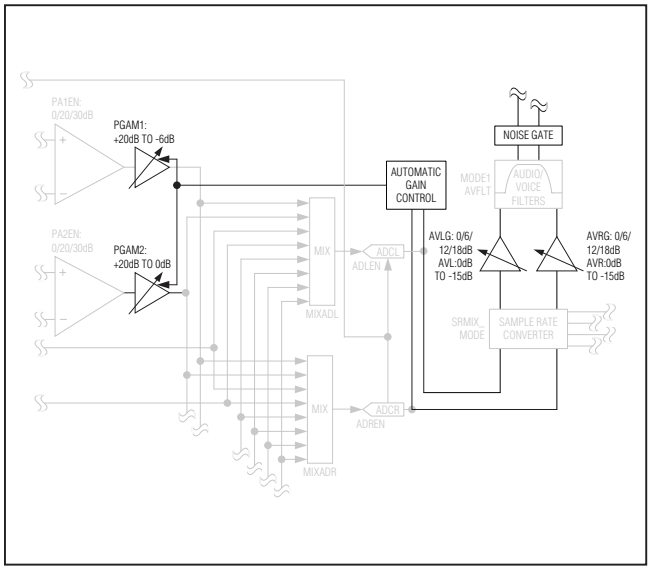


图10. 录音通路信号处理框图

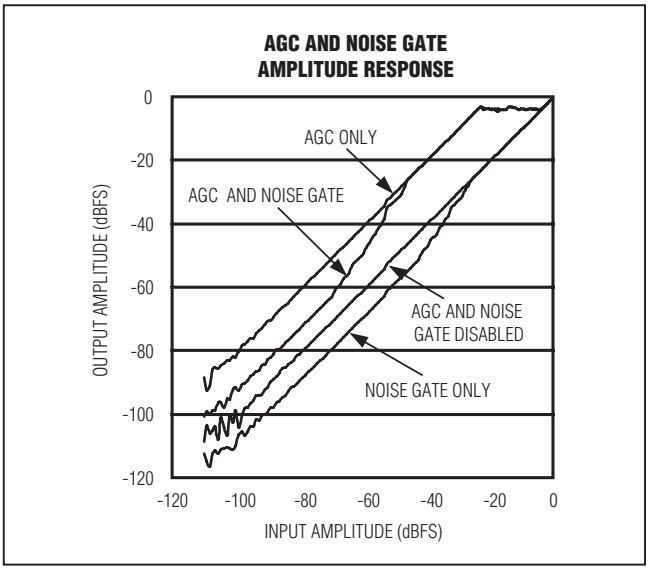


图11. AGC和噪声门限调整电路的输入–输出增益关系

表6. 录音通路信号处理寄存器

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="15">0x01</td><td>7</td><td rowspan="3">NG</td><td colspan="4">Noise Gate Attenuation
Reports the current noise gate attenuation.
000 = 0dB
001 = 1dB
010 = 2dB
011 = 3dB to 5dB
100 = 6dB to 7dB
101 = 8dB to 9dB
110 = 10dB to 11dB
111 = 12dB</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td><td rowspan="12">AGC</td><td colspan="4">AGC Gain
Reports the current AGC gain setting.</td></tr>
<tr><td rowspan="11">3
2
1
0</td><td>VALUE</td><td>GAIN (dB)</td><td>VALUE</td><td>GAIN (dB)</td></tr>
<tr><td>0x00</td><td>+20</td><td>0x0B</td><td>+9</td></tr>
<tr><td>0x01</td><td>+19</td><td>0x0C</td><td>+8</td></tr>
<tr><td>0x02</td><td>+18</td><td>0x0D</td><td>+7</td></tr>
<tr><td>0x03</td><td>+17</td><td>0x0E</td><td>+6</td></tr>
<tr><td>0x04</td><td>+16</td><td>0x0F</td><td>+5</td></tr>
<tr><td>0x05</td><td>+15</td><td>0x10</td><td>+4</td></tr>
<tr><td>0x06</td><td>+14</td><td>0x11</td><td>+3</td></tr>
<tr><td>0x07</td><td>+13</td><td>0x12</td><td>+2</td></tr>
<tr><td>0x08</td><td>+12</td><td>0x13</td><td>+1</td></tr>
<tr><td>0x09</td><td>+11</td><td>0x14 to 0x1F</td><td>0</td></tr>
<tr><td>0x0A</td><td>+10</td><td colspan="2"></td></tr>
<tr><td rowspan="4">0x3F</td><td>7</td><td>AGCSRC</td><td colspan="4">AGC/Noise Gate Signal Source
Determines which ADC channel the AGC and noise gates analyze. Gain is adjusted on both channels regardless of the AGCSRC setting.
0 = Left ADC output
1 = Maximum of either the left or right ADC output</td></tr>
<tr><td>6</td><td rowspan="3">AGCRLS</td><td colspan="4">AGC Release Time
Defined as the duration from start to finish of gain increase in the region shown in Figure 12.
000 = 78ms
001 = 156ms
010 = 312ms
011 = 625ms
100 = 1.25s
101 = 2.5s
110 = 5s
111 = 10s</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td></tr>
</table>

表6. 录音通路信号处理寄存器(续)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="3">0x3F</td><td>3</td><td rowspan="2">AGCATK</td><td rowspan="2">AGC Attack Time
Defined as the time required to reduce gain by 63% of the total gain reduction (one time constant of the exponential response). Attack times are longer for low AGC threshold levels. See Figure 12 for details.
00 = 2ms
01 = 7.2ms
10 = 31ms
11 = 123ms</td></tr>
<tr><td>2</td></tr>
<tr><td>1</td><td rowspan="2">AGCHLD</td><td rowspan="2">AGC Hold Time
The delay before the AGC release begins. The hold time counter starts whenever the signal drops below the AGC threshold and is reset by any signal that exceeds the threshold. Set AGCHLD to enable the AGC circuit. See Figure 12 for details.
00 = AGC disabled
01 = 50ms
10 = 100ms
11 = 400ms</td></tr>
<tr><td>0</td></tr>
<tr><td rowspan="11">0x40</td><td>7</td><td rowspan="5">ANTH</td><td>Noise Gate Threshold
Gain is reduced for signals below the threshold to quiet noise. The thresholds are relative to the ADC's full-scale output voltage.</td></tr>
<tr><td>6</td><td>
<table>
<tr><th>VALUE</th><th>THRESHOLD (dBFS)</th><th>VALUE</th><th>THRESHOLD (dBFS)</th></tr>
<tr><td>0x0</td><td>Noise gate disabled</td><td>0x8</td><td>-45</td></tr>
<tr><td>0x1</td><td>Reserved</td><td>0x9</td><td>-41</td></tr>
<tr><td>0x2</td><td>Reserved</td><td>0xA</td><td>-38</td></tr>
<tr><td>0x3</td><td>-64</td><td>0xB</td><td>-34</td></tr>
<tr><td>0x4</td><td>-62</td><td>0xC</td><td>-30</td></tr>
<tr><td>0x5</td><td>-58</td><td>0xD</td><td>-27</td></tr>
<tr><td>0x6</td><td>-53</td><td>0xE</td><td>-22</td></tr>
<tr><td>0x7</td><td>-50</td><td>0xF</td><td>-16</td></tr>
</table>
</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td></tr>
<tr><td>3</td><td rowspan="5">AGCTH</td><td>AGC Threshold
Gain is reduced when signals exceed the threshold to prevent clipping. The thresholds are relative to the ADC's full-scale voltage.</td></tr>
<tr><td>2</td><td>
<table>
<tr><th>VALUE</th><th>THRESHOLD (dBFS)</th><th>VALUE</th><th>THRESHOLD (dBFS)</th></tr>
<tr><td>0x0</td><td>-3</td><td>0x8</td><td>-11</td></tr>
<tr><td>0x1</td><td>-4</td><td>0x9</td><td>-12</td></tr>
<tr><td>0x2</td><td>-5</td><td>0xA</td><td>-13</td></tr>
<tr><td>0x3</td><td>-6</td><td>0xB</td><td>-14</td></tr>
<tr><td>0x4</td><td>-7</td><td>0xC</td><td>-15</td></tr>
<tr><td>0x5</td><td>-8</td><td>0xD</td><td>-16</td></tr>
<tr><td>0x6</td><td>-9</td><td>0xE</td><td>-17</td></tr>
<tr><td>0x7</td><td>-10</td><td>0xF</td><td>-18</td></tr>
</table>
</td></tr>
<tr><td>1</td></tr>
<tr><td>0</td></tr>
</table>

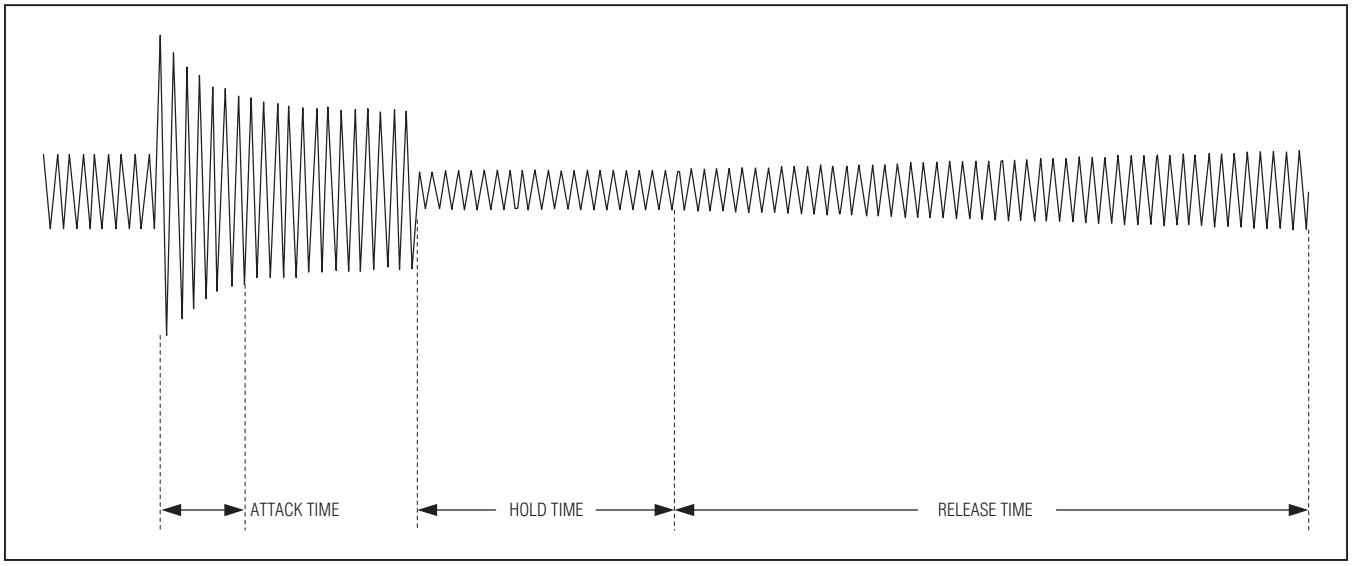


图12. AGC时序图

ADC录音电平控制

IC包括用于左声道和右声道ADC输出的独立数字电平控制(图13)。为了提高动态范围，应尽可能使用模拟增益调节信号电平，并将数字电平控制设置为0dB。数字电平控制主要用于调节数字麦克风的录音电平。

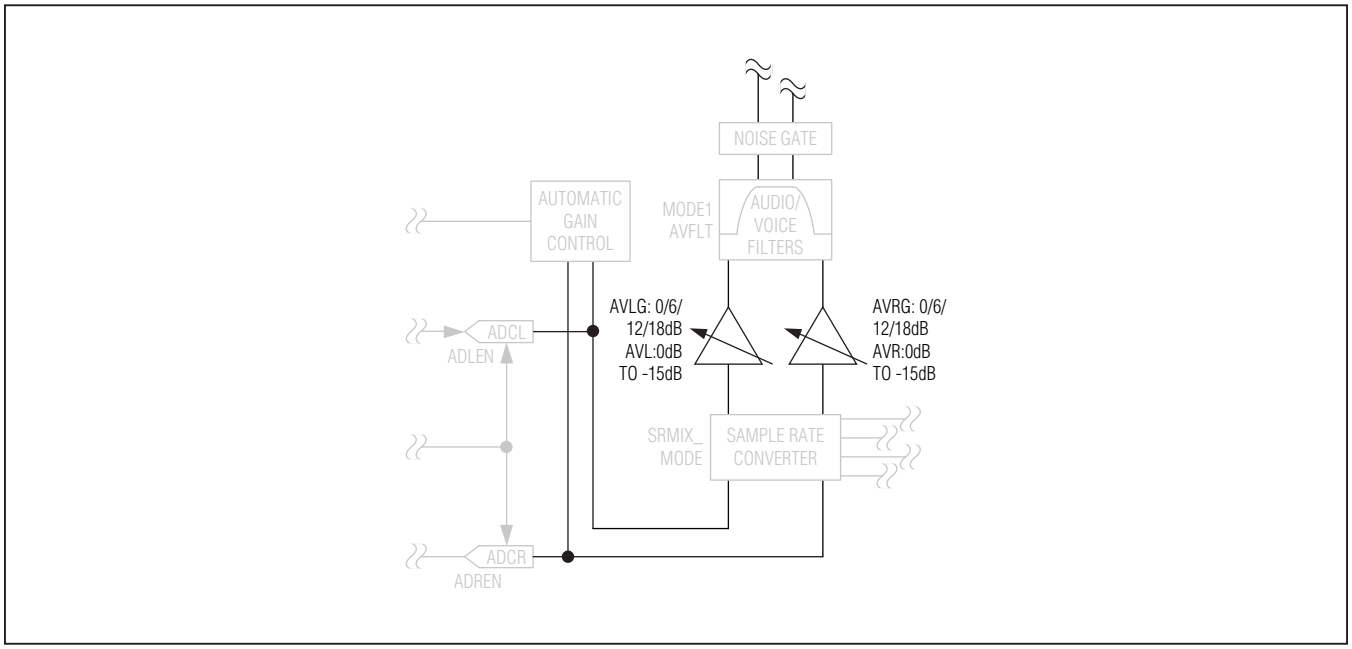


图13. ADC录音电平控制框图

表7. ADC录音电平控制寄存器

REGISTER	BIT	NAME	DESCRIPTION			
0x33/0x34	5	AVLG/AVRG	**Left/Right ADC Gain** 00 = 0dB 01 = 6dB 10 = 12dB 11 = 18dB			
	4					
	3	AVL/AVR	**Left/Right ADC Level**			
			VALUE	**GAIN (dB)**	**VALUE**	**GAIN (dB)**
	2		0x0	+3	0x8	-5
			0x1	+2	0x9	-6
	1		0x2	+1	0xA	-7
			0x3	0	0xB	-8
			0x4	-1	0xC	-9
	0		0x5	-2	0xD	-10
			0x6	-3	0xE	-11
			0x7	-4	0xF	-12

侧音

工作在全双工状态时，使能侧音功能可以在DAI1播放通道所播放的音频信号中增加一个小幅度的录音信号拷贝(图14)。侧音功能通常用于电话通信中，使得讲话者能够听到自己的声音，提供更逼真的用户体验。IC以数字方式实现侧音功能，以避免干扰信号反馈到信号播放通路，也为音频信号播放通路提供更好的匹配。侧音功能仅在语音模式下有效。

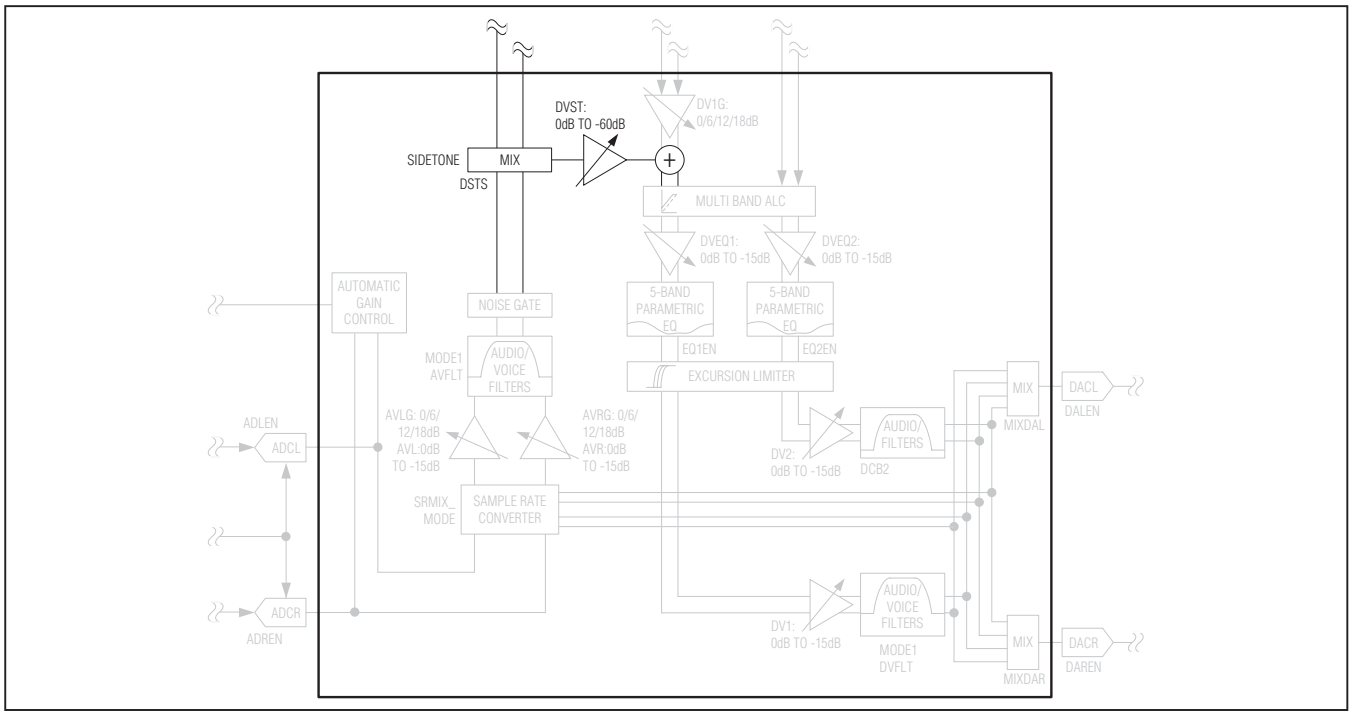


图14. 侧音电路框图

表8. 侧音寄存器

REGISTER	BIT	NAME	DESCRIPTION			
0x2E	7	DSTS	**Sidetone Source** Selects which ADC output is fed back as sidetone. When mixing the left and right ADC outputs, each is attenuated by 6dB to prevent full-scale signals from clipping. 00 = Sidetone disabled 01 = Left ADC 10 = Right ADC 11 = Left + Right ADC			
	6					
	4	DVST	**Sidetone Level** Adjusts the sidetone signal level. All levels are referenced to the ADC's full-scale output.			
			VALUE	**LEVEL (dB)**	**VALUE**	**LEVEL (dB)**
	3		0x00	Sidetone disabled	0x10	-30.5
			0x01	-0.5	0x11	-32.5
			0x02	-2.5	0x12	-34.5
			0x03	-4.5	0x13	-36.5
	2		0x04	-6.5	0x14	-38.5
			0x05	-8.5	0x15	-40.5
			0x06	-10.5	0x16	-42.5
			0x07	-12.5	0x17	-44.5
	1		0x08	-14.5	0x18	-46.5
			0x09	-16.5	0x19	-48.5
			0x0A	-18.5	0x1A	-50.5
			0x0B	-20.5	0x1B	-52.5
	0		0x0C	-22.5	0x1C	-54.5
			0x0D	-24.5	0x1D	-56.6
			0x0E	-26.5	0x1E	-58.5
			0x0F	-28.5	0x1F	-60.5

数字音频接口

IC包括两个独立的回放信号通路和一个录音信号通路。数字音频接口1 (DAI1)用于发送记录的立体声音频信号，接收一路立体声音频信号用于回放。数字音频接口2 (DAI2)用于接收第二路立体声音频信号。将DAI1用于全双工操作和所有语音信号；将DAI2用于音乐及两路播放音频信号的混音。数字音频接口独立于音频端口，以使能连接到任意音频端口的外部设备的通信。

每个音频接口可以配置成不同格式，包括左对齐、I²S、PCM及时分复用(TDM)。TDM模式支持每帧多达4个单声道音频时隙的格式。IC的每个接口可以使用2个单声道时隙，剩余的两个时隙可用于另一器件。表9所示为器件常见的数字音频格式配置，图16和图17给出了常见的音频格式示例。默认设置下，SDOUTS1和SDOUTS2在IC不输出数据时设置为高阻，以便共用总线。将接口配置为仅使用时隙1的TDM模式，用于发送、接收单声道PCM语音数据。

IC的数字音频接口支持ADC至DAC环通和数字环回，环通状态下将ADC转换输出信号连接到DAC，用于回放。信号在数字音频接口从录音通路连接到回放通路，允许使用IC的所有数字信号处理功能。环回状态下，SDINS1或SDINS2输入数据从一个接口连接到另一个接口，分别在SDOUTS2或SDOUTS1输出。两个接口必须配置成相同的采样率，但接口格式不必相同。这允许IC将音频输入从一个接口连接到另一个接口，根据实际需要转换格式，图15所示为可以利用的数字信号连接选项。

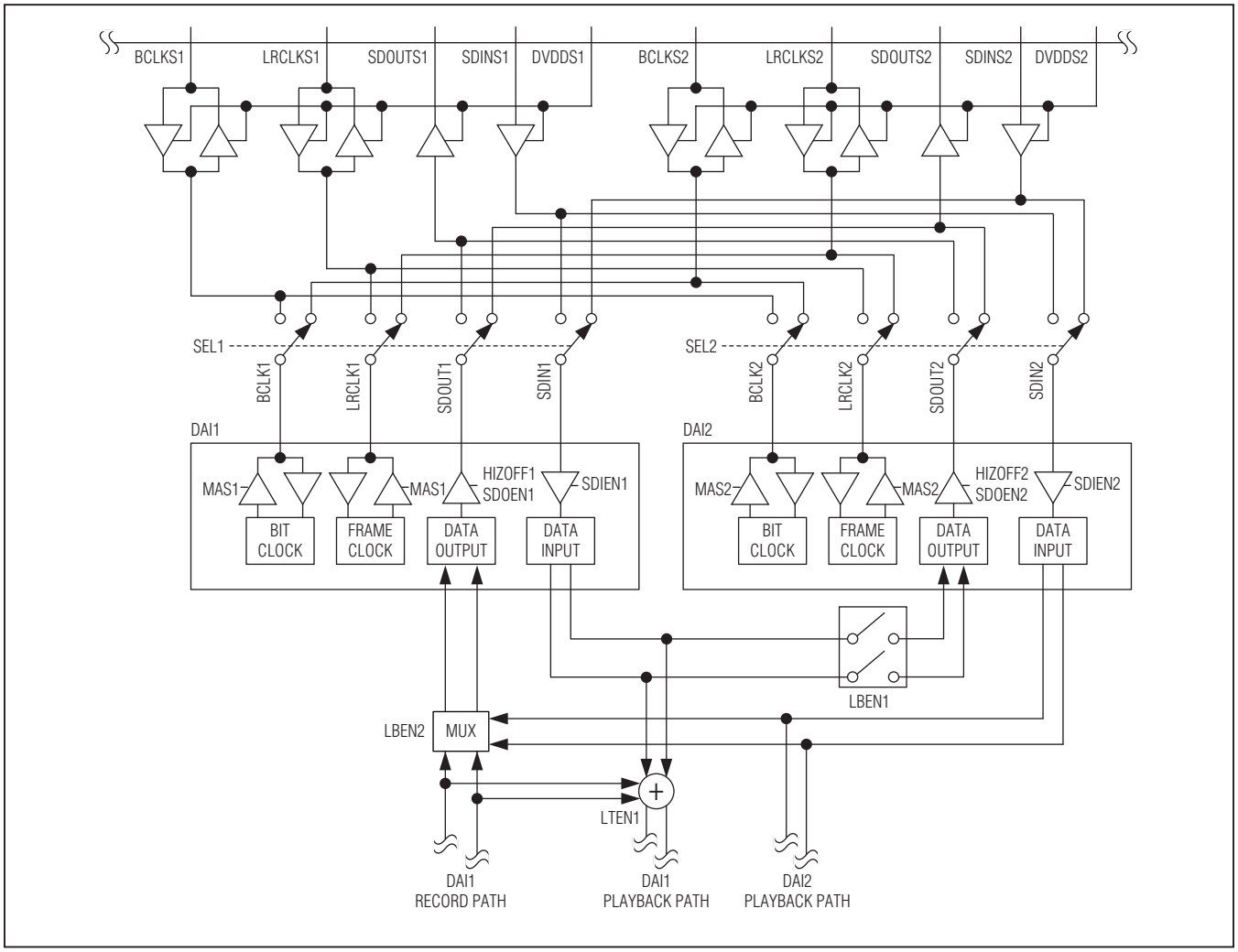


图15. 数字音频信号连接

表9. 常见数字音频格式

MODE	WCI1/WCI2	BCI1/BCI2	DLY1/DLY2	TDM1/TDM2	SLOTL1/SLOTL2	SLOTR1/SLOTR2
Left Justified	1	0	0	0	X	X
I²S	0	0	1	0	X	X
PCM	X	1	X	1	0	0
TDM	X	1	X	1	Set as desired	

X = 无关。

表10. 数字音频接口寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x14/0x1C	7	MAS1/MAS2	**DAI1/DAI2 Master Mode** In master mode, DAI1/DAI2 outputs LRCLK and BCLK. In slave mode, DAI1/DAI2 accept LRCLK and BCLK as inputs. 0 = Slave mode 1 = Master mode
	6	WCI1/WCI2	**DAI1/DAI2 Word Clock Invert** TDM1/TDM2 = 0: 0 = Left-channel data is transmitted while LRCLK is low. 1 = Right-channel data is transmitted while LRCLK is low. TDM1/TDM2 = 1: Always set WCI = 0.
	5	BCI1/BCI2	**DAI1/DAI2 Bit Clock Invert** BCI1/BCI2 must be set to 1 when TDM1/TDM2 = 1. 0 = SDIN is accepted on the rising edge of BCLK. SDOUT is valid on the rising edge of BCLK. 1 = SDIN is accepted on the falling edge of BCLK. SDOUT is valid on the falling edge of BCLK. Master Mode: 0 = LRCLK transitions on the falling edge of BCLK. 1 = LRCLK transitions on the rising edge of BCLK.
	4	DLY1/DLY2	**DAI1/DAI2 Data Delay** DLY1/DLY2 has no effect when TDM1/TDM2 = 1. 0 = The most significant data bit is clocked on the first active BCLK edge after an LRCLK transition. 1 = The most significant data bit is clocked on the second active BCLK edge after an LRCLK transition.
	2	TDM1/TDM2	**DAI1/DAI2 Time-Division Multiplex Mode (TDM Mode)** Set TDM1/TDM2 when communicating with devices that use a frame synchronization pulse on LRCLK instead of a square wave. 0 = Disabled 1 = Enabled (BCI1/BCI2 must be set to 1)
	1	FSW1/FSW2	**DAI1/DAI2 Wide Frame Sync Pulse** Increases the width of the frame sync pulse to the full data width when TDM1/TDM2 = 1. FSW1/FSW2 has no effect when TDM1/TDM2 = 0. 0 = Disabled 1 = Enabled
	0	WS1/WS2	**DAI1/DAI2 Audio Data Bit Depth** Determines the maximum bit depth of audio being transmitted and received. Data is always 16 bit when TDM1/TMD2 = 0. 0 = 16 bits 1 = 24 bits

表10. 数字音频接口寄存器(续)

REGISTER	BIT	NAME	DESCRIPTION
0x15/0x1D	7	OSR1	**ADC Oversampling Ratio** Use the higher setting for maximum performance. Use the lower setting for reduced power consumption at the expense of performance. 00 = 96x 01 = 64x 10 = Reserved 11 = Reserved
	6		
	5	DAC_OSR1/ DAC_OSR2	**DAC Oversample Clock (Select PCLK/2 for higher performance. Select PCLK/4 for lower power consumption.)** 1 = DAC input clock = PCLK/2 0 = DAC input clock = PCLK/4
	2	BSEL1/ BSEL2	**DAI1/DAI2 BCLK Output Frequency** When operating in master mode, BSEL1/BSEL2 set the frequency of BCLK. When operating in slave mode, BSEL1/BSEL2 have no effect. Select the lowest BCLK frequency that clocks all data input to the DAC and output by the ADC. 000 = BCLK disabled 001 = 64 x LRCLK 010 = 48 x LRCLK 011 = 128 x LRCLK (invalid for DHF1/DHF2 = 1) 100 = PCLK/2 101 = PCLK/4 110 = PCLK/8 111 = PCLK/16
	1		
	0		
0x16/0x1E	7	SEL1/SEL2	**DAI1/DAI2 Audio Port Selector** Selects which port is used by DAI1/DAI2. 00 = None 01 = Port S1 10 = Port S2 11 = Reserved
	6		
	5	LTEN1	**DAI1 Digital Loopthrough** Connects the output of the record signal path to the input of the playback path. Data input to DAI1 from an external device is mixed with the recorded audio signal. 0 = Disabled 1 = Enabled
	4	LBEN1/ LBEN2	**DAI1/DAI2 Digital Audio Interface Loopback** LBEN1 routes the digital audio input to DAI1 back out on DAI2. LBEN2 routes the digital audio input to DAI2 back out on DAI1. Selecting LBEN2 disables the ADC output data. 0 = Disabled 1 = Enabled
	3	DMONO1/ DMONO2	**DAI1/DAI2 DAC Mono Mix** Mixes the left and right digital input to mono and routes the combined signal to the left and right playback paths. The left and right input data is attenuated by 6dB prior to the mono mix. 0 = Disabled 1 = Enabled

表10. 数字音频接口寄存器(续)

REGISTER	BIT	NAME	DESCRIPTION
0x16/0x1E	2	HIZOFF1/ HIZOFF2	**Disable DA1/DAI2 Output High-Impedance Mode** Normally SDOUT is set high impedance between data words. Set HIZOFF1/HIZOFF2 to force a level on SDOUT at all times. 0 = Disabled 1 = Enabled
	1	SDOEN1/ SDOEN2	**DAI1/DAI2 Record Path Output Enable** DAI2 outputs data only if LBEN1 = 1. 0 = Disabled 1 = Enabled
	0	SDIEN1/ SDIEN2	**DAI1/DAI2 Playback Path Input Enable** 0 = Disabled 1 = Enabled
0x17/0x1F	7 6	SLOTL1/ SLOTL2	**TDM Left Time Slot** Selects which of the four slots is used for left data on DAI1/DAI2. If the same slot is selected for left and right audio, left audio is placed in the slot. 00 = Slot 1 01 = Slot 2 10 = Slot 3 11 = Slot 4
	5 4	SLOTR1/ SLOTR2	**TDM Right Time Slot** Selects which of the four slots is used for right data on DAI1/DAI2. If the same slot is selected for left and right audio, left audio is placed in the slot. 00 = Slot 1 01 = Slot 2 10 = Slot 3 11 = Slot 4
	3 2 1 0	SLOTDLY1/ SLOTDLY2	**TDM Slot Delay** Adds 1 BCLK cycle delay to the data in the specified TDM slot. 1xxx = Slot 4 delayed x1xx = Slot 3 delayed xx1x = Slot 2 delayed xxx1 = Slot 1 delayed

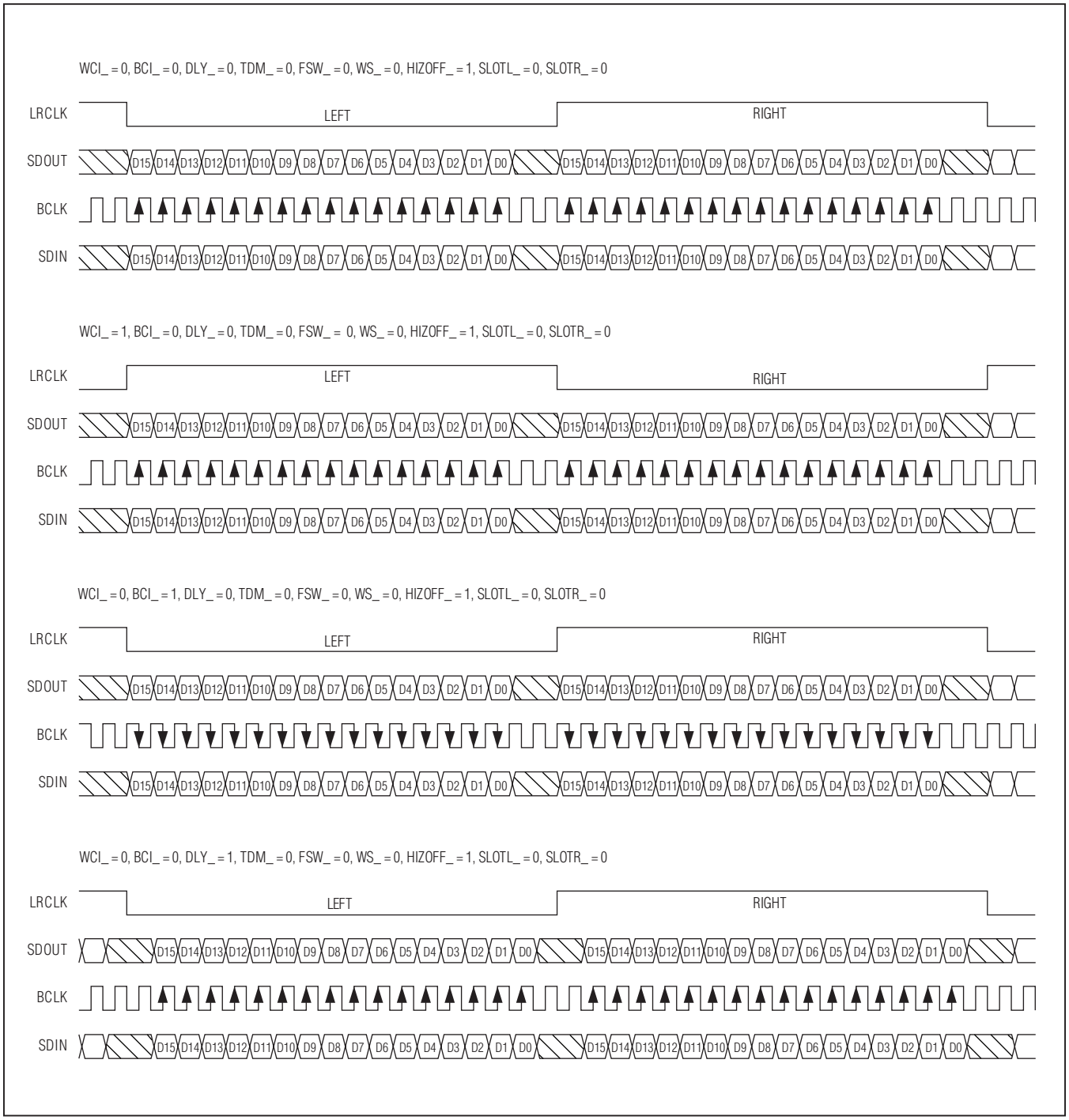


图16. Non–TDM数据格式示例

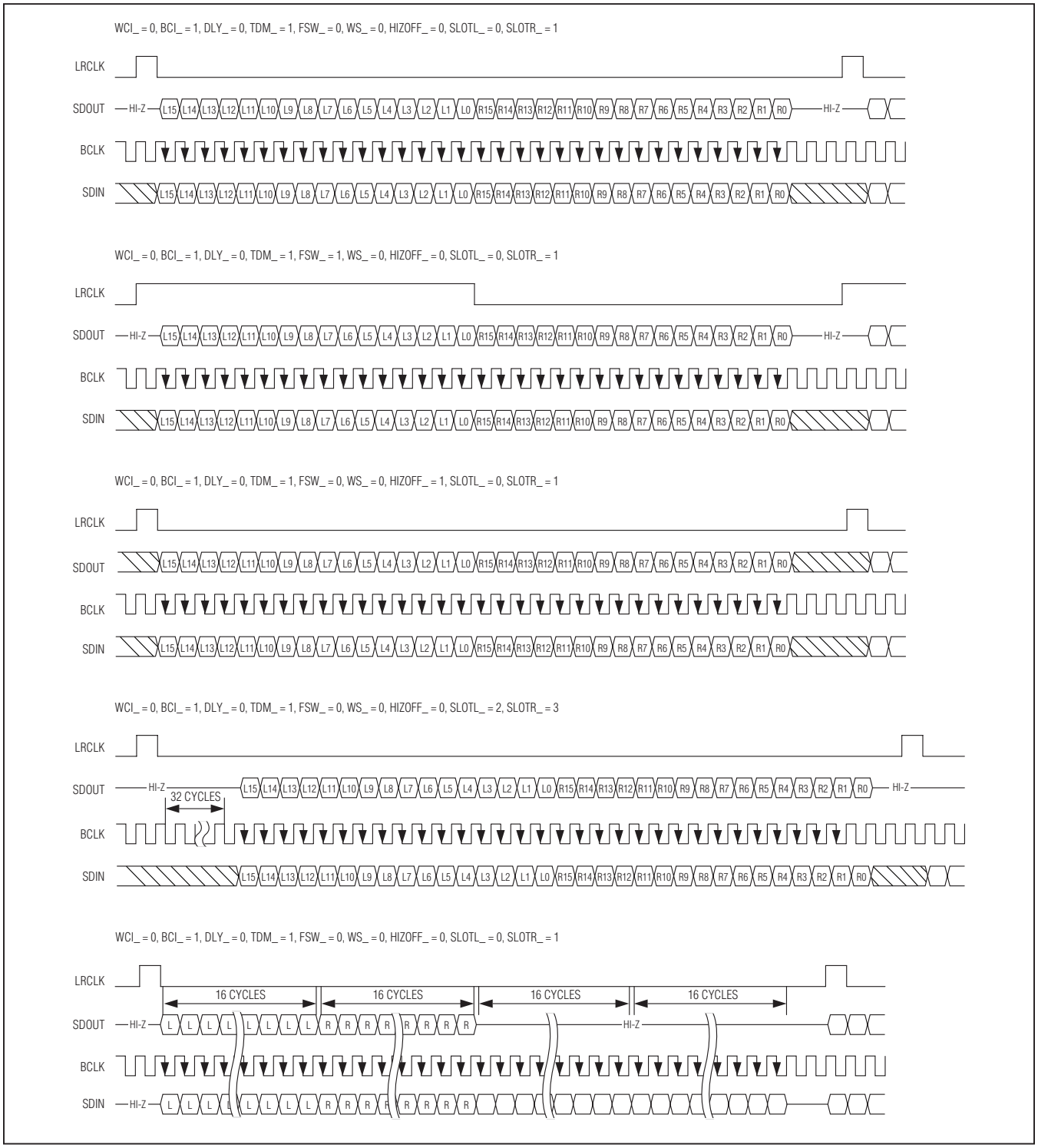


图17. TDM模式数据格式示例

时钟控制

IC中的数字信号通路需要10MHz至60MHz的主控时钟(MCLK)才能工作。MAX98089需要10MHz至20MHz的内部时钟，预分频器对MCLK进行1、2或4分频，产生内部时钟(PCLK)。PCLK为IC的各部分电路提供时钟。

MAX98089包括两个数字音频信号通路，均支持8kHz至96kHz的采样速率。每一通路独立配置，允许工作在不同的采样率。为了满足各种系统架构，支持四种主时钟模式：

- **PLL模式：**器件工作在从模式时，使能PLL使器件锁定至任意LRCLK输入。该模式下需要的配置最少，但能够支持的性能也最低。为了简化初始设置，或者不能使用常规工作模式和整数模式时，可以采用这一模式。
- **常规模式：**该模式下提供一个15位的时钟分频器，用于设置相对于PCLK的采样率，从而使PCLK和LRCLK频率具有高度灵活性，并可用于主模式和从模式。
- **整数模式(仅限DAI1)：**器件工作在主模式或从模式时，对于8kHz和16kHz采样率，常见的MCLK频率(12MHz、13MHz、16MHz和19.2MHz)可编程工作在精确的整数模式。该模式下，MCLK和LRCLK速率通过FREQ1位选择，而非使用NI和PLL控制位。
- **DAC低功耗模式：**该模式旁路PLL，以降低功耗，并使用固定计数器产生时钟。DAI__DAC_LP位将覆盖其它时钟设置。

表11. 时钟控制寄存器

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="2">0x10</td><td>5</td><td rowspan="2">PSCLK</td><td colspan="4">MCLK Prescaler
Generates PCLK, which is used by all internal circuitry.
00 = PCLK disabled
01 = 10MHz ≤ MCLK ≤ 20MHz (PCLK = MCLK)
10 = 20MHz ≤ MCLK ≤ 40MHz (PCLK = MCLK/2)
11 = 40MHz ≤ MCLK ≤ 60MHz (PCLK = MCLK/4)</td></tr>
<tr><td>4</td></tr>
<tr><td rowspan="11">0x11/0x19</td><td>7</td><td rowspan="11">SR1/SR2</td><td colspan="4">DAI1/DAI2 Sample Rate
Used by the ALC to correctly set the dual-band crossover frequency and the excursion limiter to set the predefined corner frequencies.</td></tr>
<tr><td rowspan="2">6</td><td>VALUE</td><td>SAMPLE RATE (kHz)</td><td>VALUE</td><td>SAMPLE RATE (kHz)</td></tr>
<tr><td>0x0</td><td>Reserved</td><td>0x8</td><td>48</td></tr>
<tr><td rowspan="3">5</td><td>0x1</td><td>8</td><td>0x9</td><td>88.2</td></tr>
<tr><td>0x2</td><td>11.025</td><td>0xA</td><td>96</td></tr>
<tr><td>0x3</td><td>16</td><td>0xB</td><td>Reserved</td></tr>
<tr><td rowspan="4">4</td><td>0x4</td><td>22.05</td><td>0xC</td><td>Reserved</td></tr>
<tr><td>0x5</td><td>24</td><td>0xD</td><td>Reserved</td></tr>
<tr><td>0x6</td><td>32</td><td>0xE</td><td>Reserved</td></tr>
<tr><td>0x7</td><td>44.1</td><td>0xF</td><td>Reserved</td></tr>
</table>

表11. 时钟控制寄存器(续)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="10">0x11</td><td rowspan="3">3</td><td rowspan="10">FREQ1</td><td colspan="3">Exact Integer Mode
Overrides PLL1 and NI1 and configures a specific PCLK to LRCLK ratio.</td></tr>
<tr><td>VALUE</td><td>SAMPLE RATE</td><td>VALUE</td><td>SAMPLE RATE</td></tr>
<tr><td>0x0</td><td>Disabled</td><td>0x8</td><td>PCLK = 12MHz,
LRCLK = 8kHz</td></tr>
<tr><td rowspan="4">2</td><td>0x1</td><td>Reserved</td><td>0x9</td><td>PCLK = 12MHz,
LRCLK = 16kHz</td></tr>
<tr><td>0x2</td><td>Reserved</td><td>0xA</td><td>PCLK = 13MHz,
LRCLK = 8kHz</td></tr>
<tr><td>0x3</td><td>Reserved</td><td>0xB</td><td>PCLK = 13MHz,
LRCLK = 16kHz</td></tr>
<tr><td>0x4</td><td>Reserved</td><td>0xC</td><td>PCLK = 16MHz,
LRCLK = 8kHz</td></tr>
<tr><td rowspan="3">1</td><td>0x5</td><td>Reserved</td><td>0xD</td><td>PCLK = 16MHz,
LRCLK = 16kHz</td></tr>
<tr><td>0x6</td><td>Reserved</td><td>0xE</td><td>PCLK = 19.2MHz,
LRCLK = 8kHz</td></tr>
<tr><td>0x7</td><td>Reserved</td><td>0xF</td><td>PCLK = 19.2MHz,
LRCLK = 16kHz</td></tr>
<tr><td rowspan="8">0x12/0x1A</td><td>7</td><td>PLL1/PLL2</td><td colspan="3">PLL Mode Enable (Slave Mode Only)
PLL1/PLL2 enables a digital PLL that locks on to the externally supplied LRCLK frequency and automatically sets the LRCLK divider (NI1/NI2).
0 = Disabled
1 = Enabled</td></tr>
<tr><td>6</td><td rowspan="16">NI1/
NI2</td><td colspan="3" rowspan="2">Normal Mode LRCLK Divider
When PLL1/PLL2 = 0, the frequency of LRCLK is determined by NI1/NI2. See Table 12 for common NI values.</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td><td>SAMPLE RATE</td><td>DHF1/DHF2</td><td>NI1/NI2 FORMULA</td></tr>
<tr><td>3</td><td rowspan="2">8kHz ≤ LRCLK ≤ 48kHz</td><td rowspan="2">0</td><td rowspan="2">$NI = \frac{65{,}536 \times 96 \times f_{LRCLK}}{f_{PCLK}}$</td></tr>
<tr><td>2</td></tr>
<tr><td>1</td><td rowspan="2">48kHz < LRCLK ≤ 96kHz</td><td rowspan="2">1</td><td rowspan="2">$NI = \frac{65{,}536 \times 48 \times f_{LRCLK}}{f_{PCLK}}$</td></tr>
<tr><td>0</td></tr>
<tr><td rowspan="8">0x13/0x1B</td><td>7</td><td colspan="3" rowspan="2">f_{LRCLK} = LRCLK frequency
f_{PCLK} = Prescaled MCLK frequency (PCLK)</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td><td colspan="3" rowspan="2"></td></tr>
<tr><td>4</td></tr>
<tr><td>3</td><td colspan="3" rowspan="2"></td></tr>
<tr><td>2</td></tr>
<tr><td>1</td><td colspan="3" rowspan="2"></td></tr>
<tr><td>0</td><td>NI1[0]/NI2[0]</td><td colspan="3">Rapid Lock Mode
Program NI1/NI2 to the nearest valid ratio and set NI1[0]/NI2[0] when PLL1/PLL2 = 1 to enable rapid lock mode. Normally, the PLL automatically calculates and dynamically adjusts NI1/NI2. When rapid lock mode is properly configured, the PLL starting point is much closer to the correct value, thus speeding up lock time. Wait one LRCLK period after programming NI1/NI2 before setting PLL1/PLL2 = 1.</td></tr>
</table>

表11. 时钟控制寄存器(续)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="6">DESCRIPTION</th></tr>
<tr><td rowspan="10">0x4F</td><td>7</td><td rowspan="4">DAI2_DAC_LP</td><td colspan="6">DAI_ DAC Low Power Select.
These bits setup the clocks to be generated from fixed counters that bypass the PLL for DAC low power mode.</td></tr>
<tr><td rowspan="2">6</td><td>VALUE</td><td>SETTING</td><td>FILTER SELECT</td><td>VALUE</td><td>SETTING</td><td>FILTER SELECT</td></tr>
<tr><td>0x0</td><td>PLL derived clock</td><td>—</td><td>0x8</td><td>PCLK = 2304 x LRCLK</td><td>Voice</td></tr>
<tr><td>5</td><td>0x1</td><td>PCLK = 128 x LRCLK</td><td>Audio 96kHz</td><td>0x9</td><td>Reserved</td><td>—</td></tr>
<tr><td>4</td><td>0x2</td><td>PCLK = 192 x LRCLK</td><td>Audio 96kHz</td><td>0xA</td><td>Reserved</td><td>—</td></tr>
<tr><td rowspan="2">3</td><td rowspan="5">DAI1_DAC_LP</td><td>0x3</td><td>PCLK = 256 x LRCLK</td><td>Audio 48kHz</td><td>0xB</td><td>Reserved</td><td>—</td></tr>
<tr><td>0x4</td><td>PCLK = 384 x LRCLK</td><td>Audio 48kHz</td><td>0xC</td><td>Reserved</td><td>—</td></tr>
<tr><td>2</td><td>0x5</td><td>PCLK = 768 x LRCLK</td><td>Voice</td><td>0xD</td><td>Reserved</td><td>—</td></tr>
<tr><td>1</td><td>0x6</td><td>PCLK = 1152 x LRCLK</td><td>Voice</td><td>0xE</td><td>Reserved</td><td>—</td></tr>
<tr><td>0</td><td>0x7</td><td>PCLK = 1536 x LRCLK</td><td>Voice</td><td>0xF</td><td>Reserved</td><td>—</td></tr>
<tr><td rowspan="4">0x50</td><td>3</td><td>DAC2DITHEN</td><td colspan="6">DAI2 DAC Input Dither Enable
DAC2DITHEN is recommended to be set when DAI2_DAC_LP = 0000.
0 = Disabled
1 = Enabled</td></tr>
<tr><td>2</td><td>DAC1DITHEN</td><td colspan="6">DAI1 DAC Input Dither 1 Enable
DAC1DITHEN is recommended to be set when DAI1_DAC_LP = 0000.
0 = Disabled
1 = Enabled</td></tr>
<tr><td>1</td><td>CGM2_EN</td><td colspan="6">DAI2 Clock Gen Module Enable
CGM1_EN has to be set along with CGM2_EN to enable the clock generation for the DAI2 DAC playback path.
0 = Disabled
1 = Enabled</td></tr>
<tr><td>0</td><td>CGM1_EN</td><td colspan="6">DAI1/Device Clock Gen Module Enable
CGM1_EN enables the device clock generation, and needs to be set for DAC playback or ADC record.
0 = Disabled
1 = Enabled</td></tr>
</table>

表12. 常见的NI1/NI2值

PCLK (MHz)	LRCLK (kHz)											
	DHF1/2 = 0									DHF1/2 = 1		
	8	11.025	12	16	22.05	24	32	44.1	48	64	88.2	96
10	13A9	1B18	1D7E	2752	3631	3AFB	4EA5	6C61	75F7	4EA5	6C61	75F7
11	11E0	18A2	1ACF	23BF	3144	359F	477E	6287	6B3E	477E	6287	6B3E
11.2896	116A	**1800**	1A1F	22D4	**3000**	343F	45A9	**6000**	687D	45A9	**6000**	687D
12	1062	1694	1893	20C5	2D29	3127	4189	5A51	624E	4189	5A51	624E
12.288	**1000**	160D	**1800**	**2000**	2C1A	**3000**	**4000**	5833	**6000**	**4000**	5833	**6000**
13	0F20	14D8	16AF	1E3F	29AF	2D5F	3C7F	535F	5ABE	3C7F	535F	5ABE
16	0C4A	10EF	126F	1893	21DE	24DD	3127	43BD	49BA	3127	43BD	49BA
16.9344	0B9C	**1000**	116A	1738	**2000**	22D4	2E71	**4000**	45A9	2E71	**4000**	45A9
18.432	0AAB	0EB3	**1000**	1555	1D66	**2000**	2AAB	3ACD	**4000**	2AAB	3ACD	**4000**
20	09D5	0D8C	0EBF	13A9	1B18	1D7E	2752	3631	3AFB	2752	3631	3AFB

注：*用粗体表示的整数值可提供满负荷操作。*

采样率转换器

采样率转换电路用于DAI1 (SDIN1)和DAI2 (SDIN2)异步音频数据的采样率转换和混音。所得到的音频信号可通过DAI1输出到SDOUTS1或SDOUTS2。可按声道使能采样率转换，允许DAI1的一个声道输出麦克风数据，而另一个声道输出采样率转换后的数据。

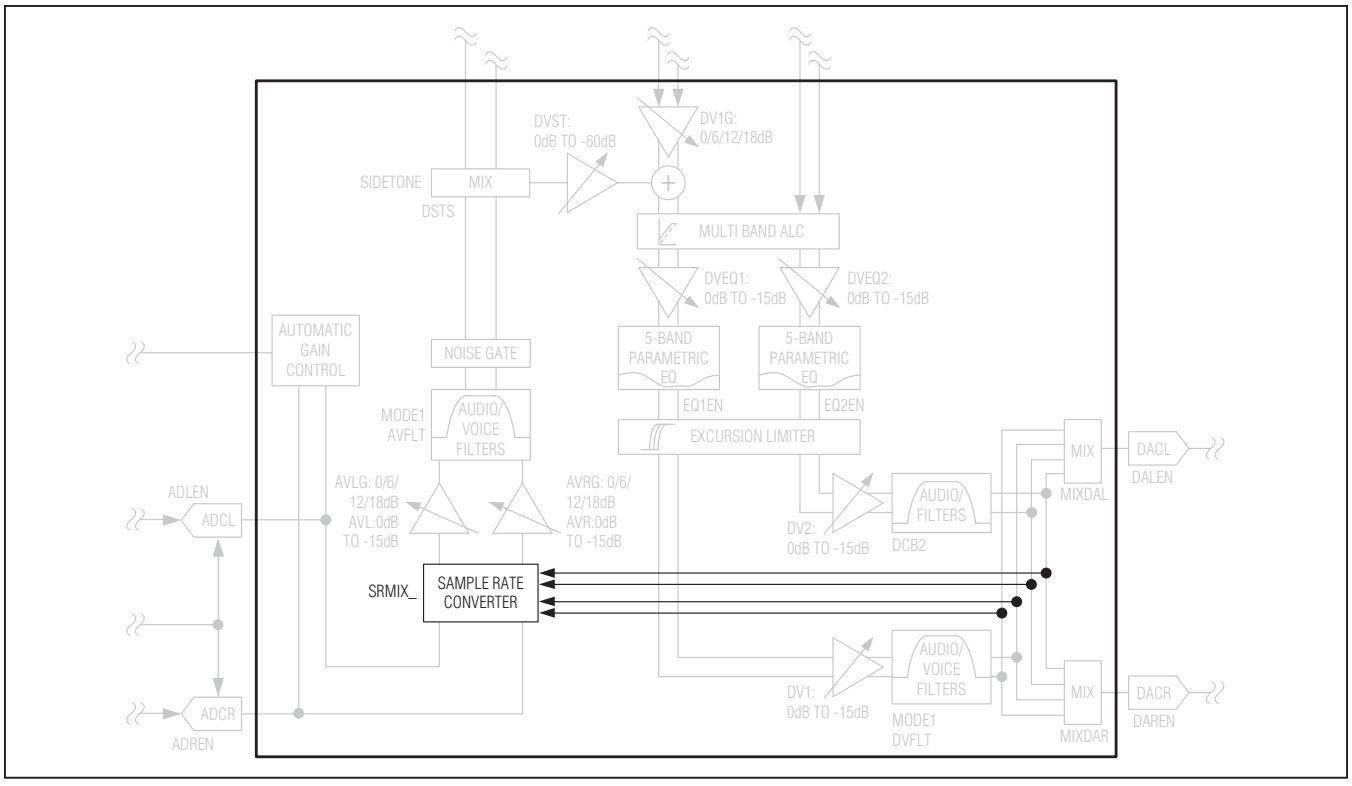


图18. 采样率转换器

表13. 采样率转换器寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x21	4	SRMIX_MODE	**Sample Rate Mix Mode.** Sets mixing configuration applied to the sample rate converted channel(s). 0 = (DAI1 + DAI2) 1 = (DAI1 + DAI2)/2
	3	SRMIX_ENL	**Sample Rate Mix Enable.** If enabled, mixes data on DAI1 and DAI2. If cleared, SRC data source is DAI2 only. 0 = SRC mix disable 1 = SRC mix enable
	2	SRMIX_ENR	
	1	SRC_ENL	**Sample Rate Converter Enable.** Select if the SRC is enabled on a per channel basis. 0 = Sample rate converter disable 1 = Sample rate converter enable
	0	SRC_ENR	

通带滤波

IC中的每个数字信号通路均包含用于定义通路带宽的选项(图19)，连接到DAI1的回放和录音通路支持语音和音乐滤波，连接在DAI2的回放通路仅支持音乐滤波。

语音IIR滤波器对于$f_S/2$以上的频率提供大于70dB的阻带衰减，以减小混叠。三个可选的高通滤波器消除了低频干扰信号。

处理高保真音频内容时采用音乐模式，音乐FIR滤波器采用低功耗设计，并具有线性相位，以维持立体声相位。可选择隔直流滤波器，以滤除直流失调。

音乐模式下，第二组FIR滤波器用于支持50kHz以上的采样率。DAI1和DAI2可独立选择滤波器，并支持回放和录音通路。

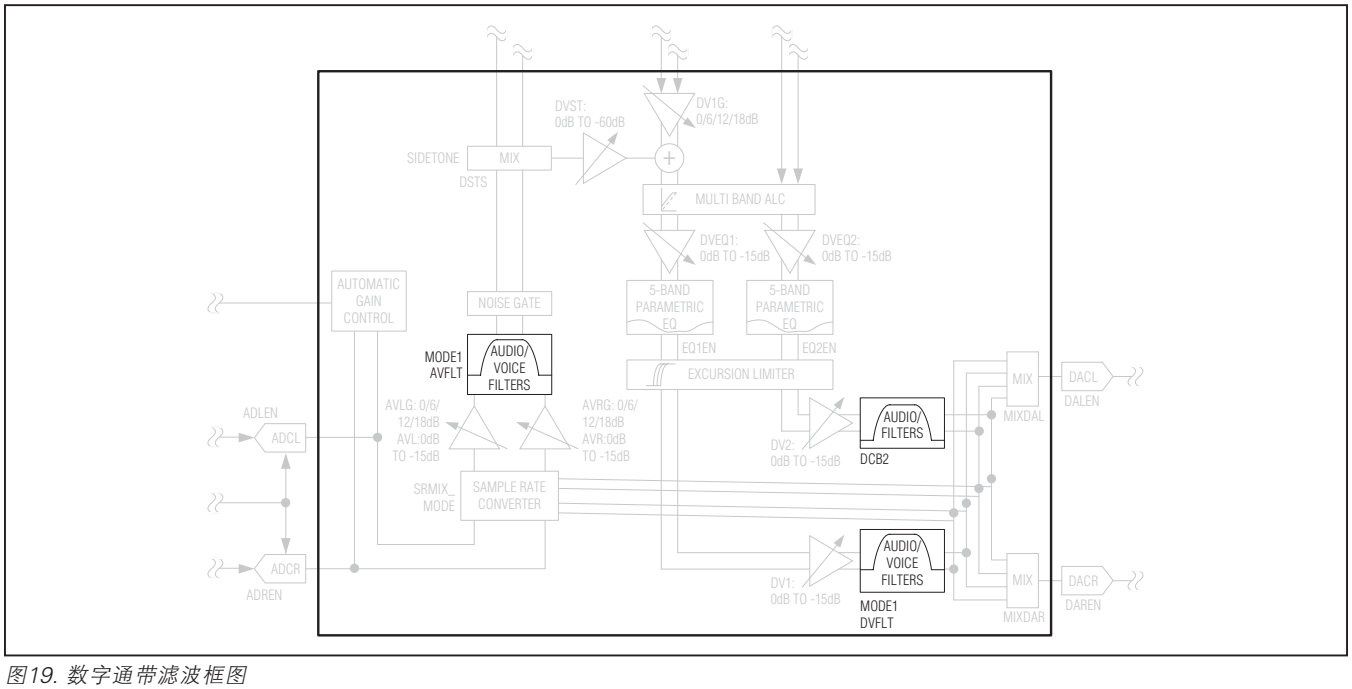
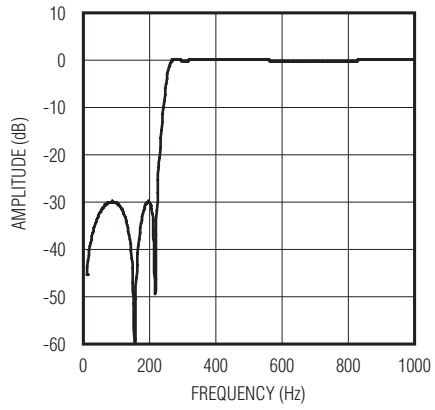
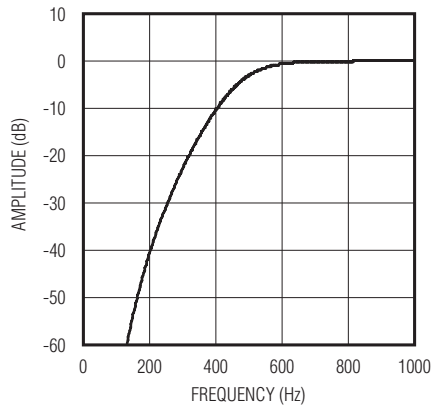
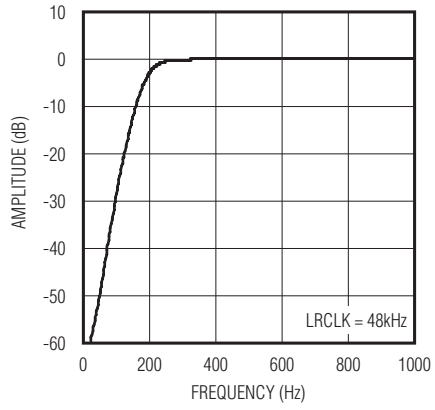


图19. 数字通带滤波框图

表14. 通带滤波寄存器

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="10">0x18</td><td>7</td><td>MODE1</td><td colspan="2">DAI1 Passband Filtering Mode
0 = Voice filters
1 = Music filters (recommended for fS > 24kHz)</td></tr>
<tr><td>6</td><td rowspan="3">AVFLT1</td><td colspan="2">DAI1 ADC Highpass Filter Mode</td></tr>
<tr><td>5</td><td>MODE1</td><td>AVFLT1</td></tr>
<tr><td rowspan="2">4</td><td>0</td><td>See Table 15.</td></tr>
<tr><td>1</td><td>Select a nonzero value to enable the DC- blocking filter.</td></tr>
<tr><td>3</td><td>DHF1</td><td colspan="2">DAI1 High Sample Rate Mode
Selects the sample rate range.
0 = 8kHz ≤ LRCLK ≤ 48kHz
1 = 48kHz ≤ LRCLK ≤ 96kHz</td></tr>
<tr><td>2</td><td rowspan="3">DVFLT1</td><td colspan="2">DAI1 DAC Highpass Filter Mode</td></tr>
<tr><td rowspan="2">1</td><td>MODE1</td><td>DVFLT1</td></tr>
<tr><td>0</td><td>See Table 15.</td></tr>
<tr><td>0</td><td>1</td><td>Select a nonzero value to enable the DC-blocking filter.</td></tr>
<tr><td rowspan="2">0x20</td><td>3</td><td>DHF2</td><td colspan="2">DAI2 High Sample Rate Mode
Selects the sample rate range.
0 = 8kHz ≤ LRCLK ≤ 48kHz
1 = 48kHz < LRCLK ≤ 96kHz</td></tr>
<tr><td>0</td><td>DCB2</td><td colspan="2">DAI2 DC Blocking Filter
Enables a DC-blocking filter on the DAI2 playback audio path.
0 = Disabled
1 = Enabled</td></tr>
</table>

表15. 语音高通滤波器

AVFTL/DVFLT VALUE	INTENDED SAMPLE RATE	FILTER RESPONSE
000	N/A	Disabled
001/011	16kHz/8kHz	
010/100	16kHz/8kHz	
101	8kHz to 48kHz	
110/111	N/A	Reserved

回放通路信号处理

IC回放信号通路包括自动电平控制(ALC)和5波段参数均衡器(EQ) (图20)。DAI1和DAI2回放通路包括由一组寄存器控制的独立ALC。提供两个完全独立的参数EQ，分别用于DAI1和DAI2回放通路。

自动电平控制

自动电平控制(ALC)电路确保最大信号幅度下不会产生信号削波。通过可调节增益级电路实现，根据每次采样可以将增益提高到最大12dB。预测电路确定下次采样是否会超出满量程范围，必要时降低增益，从而将采样值控制在满量程处。

可编程小信号门限用于确定所要放大信号的最小幅度，选择适当门限可以避免放大背景噪声。信号电平低于设置门限以下时，ALC将增益降至0dB，直到信号上升到门限以上。图21所示为ALC输入与输出的关系曲线。

ALC可选择配置为多波段模式。该模式下，输入信号滤波后划分到以5kHz为中心频率的两个波段。每个波段的信号分别送入独立的ALC，然后再叠加到一起。多波段模式下，两个波段采用相同参数。

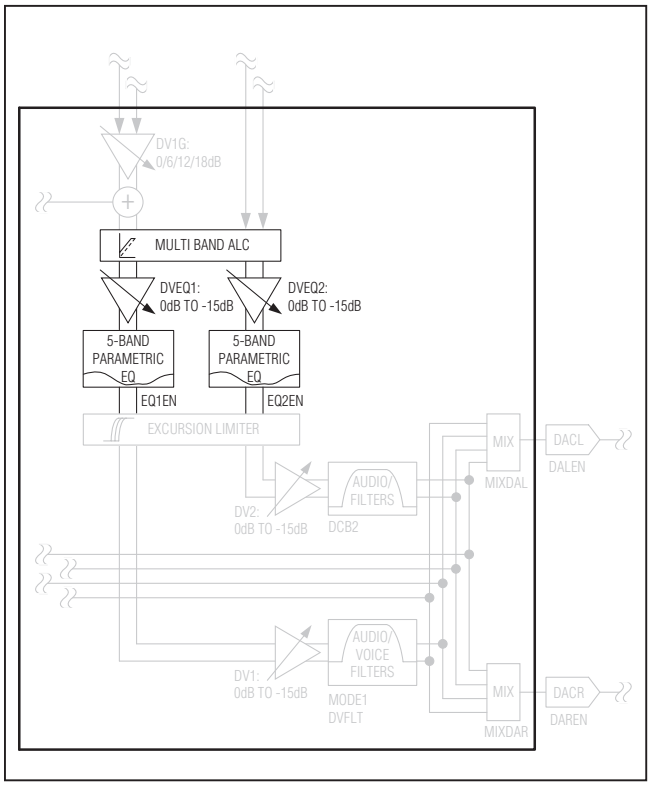


图20. 回放通路信号处理框图

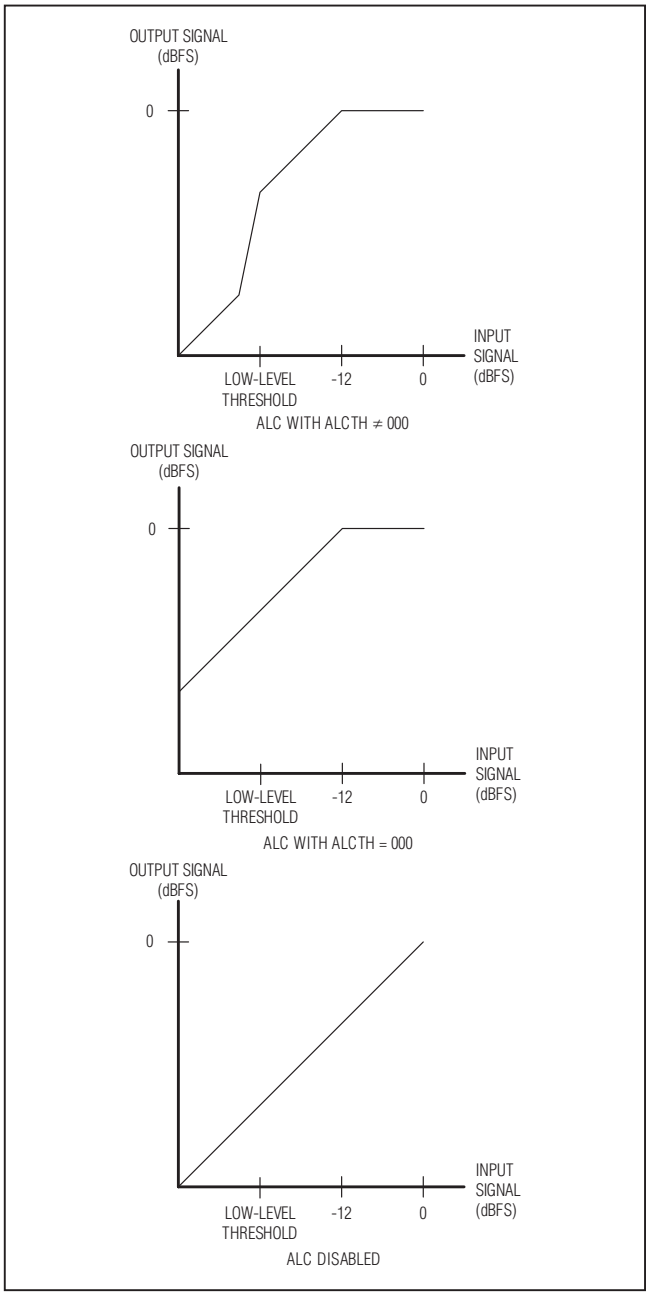


图21. ALC输入与输出关系示例

表16. 自动电平控制寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x43	7	ALCEN	**ALC Enable** Enables ALC on both the DAI1 and DAI2 playback paths. 0 = Disabled 1 = Enabled
	6	ALCRLS	**ALC and Excursion Limiter Release Time** Sets the release time for both the ALC and Excursion Limiter. See the *Excursion Limiter* section for Excursion Limiter release times. ALC release time is defined as the time required to adjust the gain from 12dB to 0dB.
			VALUE / **ALC RELEASE TIME (s)**
	5		000 / 8
			001 / 4
			010 / 2
			011 / 1
	4		100 / 0.5
			101 / 0.25
			110 / Reserved
			111 / Reserved
	3	ALCMB	**Multiband Enable** Enables multiband processing with a 5kHz center frequency. SR1 and SR2 must be configured properly to achieve the correct center frequency for each playback path. 0 = Single-band ALC 1 = Dual-band ALC
	2	ALCTH	**Low Signal Threshold** Selects the minimum signal level to be boosted by the ALC. 000 = -∞dB (low-signal threshold disabled) 001 = -12dB 010 = -18dB 011 = -24dB 100 = -30dB 101 = -36dB 110 = -42dB 111 = -48dB
	1		
	0		

参数均衡器

参数EQ包括5个独立的滤波器，每个滤波器包含两级二阶滤波，可编程增益、中心频率和带宽。两级二阶滤波器的增益范围为±12dB，中心频率：20Hz至20kHz。使用Q值小于图22所示的滤波器，可以获得理想的频率响应。较大的Q值容易造成不理想的频率响应。两级二阶滤波器串联在一起，可以获得±60dB的总增益。

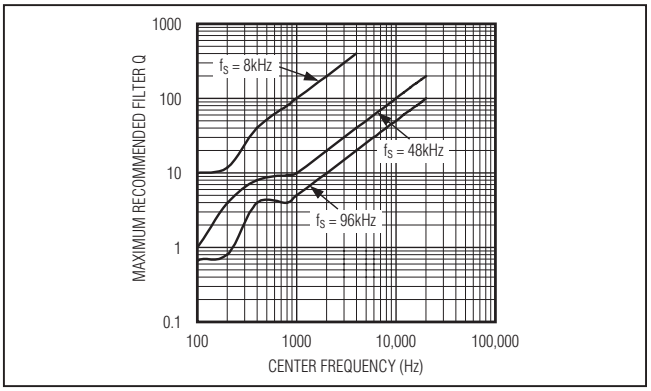


图22. 推荐的滤波器最大Q值与频率的关系曲线

在EQ输入使用衰减器，避免信号削波。衰减器可设置为固定衰减值或根据信号电平动态调整衰减。如果使能动态EQ削波检测，EQ信号电平将反馈至衰减器电路，以确定需要降低的增益量，以避免削波。

MAX98089评估软件包括用于产生EQ系数的图形界面，系数与采样率相关，储存在寄存器0x52至0xB5。

表17. EQ寄存器

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="11">0x30/0x32</td><td>4</td><td>$\overline{\text{EQCLP1}}$/
$\overline{\text{EQCLP2}}$</td><td>DAI1/DAI2 EQ Clip Detection
Automatically controls the EQ attenuator to prevent clipping in the EQ.
0 = Enabled
1 = Disabled</td></tr>
<tr><td>3</td><td rowspan="10">DVEQ1/DVEQ2</td><td>DAI1/DAI2 EQ Attenuator
Provides attenuation to prevent clipping in the EQ when full-scale signals are boosted. DVEQ1/DVEQ2 operates only when EQ1EN/EQ2EN = 1 and $\overline{\text{EQCLP1}}$/$\overline{\text{EQCLP2}}$ = 1.</td></tr>
<tr><td rowspan="3">2</td><td>VALUE | GAIN (dB) | VALUE | GAIN (dB)</td></tr>
<tr><td>0x0 | 0 | 0x8 | -8</td></tr>
<tr><td>0x1 | -1 | 0x9 | -9</td></tr>
<tr><td rowspan="3">1</td><td>0x2 | -2 | 0xA | -10</td></tr>
<tr><td>0x3 | -3 | 0xB | -11</td></tr>
<tr><td>0x4 | -4 | 0xC | -12</td></tr>
<tr><td rowspan="3">0</td><td>0x5 | -5 | 0xD | -13</td></tr>
<tr><td>0x6 | -6 | 0xE | -14</td></tr>
<tr><td>0x7 | -7 | 0xF | -15</td></tr>
<tr><td rowspan="5">0x49</td><td>7</td><td>$\overline{\text{VS2EN}}$</td><td rowspan="3">See the Click-and-Pop Reduction section.</td></tr>
<tr><td>6</td><td>$\overline{\text{VSEN}}$</td></tr>
<tr><td>5</td><td>$\overline{\text{ZDEN}}$</td></tr>
<tr><td>1</td><td>EQ2EN</td><td>DAI2 EQ Enable
0 = Disabled
1 = Enabled</td></tr>
<tr><td>0</td><td>EQ1EN</td><td>DAI1 EQ Enable
0 = Disabled
1 = Enabled</td></tr>
</table>

回放电平控制

IC包括分别用于DAI1和DAI2回放音频通路的数字电平控制。MODE1 = 0时，DAI1信号通路允许升压，任何模式下均允许衰减。DAI2信号通路只允许衰减。

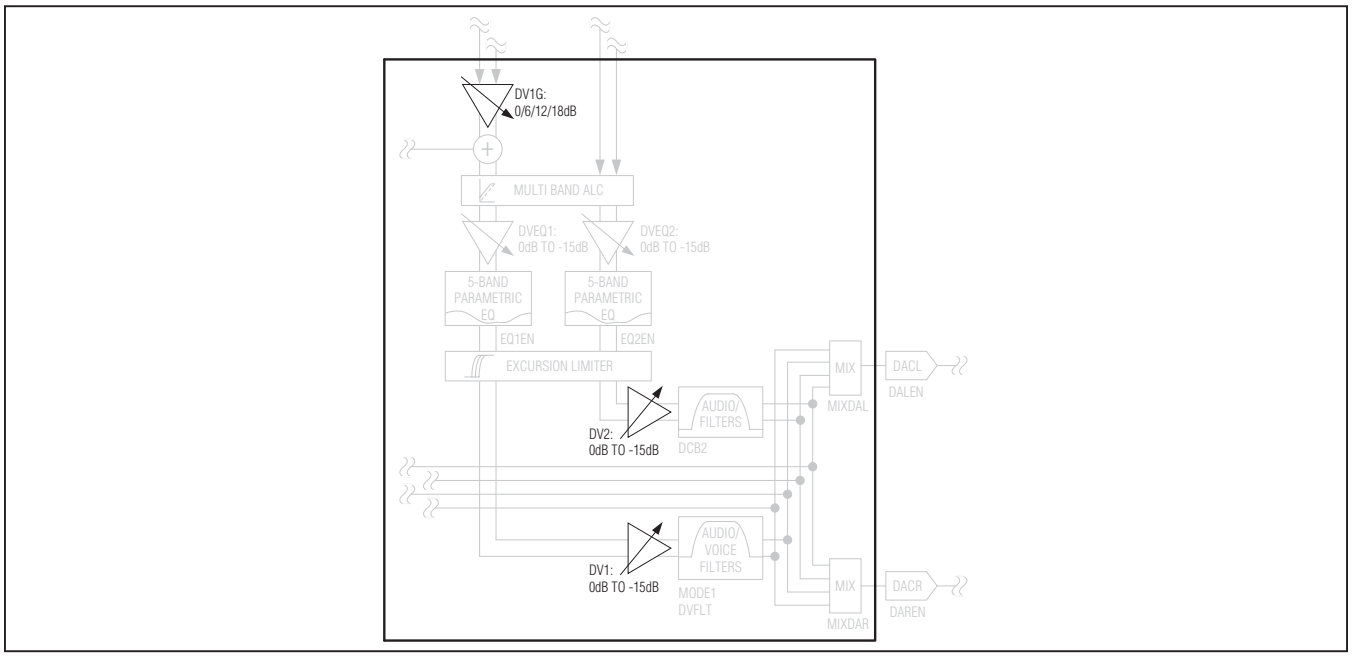


图23. 回放电平控制框图

表18. DAC回放电平控制寄存器

REGISTER	BIT	NAME	DESCRIPTION			
0x2F/0x31	7	DV1M/DV2M	**DAI1/DAI2 Mute** 0 = Disabled 1 = Enabled			
	5	DV1G	**DAI1 Voice Mode Gain** DV1G only applies when MODE1 = 0. 00 = 0dB 01 = 6dB 10 = 12dB 11 = 18dB			
	4					
	3	DV1/DV2	**DAI1/DAI2 Attenuation**			
			VALUE	**GAIN (dB)**	**VALUE**	**GAIN (dB)**
	2		0x0	0	0x8	-8
			0x1	-1	0x9	-9
			0x2	-2	0xA	-10
	1		0x3	-3	0xB	-11
			0x4	-4	0xC	-12
			0x5	-5	0xD	-13
	0		0x6	-6	0xE	-14
			0x7	-7	0xF	-15

DAC输入混音器

IC的立体声DAC接收来自两个数字音频通路的输入，DAC混音器将任意音频通路连接到左、右声道DAC (图24)。

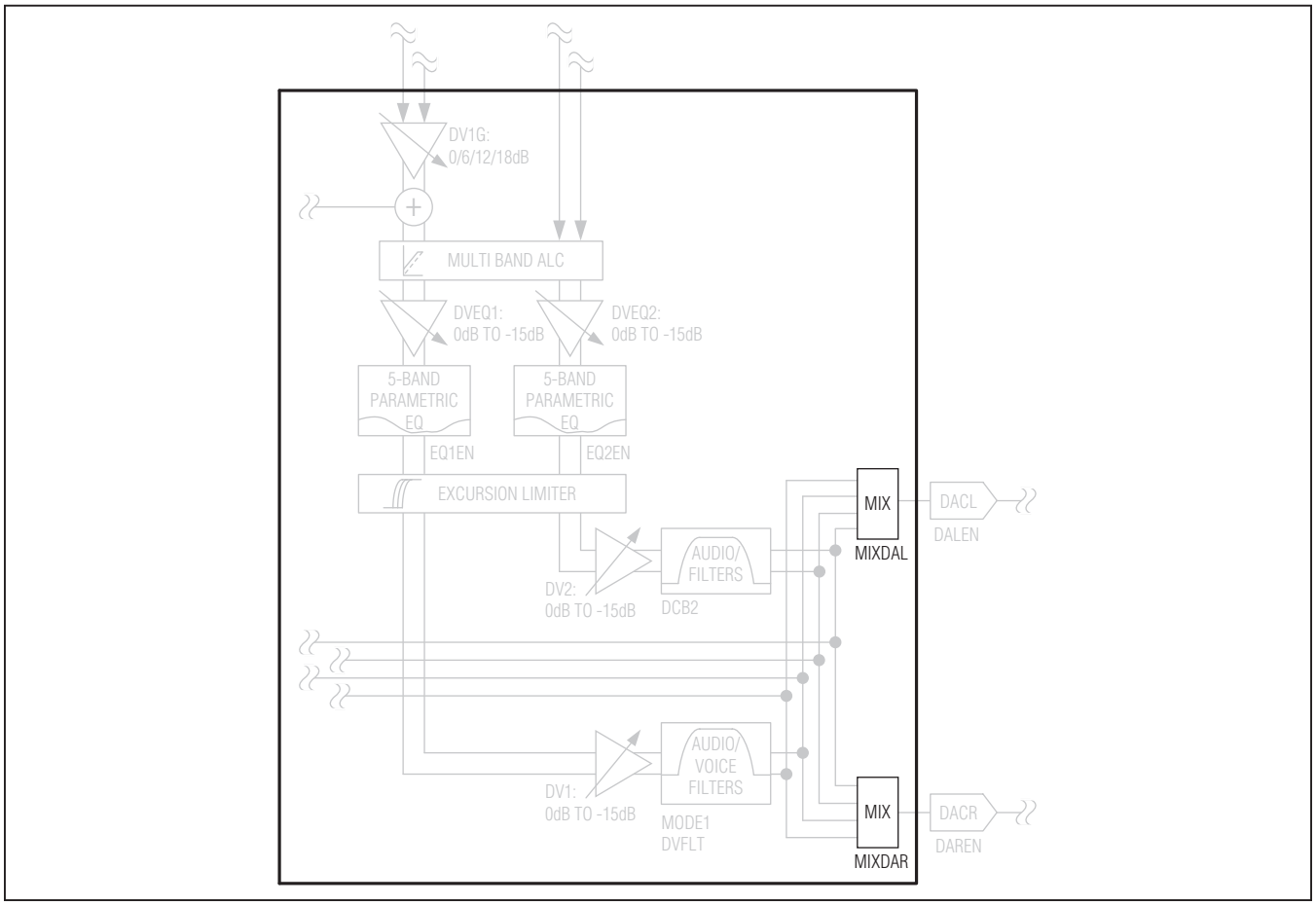


图24. DAC输入混音器框图

表19. DAC输入混音器寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x22	7	MIXDAL	**Left DAC Input Mixer** 1xxx = DAI1 left channel x1xx = DAI1 right channel xx1x = DAI2 left channel xxx1 = DAI2 right channel
	6		
	5		
	4		
	3	MIXDAR	**Right DAC Input Mixer** 1xxx = DAI1 left channel x1xx = DAI1 right channel xx1x = DAI2 left channel xxx1 = DAI2 right channel
	2		
	1		
	0		

接收放大器

IC具有一个差分接收放大器。接收放大器设计用于驱动32Ω听筒扬声器。如果一个传感器的信号同时送入扩音器和接收器，可以使用SPKBYP开关将接收放大器输出连接到左声道扬声器输出。利用I²C接口，接收放大器也可配置成立体声单端线出。

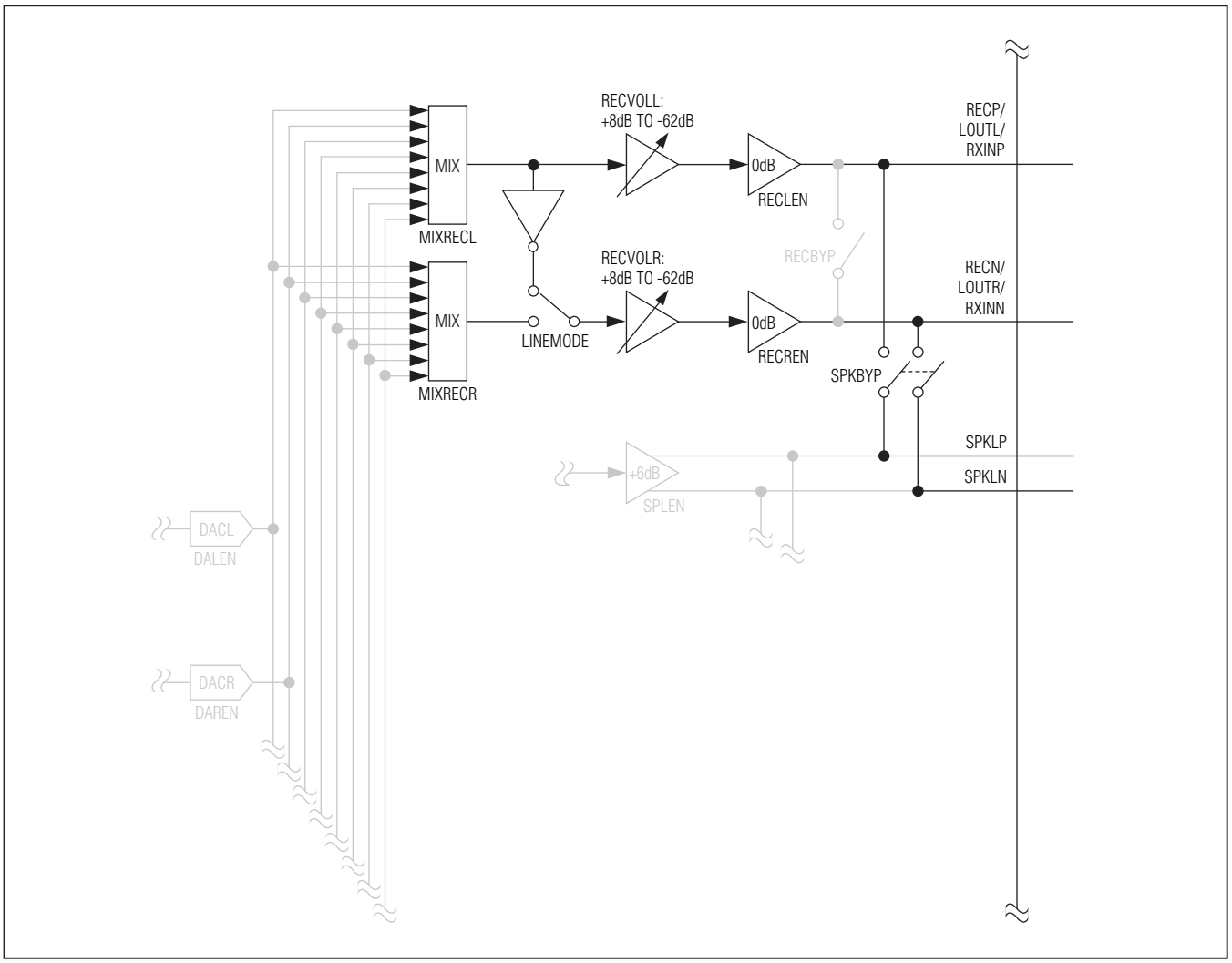


图25. 接收放大器框图

接收器输出混音器

IC的接收放大器接受来自于立体声DAC、线入(单端或差分)和MIC的输入。配置混音器对不同信号源组合进行混音。所选择的信号多于一个时，可配置为混音信号提供6dB、9dB或12dB衰减。

表20. 接收器输出混音器寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x28	7	MIXRECL	**Left Receiver Output Mixer** 1xxxxxxx = Right DAC x1xxxxxx = MIC2 xx1xxxxx = MIC1 xxx1xxxx = INB2 (INBDIFF = 0) or INB2-INB1 (INADIFF = 1) xxxx1xxx = INB1 xxxxx1xx = INA2 (INADIFF = 0) or INA2-INA1 (INADIFF = 1) xxxxxx1x = INA1 xxxxxxx1 = Left DAC
	6		
	5		
	4		
	3		
	2		
	1		
	0		
0x29	7	MIXRECR	**Right Receiver Output Mixer** 1xxxxxxx = Left DAC x1xxxxxx = MIC2 xx1xxxxx = MIC1 xxx1xxxx = INB2 (INBDIFF = 0) or INB2-INB1 (INBDIFF = 1) xxxx1xxx = INA1 xxxxx1xx = INA2 (INADIFF = 0) or INA2-INA1 (INADIFF = 1) xxxxxx1x = INA1 xxxxxxx1 = Right DAC
	6		
	5		
	4		
	3		
	2		
	1		
	0		
0x2A	7	LINE_MODE	**Receiver Output Mode**. Configures receive path output mode between BTL and stereo line output. 0 = BTL 1 = Stereo line output
	3	MIXRECR _GAIN	**Right Receiver Mixer Gain Select** 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	2		
	1	MIXRECL _GAIN	**Left Receiver Mixer Gain Select** 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	0		
	0		

接收器输出音量

表21. 接收器输出电平寄存器

REGISTER	BIT	NAME	DESCRIPTION			
0x3B/0x3C	7	RECLM/ RECRM	**Receiver Output Mute** 0 = Disabled 1 = Enabled			
	4	RECVOLL/ RECVOLR	**Receiver Output Volume Level**			
			VALUE	**VOLUME (dB)**	**VALUE**	**VOLUME (dB)**
	3		0x00	-62	0x10	-10
			0x01	-58	0x11	-8
			0x02	-54	0x12	-6
			0x03	-50	0x13	-4
	2		0x04	-46	0x14	-2
			0x05	-42	0x15	0
			0x06	-38	0x16	+1
			0x07	-35	0x17	+2
	1		0x08	-32	0x18	+3
			0x09	-29	0x19	+4
			0x0A	-26	0x1A	+5
			0x0B	-23	0x1B	+6
	0		0x0C	-20	0x1C	+6.5
			0x0D	-17	0x1D	+7
			0x0E	-14	0x1E	+7.5
			0x0F	-12	0x1F	+8

扬声器放大器

IC集成了立体声无滤波D类放大器，效率远远高于AB类放大器，而且消除了D类放大器常见的缺点。

D类放大器的高效率得益于输出级晶体管的开关工作模式。D类放大器中，输出晶体管作为电流驱动开关，所消耗的功率可忽略不计。与D类放大器输出级相关的功率损耗主要源于MOSFET导通电阻的I^2R损耗和静态电流开销。

线性放大器在理论上的最大效率是78%，但只有在峰值输入功率下才能达到这一效率。常规工作模式(典型的音乐信号幅度)下，效率大多在30%以下；而利用IC内部的D类放大器，同等条件下效率仍可保持在80%以上。

传统的D类放大器要求使用外部LC滤波或屏蔽，以满足EN55022B和FCC电磁干扰(EMI)规范要求。Maxim的有源辐射抑制专利技术通过控制边沿速率，降低电路的EMI辐射，在典型应用中可以不使用输出滤波器。

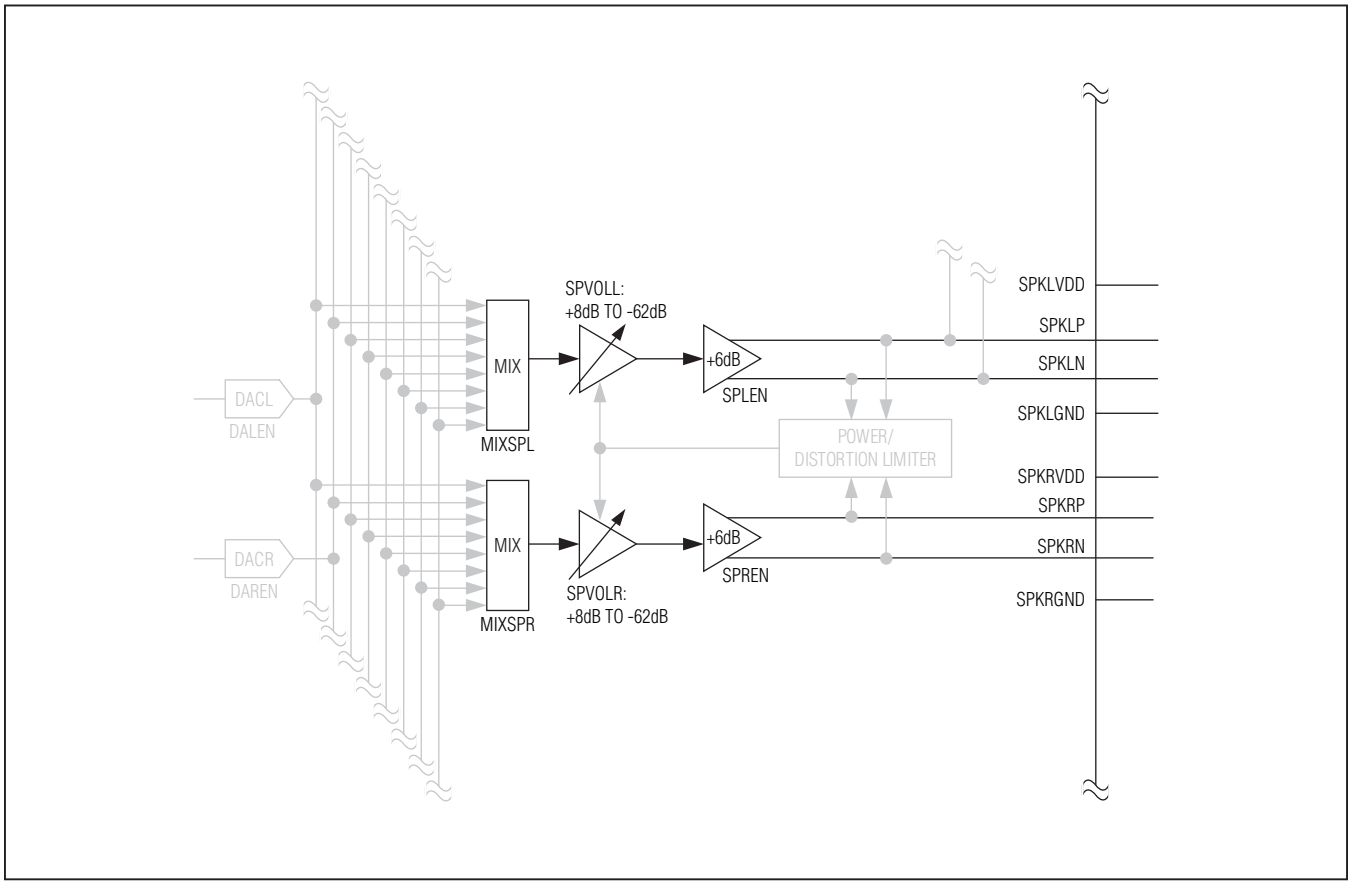


图26. 扬声器放大器通路框图

扬声器输出混音器

IC的扬声器放大器接收立体声DAC、线入(单端或差分)和MIC的输入。配置混音器对不同信号源的任意组合进行混音。选择信号多于一个时，可配置混音器对信号提供6dB、9dB或12dB衰减。

表22. 扬声器输出混音器寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x2B	7	MIXSPL	**Left Speaker Output Mixer** 1xxxxxxx = Right DAC x1xxxxxx = MIC2 xx1xxxxx = MIC1 xxx1xxxx = INB2 (INBDIFF = 0) or INB2-INB1 (INBDIFF = 1) xxxx1xxx = INB1 xxxxx1xx = INA2 (INBDIFF = 0) or INA2-INA1 (INADIFF = 1) xxxxxx1x = INA1 xxxxxxx1 = Left DAC
	6		
	5		
	4		
	3		
	2		
	1		
	0		
0x2C	7	MIXSPR	**Right Speaker Output Mixer** 1xxxxxxx = Left DAC x1xxxxxx = MIC2 xx1xxxxx = MIC1 xxx1xxxx = INB2 (INBDIFF = 0) or INB2-INB1 (INBDIFF = 1) xxxx1xxx = INB1 xxxxx1xx = INA2 (INADIFF = 0) or INA2-INA1 (INADIFF = 1) xxxxxx1x = INA1 xxxxxxx1 = Right DAC
	6		
	5		
	4		
	3		
	2		
	1		
	0		
0x2D	3	MIXSPR_GAIN	**Right Speaker Mixer Gain Select** 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	2		
	1	MIXSPL_GAIN	**Left Speaker Mixer Gain Select** 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	0		

表23. 扬声器输出电平寄存器

REGISTER	BIT	NAME	DESCRIPTION			
0x3D/0x3E	7	SPLM/SPRM	**Left/Right Speaker Output Mute** 0 = Disabled 1 = Enabled			
	4 3 2 1	SPVOLL/SPVOLR	**Left/Right Speaker Output Volume Level**			
			VALUE	**VOLUME (dB)**	**VALUE**	**VOLUME (dB)**
			0x00	-62	0x10	-10
			0x01	-58	0x11	-8
			0x02	-54	0x12	-6
			0x03	-50	0x13	-4
			0x04	-46	0x14	-2
			0x05	-42	0x15	0
			0x06	-38	0x16	+1
			0x07	-35	0x17	+2
			0x08	-32	0x18	+3
			0x09	-29	0x19	+4
			0x0A	-26	0x1A	+5
			0x0B	-23	0x1B	+6
			0x0C	-20	0x1C	+6.5
			0x0D	-17	0x1D	+7
			0x0E	-14	0x1E	+7.5
			0x0F	-12	0x1F	+8

扬声器放大器信号处理

IC包括信号处理功能，以改善扬声器输出音质，并防止损坏传感器。失调抑制电路动态调整高通滤波器的截止频率，而功率抑制和失真抑制可以防止放大器输出产生过大的失真或功率。失调抑制电路位于DSP，失真抑制和功率抑制电路控制模拟音量开关(图28)。三个抑制器对扬声器放大器的输出信号进行分析，确定相应的操作。

抑制失调

抑制失调电路是一个动态高通滤波器，对扬声器输出进行监测，当扬声器放大器输出超出预设门限时，提高高通滤波器的截止频率。滤波器在高截止频率和低截止频率之间平滑切换，抑制杂波输出。滤波器可以工作在四种不同模式：

- **固定频率预设模式**。高通截止频率固定在较高拐点频率，不随信号电平变化。
- **固定频率可编程模式**。高通截止频率由可编程的两级二阶滤波器确定。
- **预设动态模式**。高通滤波器根据输出信号电平的大小在预设的高截止频率和低截止频率之间平滑切换。
- **用户可编程动态模式**。高通滤波器在低边用户编程双二阶滤波器和高边预置截止频率之间平滑切换。

用户可编程双二阶滤波器的传递函数为：

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

系数b_0、b_1、b_2、a_1和a_2与采样率有关，储存在寄存器0xB4至0xC7。b_0、b_1和b_2储存为正数，a_1和a_2储存为二进制补码负数。可独立储存DAI1和DAI2播放通路的滤波器参数。

MAX98089评估软件包括用于产生用户可编程双二阶滤波器系数的图形界面。

注：仅在信号通路被禁用时改变失调抑制设置，以消除杂波输出。

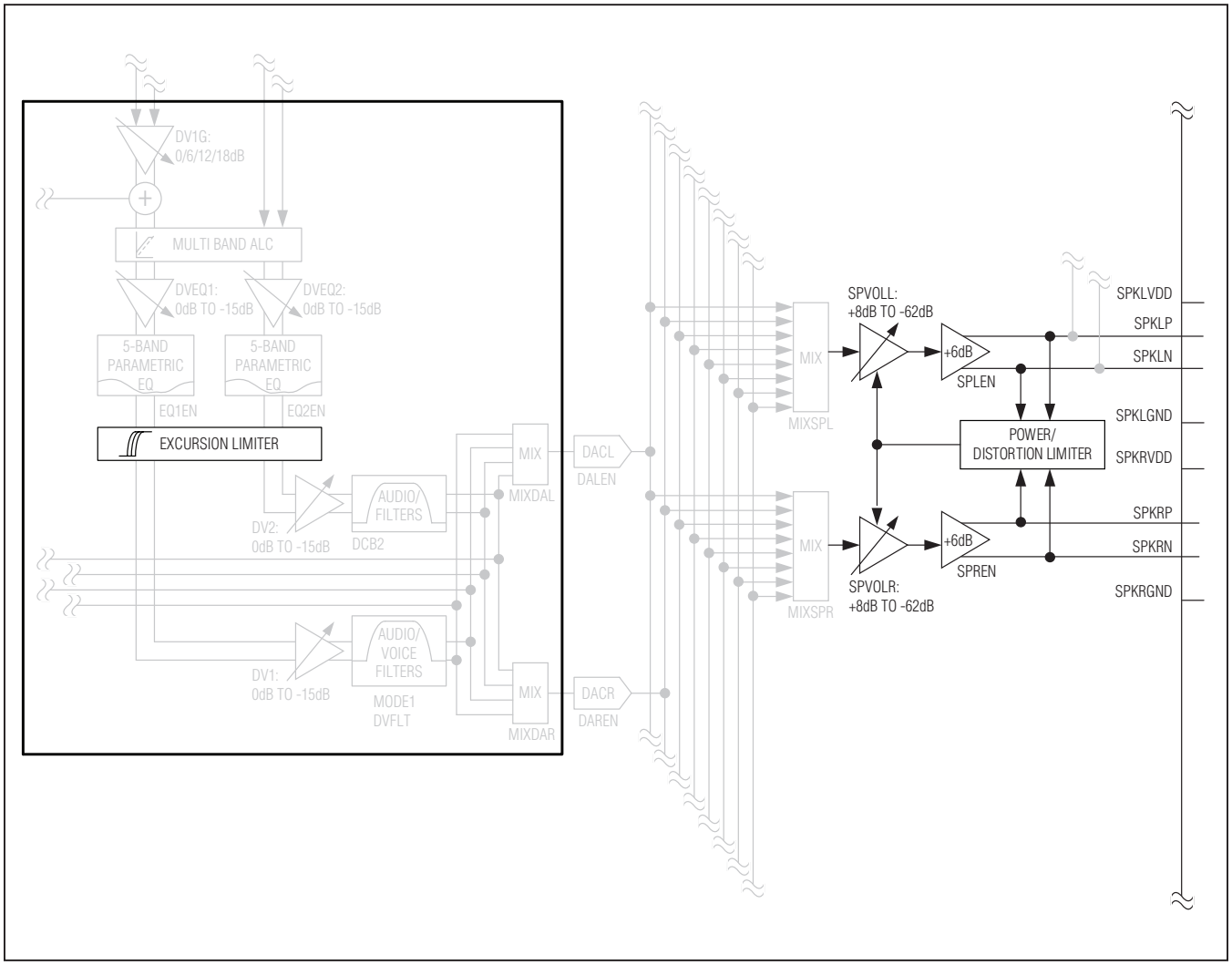


图27. 扬声器放大器信号处理框图

表24. 失调抑制寄存器

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="6">DESCRIPTION</th></tr>
<tr><td rowspan="15">0x41</td><td>6</td><td rowspan="6">DHPUCF</td><td colspan="6">Excursion Limiter Corner Frequency
The excursion limiter has limited sliding range and minimum corner frequencies. Listed below are all the valid filter combinations.</td></tr>
<tr><td>5</td><td colspan="2">LOWER CORNER FREQUENCY</td><td>UPPER CORNER FREQUENCY</td><td>MINIMUM BIQUAD CORNER FREQUENCY</td><td>DHPUCF</td><td>DHPLCF</td></tr>
<tr><td rowspan="4">4</td><td colspan="2">Excursion limiter disabled</td><td>—</td><td>000</td><td>00</td></tr>
<tr><td colspan="2">400Hz</td><td>—</td><td>001</td><td>00</td></tr>
<tr><td colspan="2">600Hz</td><td>—</td><td>010</td><td>00</td></tr>
<tr><td colspan="2">800Hz</td><td>—</td><td>011</td><td>00</td></tr>
<tr><td colspan="2">1kHz</td><td>—</td><td>100</td><td>00</td></tr>
<tr><td rowspan="4">1</td><td rowspan="9">DHPLCF</td><td colspan="2">Programmable using biquad</td><td>100Hz</td><td>000</td><td>11</td></tr>
<tr><td>200Hz</td><td>400Hz</td><td>—</td><td>001</td><td>01</td></tr>
<tr><td>400Hz</td><td>600Hz</td><td>—</td><td>010</td><td>10</td></tr>
<tr><td>400Hz</td><td>800Hz</td><td>—</td><td>011</td><td>10</td></tr>
<tr><td rowspan="4">0</td><td>Programmable using biquad</td><td>400Hz</td><td>200Hz</td><td>001</td><td>11</td></tr>
<tr><td>Programmable using biquad</td><td>600Hz</td><td>300Hz</td><td>010</td><td>11</td></tr>
<tr><td>Programmable using biquad</td><td>800Hz</td><td>400Hz</td><td>011</td><td>11</td></tr>
<tr><td>Programmable using biquad</td><td>1kHz</td><td>500Hz</td><td>100</td><td>11</td></tr>
<tr><td rowspan="10">0x43</td><td>6</td><td rowspan="10">ALCRLS</td><td colspan="6">ALC and Excursion Limiter Release Time
Sets the release time for both the ALC and Excursion Limiter. See the Automatic Level Control section for ALC release times. Excursion limiter release time is defined as the time required to slide from the high corner frequency to the low corner frequency.</td></tr>
<tr><td rowspan="4">5</td><td colspan="3">VALUE</td><td colspan="2">EXCURSION LIMITER RELEASE TIME (s)</td></tr>
<tr><td colspan="3">000</td><td colspan="2">4</td></tr>
<tr><td colspan="3">001</td><td colspan="2">2</td></tr>
<tr><td colspan="3">010</td><td colspan="2">1</td></tr>
<tr><td rowspan="4">4</td><td colspan="3">011</td><td colspan="2">0.5</td></tr>
<tr><td colspan="3">100</td><td colspan="2">0.25</td></tr>
<tr><td colspan="3">101</td><td colspan="2">0.25</td></tr>
<tr><td colspan="3">110</td><td colspan="2">Reserved</td></tr>
<tr><td colspan="3">111</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">0x42</td><td>3</td><td rowspan="4">DHPTH</td><td colspan="6">Excursion Limiter Threshold
Measured at the Class D speaker amplifier outputs. Signals above the threshold use the upper corner frequency. Signals below the threshold use the lower corner frequency.
V_{BAT} must correctly reflect the voltage of SPKLVDD to achieve accurate thresholds.
000 = 0.34V_P
001 = 0.71V_P
010 = 1.30V_P
011 = 1.77V_P
100 = 2.33V_P
101 = 3.25V_P
110 = 4.25V_P
111 = 4.95V_P</td></tr>
<tr><td>2</td></tr>
<tr><td>1</td></tr>
<tr><td>0</td></tr>
</table>

功率抑制器

IC的功率抑制器连续跟踪扩音器驱动功率，如果扬声器存在被损坏的风险，则禁止扬声器放大器输出。

如果音圈由于长时间工作在额定功率以上而导致发热，则可能导致扩音器损坏。正常工作期间，音圈产生的热量会传递到扬声器的磁铁，磁铁又将热量扩散到周围空气中。音圈过热时，音圈和磁铁均会过热。但在扬声器发热导致损坏之前，扬声器还能在相当长的时间内工作在高于额定功率的状况下。

IC的功率抑制器可由用户设置时间常数和功率门限，以满足不同扩音器的特性。将功率抑制器的门限设置在相应扩音器的额定功率，可通过测量或查询扩音器的技术指标确定。编程时间常数1使其满足音圈的热时间常数要求；编程时间常数2使其符合磁铁的热时间常数要求。可通过绘制音圈阻抗与功率作用时间的关系曲线来确定时间常数。

表25. 功率抑制器寄存器

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="20">0x44</td><td>7</td><td rowspan="10">PWRTH</td><td colspan="4">Power Limiter Threshold
If the continuous output power from the speaker amplifiers exceeds this threshold, the output is briefly muted to protect the speaker. The threshold is measured in watts assuming an 8Ω load. VBAT must correctly reflect the voltage of SPKLVDD/SPKRVDD to achieve accurate thresholds.</td></tr>
<tr><td rowspan="2">6</td><td>VALUE</td><td>THRESHOLD (W)</td><td>VALUE</td><td>THRESHOLD (W)</td></tr>
<tr><td>0x0</td><td>Power limiter disabled</td><td>0x8</td><td>0.27</td></tr>
<tr><td rowspan="3">5</td><td>0x1</td><td>0.05</td><td>0x9</td><td>0.35</td></tr>
<tr><td>0x2</td><td>0.06</td><td>0xA</td><td>0.48</td></tr>
<tr><td>0x3</td><td>0.09</td><td>0xB</td><td>0.72</td></tr>
<tr><td rowspan="3">4</td><td>0x4</td><td>0.11</td><td>0xC</td><td>1.00</td></tr>
<tr><td>0x5</td><td>0.13</td><td>0xD</td><td>1.43</td></tr>
<tr><td>0x6</td><td>0.18</td><td>0xE</td><td>1.57</td></tr>
<tr><td>0x7</td><td>0.22</td><td>0xF</td><td>1.80</td></tr>
<tr><td>2</td><td rowspan="8">PWRK</td><td colspan="3">Power Limiter Weighting Factor
Determines the balance between time constant 1 and 2 to match the dominance of each time constant in the loudspeaker.</td></tr>
<tr><td rowspan="4">1</td><td>VALUE</td><td>T1 (%)</td><td>T2 (%)</td></tr>
<tr><td>000</td><td>50</td><td>50</td></tr>
<tr><td>001</td><td>62.5</td><td>37.5</td></tr>
<tr><td>010</td><td>75</td><td>25</td></tr>
<tr><td rowspan="4">0</td><td>011</td><td>87.5</td><td>12.5</td></tr>
<tr><td>100</td><td>100</td><td>0</td></tr>
<tr><td>101</td><td>12.5</td><td>87.5</td></tr>
<tr><td>110</td><td>25</td><td>75</td></tr>
<tr><td>111</td><td>37.5</td><td>62.5</td></tr>
</table>

表25. 功率抑制器寄存器(续)

REGISTER	BIT	NAME	DESCRIPTION			
0x45	7	PWRT2	**Power Limiter Time Constant 2** Select a value that matches the thermal time constant of the loudspeaker's magnet.			
	6		**VALUE**	**TIME CONSTANT (min)**	**VALUE**	**TIME CONSTANT (min)**
			0x0	Disabled	0x8	3.75
			0x1	0.50	0x9	5.00
	5		0x2	0.67	0xA	6.66
			0x3	0.89	0xB	8.88
			0x4	1.19	0xC	Reserved
	4		0x5	1.58	0xD	Reserved
			0x6	2.11	0xE	Reserved
			0x7	2.81	0xF	Reserved
	3	PWRT1	**Power Limiter Time Constant 1** Select a value that matches the thermal time constant of the loudspeaker's voice coil.			
	2		**VALUE**	**TIME CONSTANT (s)**	**VALUE**	**TIME CONSTANT (s)**
			0x0	Disabled	0x8	3.75
			0x1	0.50	0x9	5.00
	1		0x2	0.67	0xA	6.66
			0x3	0.89	0xB	8.88
			0x4	1.19	0xC	Reserved
	0		0x5	1.58	0xD	Reserved
			0x6	2.11	0xE	Reserved
			0x7	2.81	0xF	Reserved

失真抑制

IC的失真抑制可确保扬声器放大器的输出不超出所设置的THD+N限制。失真抑制对D类放大器的输出占空比进行分析，以确定削波波形的百分比。如果失真超出所设置的门限，则降低输出增益。

表26. 失真抑制寄存器

REGISTER	BIT	NAME	DESCRIPTION			
0x46	7	THDCLP	**Distortion Limit** Measured in % THD+N.			
	6		**VALUE**	**THD+N LIMIT (%)**	**VALUE**	**THD+N LIMIT (%)**
	5		0x0	Limiter disabled	0x8	12
			0x1	< 1	0x9	14
			0x2	1	0xA	16
			0x3	2	0xB	18
	4		0x4	4	0xC	20
			0x5	6	0xD	21
			0x6	8	0xE	22
			0x7	10	0xF	24
	0	THDT1	**Distortion Limiter Release Time Constant** Duration of time required for the speaker amplifier's output gain to adjust back to the nominal level after a large signal has passed. 0 = 1.4s 1 = 2.8s			

耳机

DirectDrive耳机放大器

传统的单电源供电耳机放大器的输出偏压为标称直流电压(通常为电源电压的一半)，需要较大的耦合电容隔离耳机的直流偏压。如果没有这些电容，则会向耳机诸入较大的直流电流，产生不必要的功耗，并可能损坏耳机和耳机放大器。

Maxim的第二代DirectDrive架构采用电荷泵产生内部负电源，从而在单电源供电的条件下，使IC的耳机输出偏置在GND (图1)，由于没有直流分量，所以省去了大尺寸隔直流电容。与使用两个大电容(220µF，典型值)不同，IC的电荷泵仅需要3个小尺寸陶瓷电容，节省电路板空间、节约成本，并改善耳机放大器的频率响应。

电荷泵

双模电荷泵产生正、负电源，用于耳机放大器供电。为提高效率，电荷泵的开关频率和输出电压均根据信号电平变化。

输入信号电平小于PVDD的10%时，开关频率降至低速，使电荷泵的开关损耗降至最小；输入信号超出PVDD的10%时，开关频率增大，以支持负载电流。

输入信号低于PVDD的25%时，电荷泵产生±(PVDD/2)电压，将放大器功率级的压降降至最小，从而提高效率；输入信号超出PVDD的25%时，电荷泵输出±PVDD。较高的输出电压允许耳机放大器输出满幅功率。

为防止从±(PVDD/2)输出模式转换到±PVDD输出模式时出现音频尖峰脉冲，电荷泵切换速度非常快，高速切换期间会从PVDD吸收相当大的电流。PVDD的旁路电容提供所要求的电流并防止PVDD跌落。

可通过I^2C接口关闭电荷泵的动态切换模式。强制电荷泵输出±(PVDD/2)或±PVDD，与输入信号电平无关。

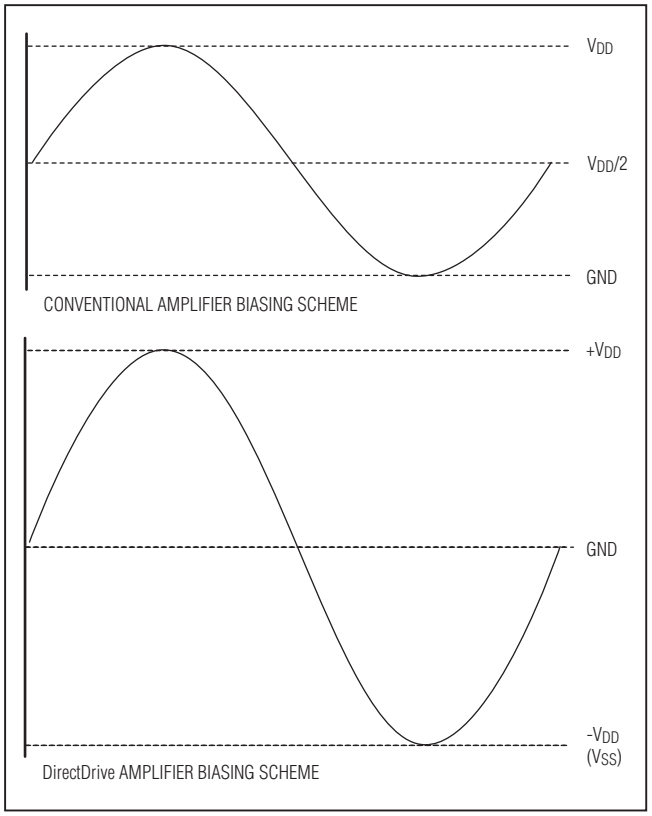


图28. 传统放大器输出与DirectDrive输出的比较

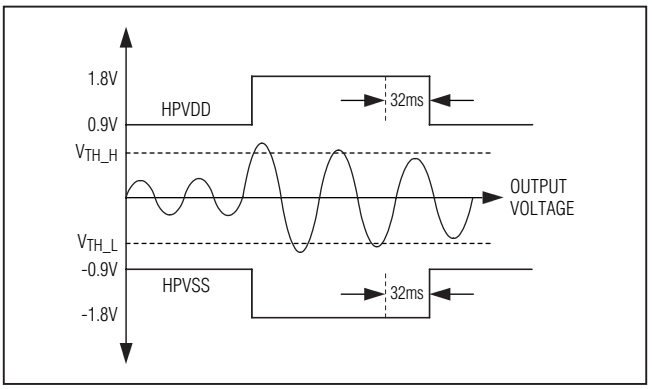


图29. H类放大器

H类放大器

H类放大器采用AB类输出级，电源电压受输出信号调制。针对这款IC，电荷泵可提供两路标称电源差：1.8V (+0.9V至–0.9V)和3.6V (+1.8V至–1.8V)，图29所示为输出电压变化时的电源电压。

耳机地检测(HPSNS)

HPSNS检测耳机负载的地回路。为获得最佳性能，利用隔离走线将HPSNS连接到插孔地端，如图30所示。如果不使用HPSNS，则将其连接到模拟地。

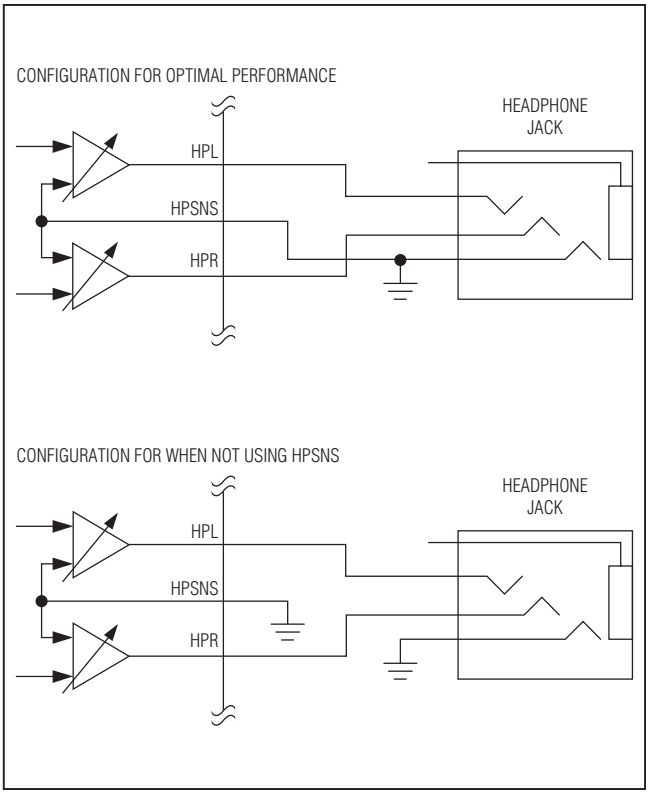


图30. HPSNS配置

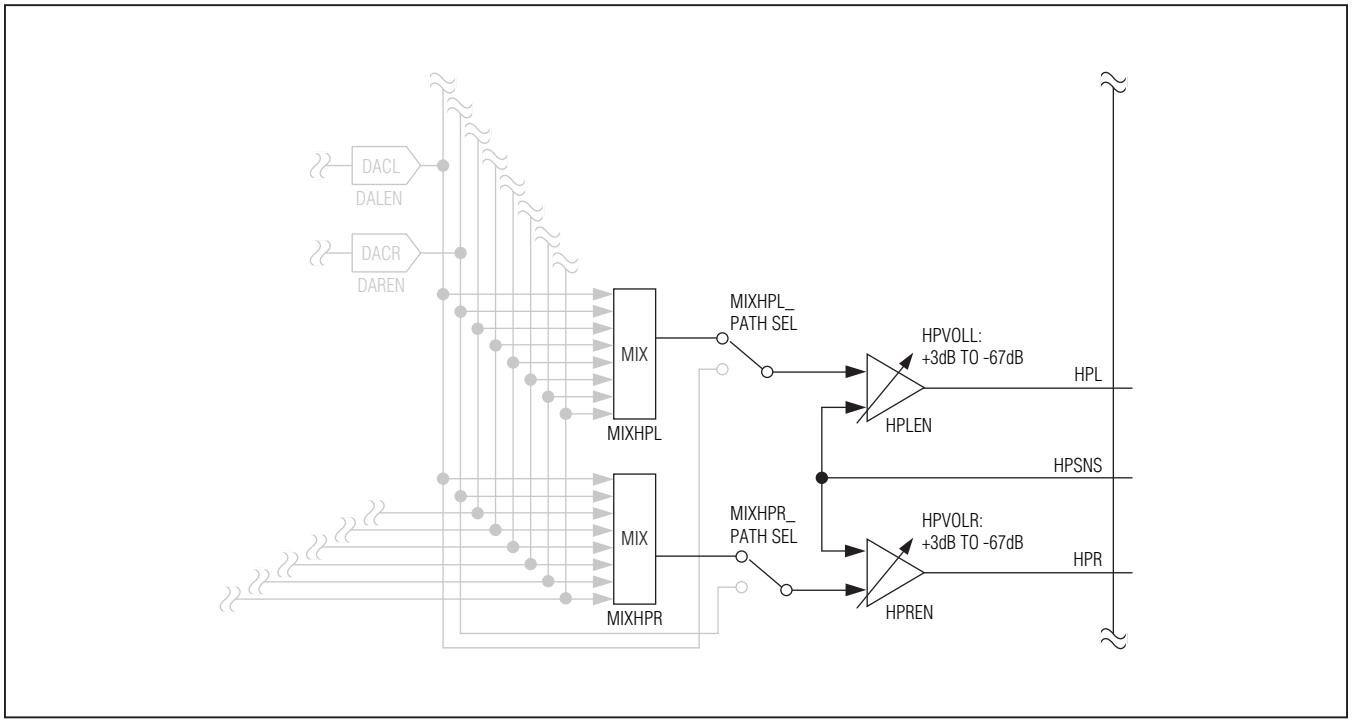

DACL
DALEN
DACR
DAREN
MIX
MIXHPL
MIXHPL_
PATH SEL
HPVOLL:
+3dB TO -67dB
HPL
HPLEN
HPSNS
MIX
MIXHPR
MIXHPR_
PATH SEL
HPVOLR:
+3dB TO -67dB
HPR
HPREN

图31. 耳机放大器框图

耳机输出混音器

耳机放大器混音器接受来自立体声DAC、线入(单端或差分)和MIC的输入。可以配置混音器对音频源的任意组合进行混音。选择信号多于一个时，可配置混音器对信号提供6dB、9dB或12dB衰减。立体声DAC可旁路耳机混音器，直接连接到耳机放大器，以降低功耗。

表27. 耳机输出混音器寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x25	7	MIXHPL	**Left Headphone Output Mixer** 1xxxxxxx = Right DAC x1xxxxxx = MIC2 xx1xxxxx = MIC1 xxx1xxxx = INB2 (INBDIFF = 0) or INB2-INB1 (INADIFF = 1) xxxx1xxx = INB1 xxxxx1xx = INA2 (INADIFF = 0) or INA2-INA1 (INADIFF = 1) xxxxxx1x = INA1 xxxxxxx1 = Left DAC
	6		
	5		
	4		
	3		
	2		
	1		
	0		
0x26	7	MIXHPR	**Right Headphone Output Mixer** 1xxxxxxx = Left DAC x1xxxxxx = MIC2 xx1xxxxx = MIC1 xxx1xxxx = INB2 (INBDIFF = 0) or INB2-INB1 (INBDIFF = 1) xxxx1xxx = INB1 xxxxx1xx = INA2 (INADIFF = 0) or INA2-INA1 (INADIFF = 1) xxxxxx1x = INA1 xxxxxxx1 = Right DAC
	6		
	5		
	4		
	3		
	2		
	1		
	0		
0x27	5	MIXHPR_ PATH SEL	**Right Headphone Mixer Path Select** 0 = Directly connect to the right DAC (bypass right headphone output mixer) 1 = Right headphone output mixer
	4	MIXHPL_ PATH SEL	**Left Headphone Mixer Path Select** 0 = Directly connect to the left DAC (bypass left headphone output mixer) 1 = Left headphone output mixer
	3	MIXHPR _GAIN	**Right Headphone Mixer Gain Select** 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	2		
	1	MIXHPL _GAIN	**Left Headphone Mixer Gain Select** 00 = 0dB 01 = -6dB 10 = -9dB 11 = -12dB
	0		

表28. 耳机输出电平寄存器

REGISTER	BIT	NAME	DESCRIPTION			
0x39/0x3A	7	HPLM/HPRM	**Headphone Output Mute** 0 = Disabled 1 = Enabled			
	4 3 2 1 0	HPVOLL/HPVOLR	**Left/Right Headphone Output Volume Level**			
			VALUE	**VOLUME (dB)**	**VALUE**	**VOLUME (dB)**
			0x00	-67	0x10	-15
			0x01	-63	0x11	-13
			0x02	-59	0x12	-11
			0x03	-55	0x13	-9
			0x04	-51	0x14	-7
			0x05	-47	0x15	-5
			0x06	-43	0x16	-4
			0x07	-40	0x17	-3
			0x08	-37	0x18	-2
			0x09	-34	0x19	-1
			0x0A	-31	0x1A	0
			0x0B	-28	0x1B	+1
			0x0C	-25	0x1C	+1.5
			0x0D	-22	0x1D	+2
			0x0E	-19	0x1E	+2.5
			0x0F	-17	0x1F	+3

输出旁路开关

IC包括两个输出旁路开关，用来解决常见的应用问题。单个传感器用于扩音器和接收器时，两个放大器将放大同一传感器的信号。旁路开关将IC的接收放大器输出连接到扬声器放大器的输出，允许任一放大器放大同一传感器信号。如果使用外部接收放大器，则通过RECP/RXINP和RECN/RXINN将其输出连接到左声道扬声器，旁路D类放大器。在外部放大器驱动接收器和IC线入的应用中，如果不需要某路差分信号，可将RECP/RXINP连接至RECN/RXINN模拟开关，断开与接收器的连接。

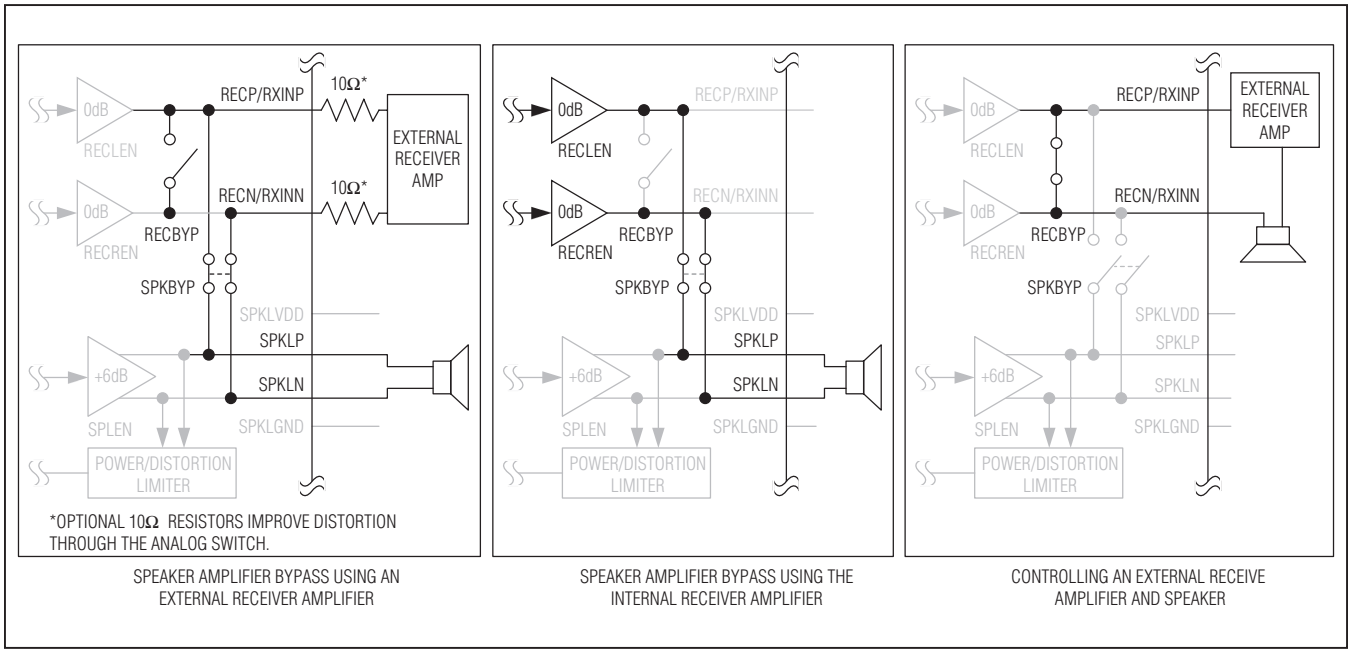


图32. 输出旁路开关框图

表29. 输出旁路开关寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x4A	7	INABYP	See the *Microphone Inputs* section.
	4	MIC2BYP	
	1	RECBYP	**RXINP to RXINN Bypass Switch** Shorts RXINP to RXINN allowing a signal to pass through the ICs. Disable the receiver amplifier when RECBYP = 1. 0 = Disabled 1 = Enabled
	0	SPKBYP	**RXIN to SPKL Bypass Switch** Shorts RXINP/RXINN to SPKLP/SPKLN allowing either the internal or an external receiver amplifier to power the left speaker. Disable the left speaker amplifier when SPKBYP = 1. 0 = Disabled 1 = Enabled

咔嗒/噼噗声抑制

IC具有全面的咔嗒/噼噗声抑制电路，使得开启、关断及音量变化时的咔嗒/噼噗声降至最小。

在所有模拟PGA和音量控制电路采用过零检测，防止音量变化时产生较大的尖峰脉冲。器件在音频信号穿过中心点时改变音量，而不是收到指令时立即改变音量。如果在超时窗口内未检测到过零，则强制改变音量。

音量摆率控制将较大的音量变化划分成最小步进值，从初始值到最终音量设置逐步调节音量。如果使能音量摆率控制，则在器件开启和关断过程中同样控制音量变化的速率。使能输出之前，将音量设置在静音状态。一旦开启输出，音量将缓变到相应水平。关断期间，在禁止输出之前控制音量缓变到静音状态。

如果没有音频信号，过零检测可避免控制音量摆率。使能增强型音量摆率控制电路，可以防止音量控制器在建立前期设置的音量水平之前，发出另一音量调整请求。由此，每一步音量调整均发生在音频信号过零之后或超出超时窗口之后。关断期间，禁用增强型音量摆率控制。

表30. 咔嗒/噼噗声抑制寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x47	7	$\overline{\text{VS2EN}}$	**Enhanced Volume Smoothing** During volume slewing, the controller waits for each step in the ramp to be applied before sending the next step. When zero-crossing detection is enabled this prevents large steps in the output volume when no zero crossings are detected. 0 = Enabled 1 = Disabled Applies to volume changes in HPVOLL, HPVOLR, RECVOL, SPVOLL, and SPVOLR.
	6	$\overline{\text{VSEN}}$	**Volume Adjustment Smoothing** Volume changes are smoothed by stepping through intermediate steps. Also ramps the volume from minimum to the programmed value at turn-on and back to minimum at turn-off. 0 = Enabled 1 = Disabled Applies to volume changes in HPVOLL, HPVOLR, RECVOL, SPVOLL, and SPVOLR.
	5	$\overline{\text{ZDEN}}$	**Zero-Crossing Detection** Holds volume changes until there is a zero crossing in the audio signal. This reduces click and pop during volume changes (zipper noise). If no zero crossing is detected within 100ms, the volume change is forced. 0 = Enabled 1 = Disabled Applies to volume changes in PGAM1, PGAM2, PGAOUTA, PGAOUTB, PGAOUTC, HPVOLL, HPVOLR, RECVOL, SPVOLL, and SPVOLR.
	1	EQ2EN	See the *5-Band Parametric EQ* section.
	0	EQ1EN	

插孔检测

IC具有插孔检测功能，可检测插孔的插入和拔出，以及负载类型。检测到插入插孔的操作时，可触发IRQ中断(通过置位IJDET)通知微控制器。图33所示为插孔检测的典型配置。

插孔插入检测

为了检测插孔插入事件，IC必须具备一路电源。JDETEN置位将使能插孔检测电路，并向JACKSNS施加上拉电流。置位JDWK，使电源电流最小。关断或退出关断时均可插入插孔，清零JDWK可区分带有麦克风的耳麦和不带麦克风的耳机。只要JACKSNS没有负载且MICBIAS禁用，JACKSNS的电压与SPKLVDD相同。表31所示为插入插孔时JKSNS的变化。

附件按钮检测

插入插孔后，MAX98089可检测附件上的按键是否按下，包括麦克风和将麦克风信号对地短路的开关。置位JDETEN使能插孔检测电路，使能或禁用MICBIAS时均可检测按钮是否按下。表32所示为按下附件按钮时，JKSNS的变化。

插孔拔出检测

IC通过监测JACKSNS是否跳变到11状态来监测插孔是否拔出。置位JDETEN，使能插孔检测电路。如果不需要按钮检测，则置位JDWK使电源电流最小。表33所示为拔出插孔时，JKSNS的变化。关断或退出关断时，均可拔出插孔。

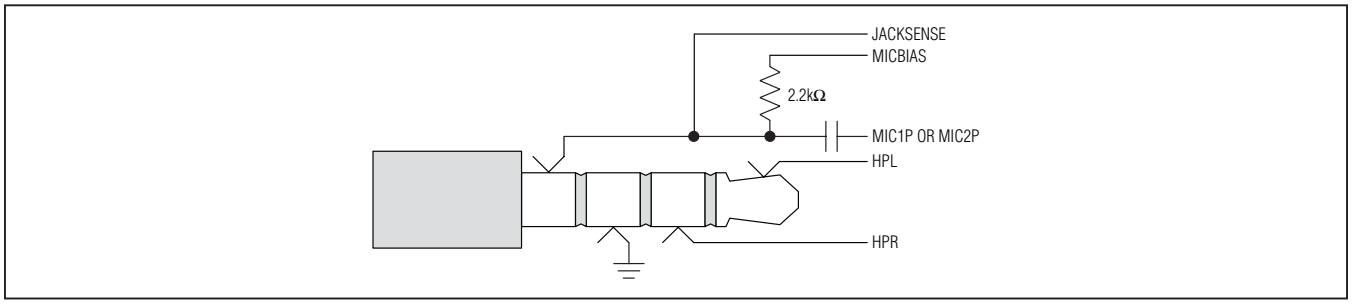


图33. 插孔检测的典型配置

表31. 插入插孔时，JKSNS的变化

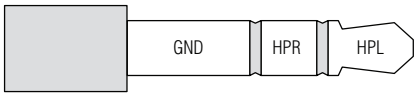
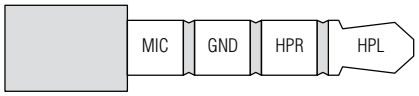
JACK TYPE	JDWK = 1	JDWK = 0
	JKSNS: 11 ➔ 00	JKSNS: 11 ➔ 00
	JKSNS: 11 ➔ 00	JKSNS: 11 ➔ 01

表32. 按下按钮时，JKSNS的变化

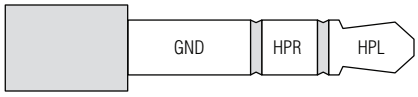
JACK TYPE	MICBIAS ENABLED OR DISABLED
	JKSNS: 01 ➔ 00

表33. 拔出插孔时，JKSNS的变化

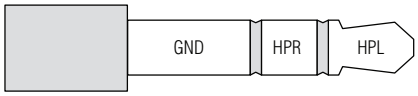
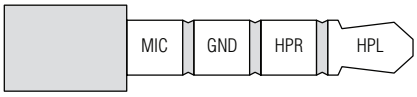
JACK TYPE	JDWK = 1 AND MICBIAS DISABLED	JDWK = 0 OR MICBIAS ENABLED
	JKSNS: 00 ➔ 11	JKSNS: 00 ➔ 11
	JKSNS: 00 ➔ 11	JKSNS: 01 ➔ 11

表34. 插孔检测寄存器

REGISTER	BIT	NAME	DESCRIPTION		
0x02 (Read Only)	7 6	JKSNS	**JACKSNS State** Reports the status of JACKSNS when JDETEN = 1.		
			VALUE	**MODE**	**DESCRIPTION**
			00	MBEN = 1	$V_{JACKSNS}$ < 0.1V x $V_{MICBIAS}$
				MBEN = 0	$V_{JACKSNS}$ < 0.1V x $V_{SPKLVDD}$
			01	MBEN = 1	0.1V x $V_{MICBIAS}$ < $V_{JACKSNS}$ < 0.95V x $V_{MICBIAS}$
				MBEN = 0	0.1V x $V_{SPKLVDD}$ < $V_{JACKSNS}$ < 0.95V x $V_{SPKLVDD}$
			10	MBEN = 1	Reserved
				MBEN = 0	Reserved
			11	MBEN = 1	0.95V x $V_{MICBIAS}$ < $V_{JACKSNS}$
				MBEN = 0	0.95V x $V_{SPKLVDD}$ < $V_{JACKSNS}$
0x4B	7	JDETEN	**Jack Detection Enable** 0 = Disabled 1 = Enabled		
	1 0	JDEB	**Jack Detection Debounce** Configures the debounce time for setting JDET. 00 = 25ms 01 = 50ms 10 = 100ms 11 = 200ms		

表34. 插孔检测寄存器(续)

REGISTER	BIT	NAME	DESCRIPTION
0x4E	7	BGEN	See the *Power Management* section.
	6	SPREGEN	See the *Power Management* section.
	5	VCMEN	See the *Power Management* section.
	4	BIASEN	See the *Power Management* section.
	0	JDWK	**JACKSNS Pullup** When JDWK = 1, JACKSNS is slow to increase in voltage. Set JDWK = 0 before setting JDETEN = 1 to prevent false detection. Valid when MBIAS = 0. 0 = 2.4kΩ to SPKLVDD (allows microphone detection) 1 = 5µA to SPKLVDD (minimizes supply current)

电池测量

IC测量作用在SPKLVDD的电压(通常为电池电压)，并将测量值储存到寄存器0x03。扬声器抑制电路利用该数值设置精确的门限电压。禁用电池测量功能时，用户可设置电池电压。

表35. 电池测量寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x03	4 3 2 1 0	VBAT	**Battery Voltage** Read VBAT when VBATEN = 1 to determine $V_{SPKLVDD}$. Program VBAT when V_{BATEN} = 0 to allow proper speaker amplifier signal processing. Calculate/program the battery voltage using the following formula: $V_{BATTERY}$ = 2.55V + [VBAT/10]
0x51	7	$\overline{SHDN}$	See the *Power Management* section.
	6	VBATEN	**Battery Measurement Enable.** Enables an internal ADC to measure $V_{SPKLVDD}$. 0 = Disabled (register 0x03 readable and writeable) 1 = Enabled (register 0x03 read only)
	3	PERFMODE	See the *Power Management* section.
	2	HPPLYBCK	See the *Power Management* section.
	1	PWRSV8K	See the *Power Management* section.
	0	PWRSV	See the *Power Management* section.

器件状态

IC利用寄存器0x00和IRQ报告器件各种功能的状态。发生某个事件时，置位相应的状态寄存器位，读取寄存器后清零。可通过轮询寄存器0x00或将IRQ配置成发生特定事件时拉低，以确定器件状态。IRQ为开漏输出，需要上拉电阻才能正常工作。寄存器0x0F确定状态寄存器的哪些位触发IRQ，将其拉低。

表36. 状态和中断寄存器

REGISTER	BIT	NAME	DESCRIPTION
0x00 (Read Only)	7	CLD	**Full Scale** 0 = All digital signals are less than full scale. 1 = The DAC or ADC signal path has reached or exceeded full scale. This typically indicates clipping.
	6	SLD	**Volume Slew Complete** SLD reports that any of the programmable-gain arrays or volume controllers has completed slewing from a previous setting to a new programmed setting. If multiple gain arrays or volume controllers are changed at the same time, the SLD flag is set after the last volume slew completes. SLD also reports when the digital audio interface soft-start or soft-stop process has completed. MCLK is required for proper SLD operation. 0 = No volume slewing sequences have completed since the status register was last read. 1 = Volume slewing complete.
	5	ULK	**Digital Audio Interface Unlocked** 0 = Both digital audio interfaces are operating normally. 1 = Either digital audio interface is configured incorrectly or receiving invalid clocks.
	1	JDET	**Jack Configuration Change** JDET reports changes to any bit in the Jack Status register (0x02). Changes to the Jack Status bits are debounced before setting JDET. The debounce period is programmable using the JDEB bits. JDET is always set the first time JDETEN or SHDN is set the first time power is applied to the IC. Read the status register following such an event to clear JDET and allow for proper jack detection. 0 = No change in jack configuration. 1 = Jack configuration has changed.
0x0F	7	ICLD	**Full-Scale Interrupt Enable** 0 = Disabled 1 = Enabled
	6	ISLD	**Volume Slew Complete Interrupt Enable** 0 = Disabled 1 = Enabled
	5	IULK	**Digital Audio Interface Unlocked Interrupt Enable** 0 = Disabled 1 = Enabled
	1	IJDET	**Jack Configuration Change Interrupt Enable** 0 = Disabled 1 = Enabled

器件版本

表37. 器件版本寄存器

REGISTER	BIT	NAME	DESCRIPTION
0xFF (Read Only)	7	REV	**Device Revision Code** REV is always set to 0x40.
	6		
	5		
	4		
	3		
	2		
	1		
	0		

I²C串行接口

IC采用I²C/SMBus™兼容的2线串行接口，包括一根串行数据线(SDA)和一根串行时钟线(SCL)。SDA和SCL的时钟速率高达400kHz，方便了IC和主机之间的通信。图5所示为2线接口的时序图。主机在总线上产生SCL并发起数据传输。主机发送相应的从地址和寄存器地址，随后是发送的数据字，由此向IC写入数据。每次传输都以START (S)或REPEATED START (Sr)条件和STOP (P)条件打包成帧。发送给IC的每个字长为8位，其后是应答时钟脉冲。主机从IC读取数据时发送相应的从地址，随后是9个SCL脉冲。IC通过SDA发送数据，与主机产生的SCL脉冲同步。主机在接收到每字节数据后对其进行应答。每次读操作由START或REPEATED START条件、非应答和STOP条件打包成帧。SDA既是输入又是开漏输出，SDA需要一个上拉电阻，通常大于500Ω。SCL仅作为输入，如果总线上有多个主机，或者单主机具有开漏SCL输出，SCL也将需要一个上拉电阻，通常大于500Ω。SDA和SCL总线串联电阻可选。串联电阻保护IC的数字输入免受总线上高压毛刺的冲击，并最大程度地降低总线信号的串扰和下冲。

位传输

每个SCL周期传输一位数据。在SCL脉冲的高电平期间内，SDA上的数据必须保持稳定。当SCL为高电平时，SDA的变化为控制信号(请参见*START和STOP条件*部分)。

START和STOP条件

总线空闲时，SDA和SCL的空闲状态为高电平。主机通过发送START条件启动通信，START条件是SCL为高电平时，SDA由高到低的跳变。STOP条件是SCL为高电平时，SDA由低到高的跳变(图33)。来自主机的START条件通知IC开始传输。主机通过发送STOP条件终止传输并释放总线。如果产生的是REPEATED START条件(而不是STOP条件)，则总线保持有效。

提前STOP条件

IC在数据传输期间可随时识别STOP条件，除非STOP条件与START条件出现在同一高电平脉冲。为确保正常工作，请勿在START条件的同一SCL高电平脉冲期间发送STOP条件。

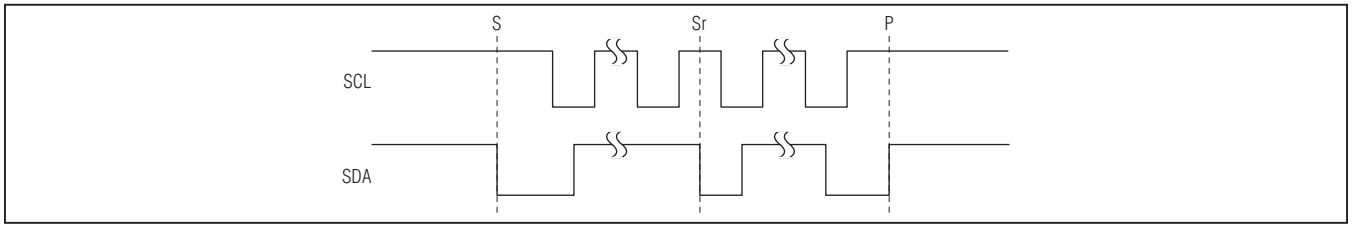


图34. START、STOP和REPEATED START条件

SMBus是Intel Corp.的商标。

从地址

从地址定义为7个最高位(MSB)，后边跟读/写控制位。对于该IC，7个最高位为0010000。将读/写控制位设置为1(从地址 = 0x21)，使IC配置为读模式；将读/写控制位设置为0 (从地址 = 0x20)，使IC配置为写模式。该地址是在START条件后发送到IC的第一个字节。

应答

写操作中，应答位(ACK)是第9个时钟位，是IC对其接收的每个数据字节的握手信号(图35)。如果成功接收了之前的字节，那么IC在主控制器产生的第9个时钟脉冲期间拉低SDA。监测ACK可以检测失败的数据传输。如果接收器件忙，或者系统发生故障，则会导致数据传输失败。数据传输失败时，总线主机会重新开始通信。当IC处于读操作时，在第9个时钟脉冲期间，主控制器拉低SDA，以应答数据接收。每次读取字节后，主机均发送应答信号，以便继续传输数据。当主机从IC读取数据的最后一个字节时，发送非应答，随后是STOP条件。

写数据格式

对IC的写操作包括：START条件、从机地址(R/$\overline{W}$位置0)、配置内部寄存器地址指针的一个数据字节、1个或多个数据字节和STOP条件。图36所示为向IC写入1个字节数据时的正确帧格式，图37所示为向IC写入n个字节数据时的帧格式。

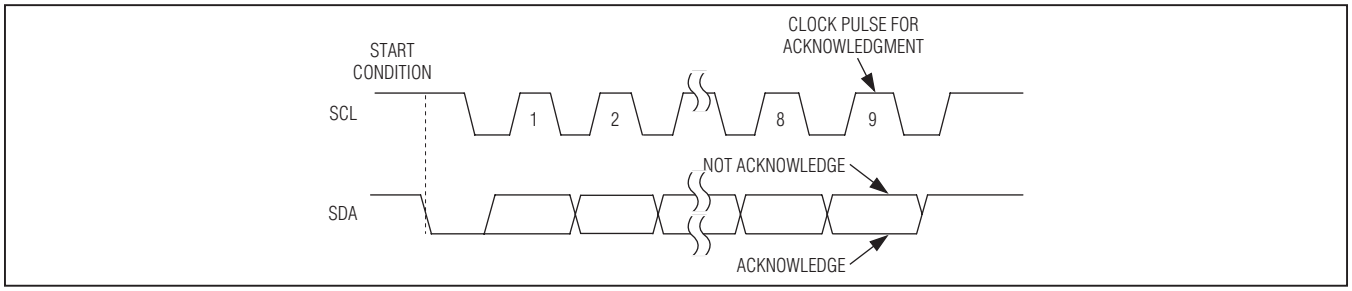


图35. 应答

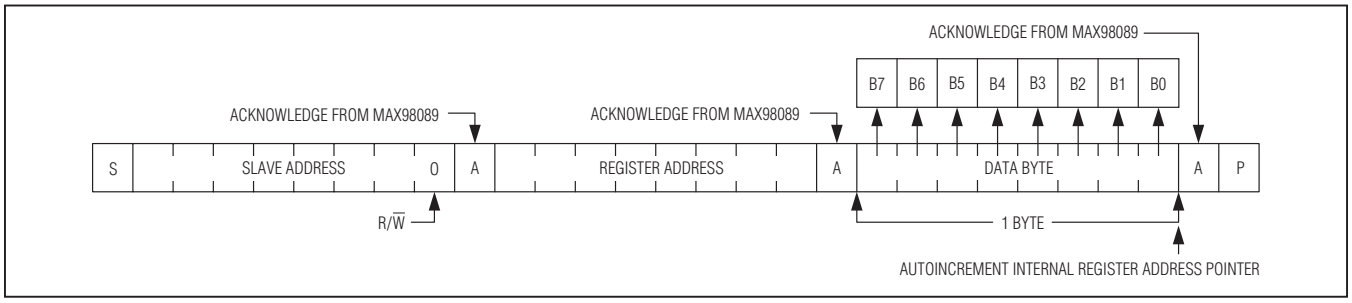


图36. 向IC写入1个数据字节

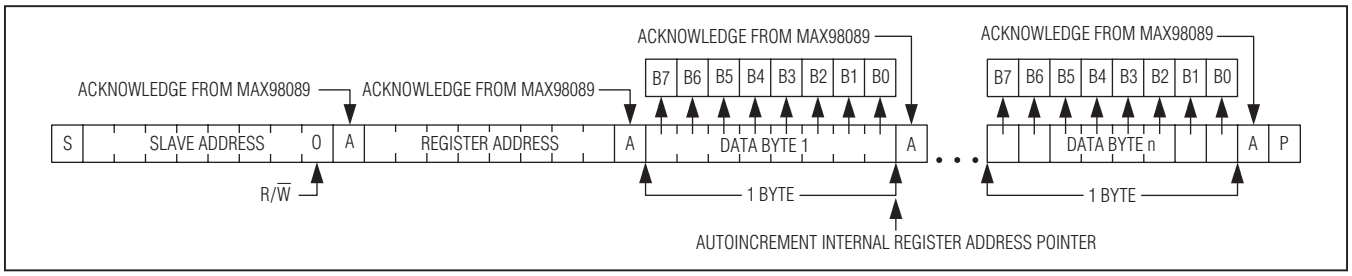


图37. 向IC写入n个数据字节

R/$\overline{W}$位置0的从地址表示主控制器要向IC写入数据。IC在主控制器产生的第9个SCL脉冲期间应答接收到的地址。

从主控制器发送的第二字节配置IC的内部寄存器地址指针，指针告诉IC要写入的下一个字节的位置。接收到地址指针数据后，IC发送一个应答脉冲。

发送到IC的第三字节为写入指定寄存器的数据。IC发送应答脉冲表示接收到数据字节，每次接收数据之后，地址指针自动递增至下一个寄存器地址。自动递增功能使主机能够在一个连续帧内连续进行寄存器写操作。主机通过发送STOP条件终止传输。0xC7以上的寄存器地址被保留，不要对这些地址进行写操作。

读数据格式

通过发送从地址，并将R/$\overline{W}$位置1，启动读操作。IC在第9个SCL时钟脉冲期间拉低SDA，应答接收到的从地址。START条件之后为读命令，将地址指针复位到寄存器0x00。

从IC发送的第一个字节是寄存器0x00的内容。发送数据在SCL的上升沿有效，地址指针在每次读取数据字节后都自动递增。这种自动递增功能使得在一个连续帧内可以连续读取全部寄存器的内容。读数据字节任何时刻都可发送STOP条件。如果发送了一个STOP条件，随后是另一个读操作，则读取的第一个字节为寄存器0x00的数据。

发送读命令之前，可将地址指针预设为某个特定的寄存器。主机预设地址指针时，首先发送IC的从地址，并将R/$\overline{W}$位置0，随后跟寄存器地址。然后发送一个REPEATED START条件和从地址，并将R/$\overline{W}$位置1。随后，IC将传输指定寄存器的内容。地址指针在传输完第一个字节后自动递增。

主机在接收到每个读字节之后的应答时钟脉冲期间进行应答。主机必须应答除最后一个字节以外所有正确接收的字节。最后一个字节之后必须是来自主机的非应答，然后是STOP条件。图38所示为从IC读取1个字节时的帧格式，图39所示为从IC读取多个字节时的帧格式。

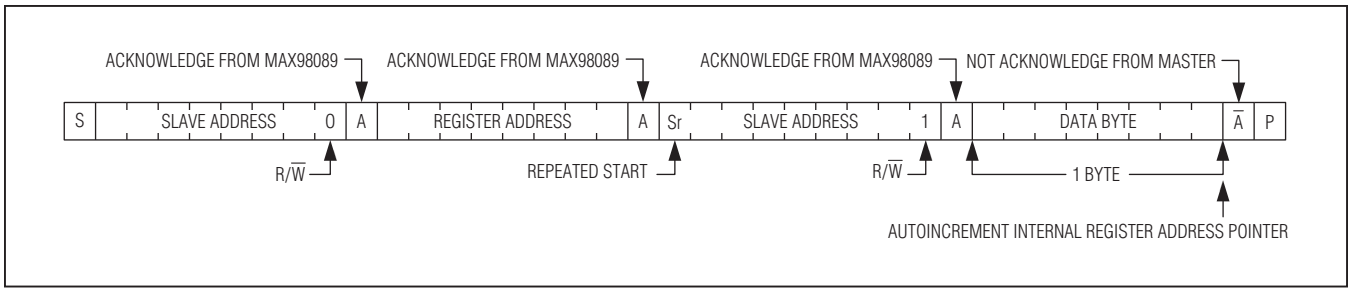


图38. 从IC读取1个字节的数据

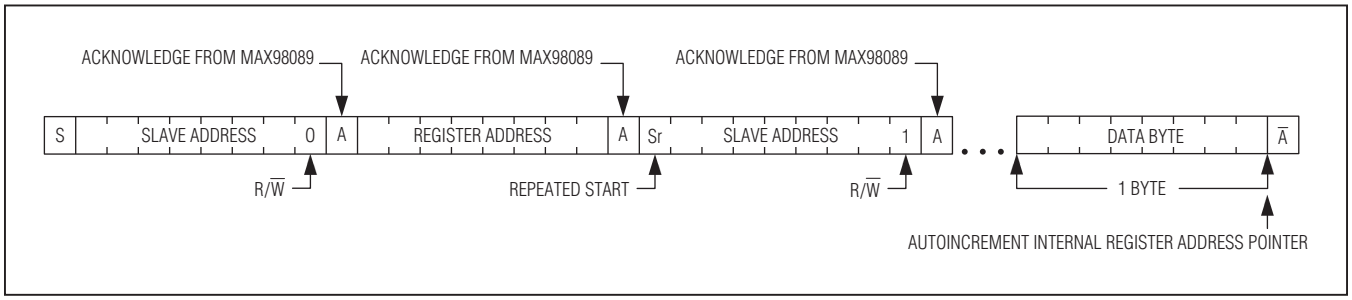


图39. 从IC读取n个字节的数据

应用信息

典型工作电路

图40和图41所示为IC工作电路示例，图中外部元件为IC工作的最低要求。根据应用的不同，可能需要其它元件。

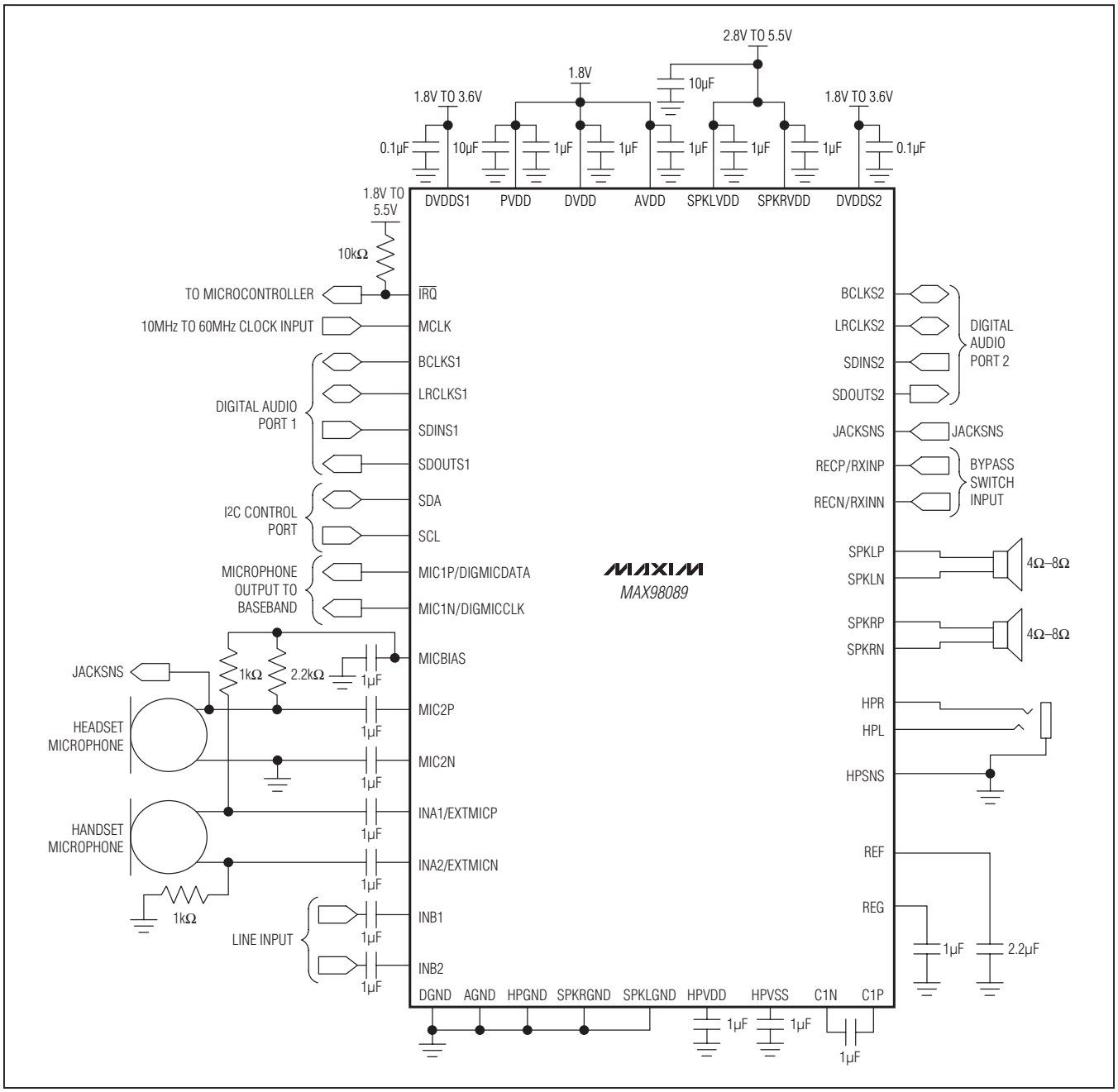


图40. 使用模拟麦克风输入和旁路开关的典型应用电路

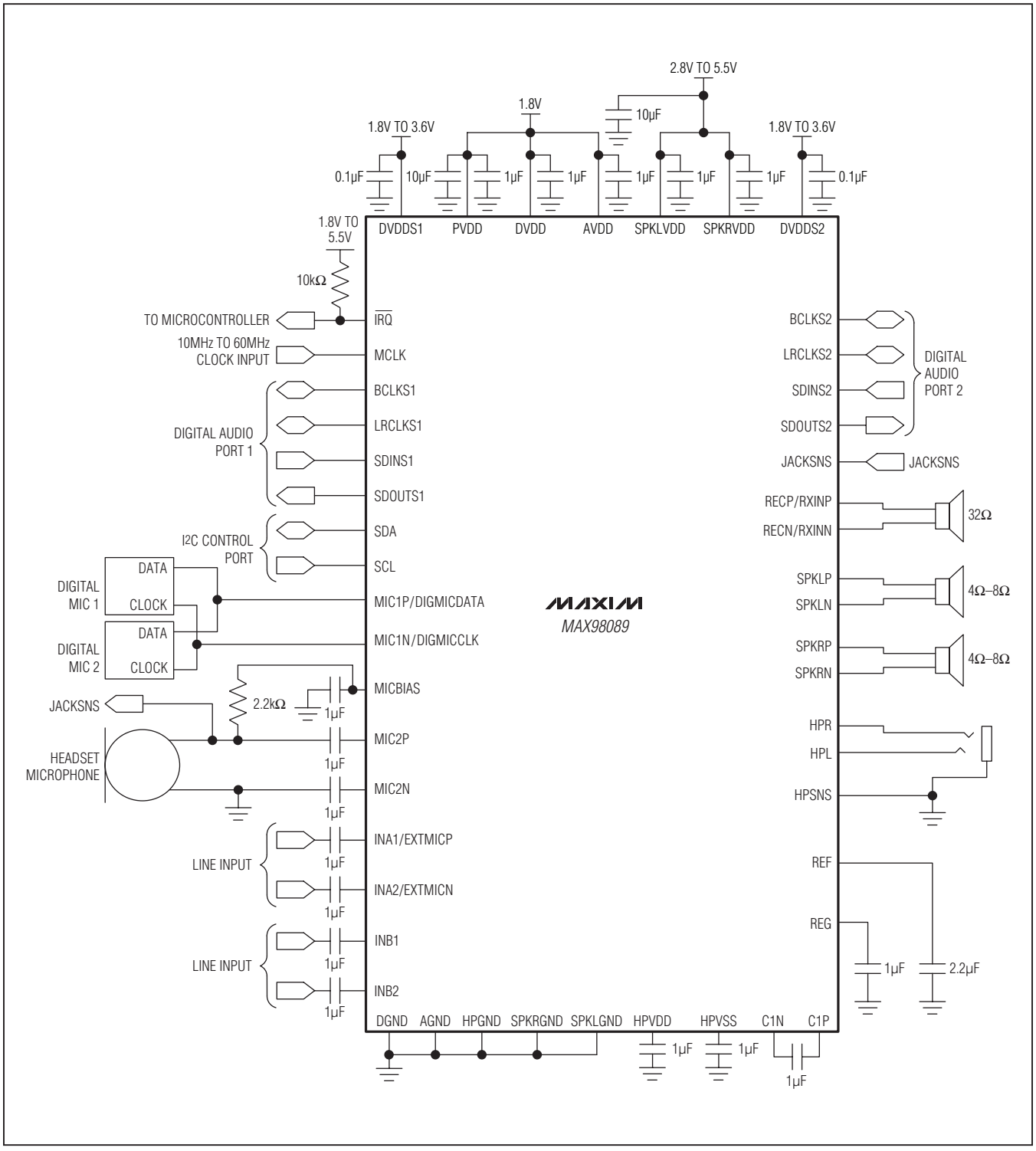


图41. 使用数字麦克风输入和接收放大器的典型应用电路

无需滤波器的D类放大器

传统的D类放大器需要外部滤波器从放大器输出中恢复音频信号。滤波器增加了系统成本并增大了方案尺寸，同时也会降低效率和THD+N性能。传统的PWM架构提供较大的差分输出摆幅(峰–峰值为2 x V_{DD})，并产生了较大的纹波电流。滤波元件中的任何寄生电阻都会造成功率损耗，降低效率。

该IC无需输出滤波器，器件依靠扬声器线圈的固有电感以及扬声器和人耳的天然滤波特性从方波输出中恢复音频信号。由于省去了输出滤波器，使得方案尺寸更小、成本更低、效率更高。

由于IC的输出频率恰好超出绝大多数扬声器的带宽，方波频率造成的音圈偏移非常小。尽管偏移很小，如果扬声器设计不能处理额外的功率，也有可能导致设备损坏。为优化性能，可选用串联电感大于10µH的扬声器。典型的8Ω扬声器，其串联电感通常在20µH至100µH范围内。

RF敏感度

GSM无线电利用时分多址(TDMA)以217Hz间隔发射。形成的射频信号以217Hz强幅值调制，其谐波很容易被音频放大器解调。IC特别针对抑制射频信号进行了设计；然而，PCB布局对最终产品的敏感度影响很大。

射频应用中，布局及元件选择的改善可减小IC对射频噪声的敏感度，防止射频信号被解调为音频噪声。走线长度应保持短于相应射频波长的1/4。将走线长度最小化，防止走线形成天线并将射频信号耦合进IC。以米为单位的波长(λ)由下式给出：λ = c/f，其中c = 3 x 10^8 m/s，f = 射频频率。

将音频信号布在PCB的中间层，使其上、下的接地区域将其屏蔽，防止射频干扰。理想情况下，PCB的顶层和底层应主要为接地区域，产生有效屏蔽。

由于电容的频率响应与陷波滤波器相似，所以利用电容的自谐频率可获得更大的射频抗扰性。根据制造商的不同，10pF至20pF电容通常在相应射频频率处呈现自谐。将这些电容安装在输入引脚时，可有效地将射频噪声短路至地。为了使这些电容有效工作，它们必须具有低阻、低感通路连接至接地区域。尽量避免使用微过孔连接至接地区域，因为这些过孔在射频频率下传导不良。

启动/关断排序

为了确保器件初始化及咔嗒/噼噗声最小化，在配置所有寄存器后，将IC设置为$\overline{SHDN}$ = 1。表38所示为器件的启动顺序示例。为了关断IC，只需设置$\overline{SHDN}$ = 0。

表38. 启动顺序示例

SEQUENCE	DESCRIPTION	REGISTERS
1	Ensure $\overline{SHDN}$ = 0	0x51
2	Configure clocks	0x10 to 0x13, 0x19 to 0x1B
3	Configure digital audio interface	0x14 to 0x17, 0x1C to 0x1F
4	Configure digital signal processing	0x18, 0x20, 0x3F to 0x46
5	Load coefficients	0x52 to 0xC9
6	Configure mixers	0x22 to 0x2D
7	Configure gain and volume controls	0x2E to 0x3E
8	Configure miscellaneous functions	0x47 to 0x4B
9	Enable desired functions	0x4C, 0x50
10	Set $\overline{SHDN}$ = 1	0x51

器件工作时，可更改IC中的许多配置选项，然而，有些寄存器只应在禁用相应音频通路时进行调节。表39列出了工作期间敏感的寄存器。更改这些寄存器时，要么禁用相应的音频通路，要么设置$\overline{SHDN}$ = 0。

元件选择

可选磁珠滤波器

如果扬声器引线超过20mm，采用磁珠及接地电容的滤波器结构，可实现进一步EMI抑制(图42)。磁珠应具有低直流电阻、高频(> 600MHz)阻抗(100Ω至600Ω)，额定值至少为1A。电容值根据所选的磁珠及实际扬声器引线长度变化。根据EMI性能，选择小于1nF的电容。

输入电容

输入电容C_{IN}结合IC线入的输入阻抗，形成高通滤波器，消除模拟输入信号中的直流偏压。交流耦合电容允许放大器自动偏置至最优直流水平。如果源阻抗为零，高通滤波器的–3dB点由下式给出：

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

所选C_{IN}的f_{-3dB}恰好低于感兴趣的最低频率。为了获得最佳音质，使用具有低电压系数电介质的电容，例如钽电容或铝电解电容。具有高电压系数的电容，例如陶瓷电容，低频时可能会增大失真。

电荷泵电容选择

选择ESR小于100mΩ的电容，以获得最佳性能。低ESR陶瓷电容最小化电荷泵的输出电阻。大多数表贴陶瓷电容满足ESR要求。为在扩展级温度范围内获得最佳性能，选择采用X7R电介质的电容。

表39. 工作期间对更改敏感的寄存器

REGISTER	DESCRIPTION
0x10 to 0x13, 0x19 to 0x1B	Clock Control Registers
0x14 to 0x17, 0x1C to 0x1F	Digital Audio Interface Configuration
0x18, 0x20	Digital Passband Filters
0x25 to 0x2D	Analog Mixers
0x52 to 0xC9	Digital Signal Processing Coefficients

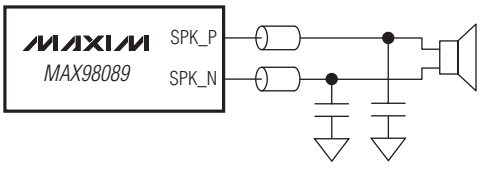


图42. 可选D类磁珠滤波器

电荷泵飞电容

飞电容(连接在C1N和C1P之间)的值影响电荷泵的输出电阻。太小的值影响器件提供足够电流驱动的能力，造成输出电压降低。增大飞电容的值则在一定程度上降低电荷泵的输出电阻。1µF以上，内部开关的导通电阻和外部电荷泵电容的ESR起主要作用。

电荷泵保持电容

保持电容(旁路HPVSS至HPGND及HPVDD至HPGND)值和ESR直接影响HPVSS和HPVDD处的纹波。增大电容值减小输出纹波。同样，降低ESR将减小纹波和输出电阻。在最大输出功率较低的系统中，可使用较小的电容值。更多信息请参见*典型工作特性*部分的输出功率和负载电阻关系图。

不使用的引脚

表40列出了不使用电路模块时如何连接IC引脚。

表40. 不使用的引脚

NAME	CONNECTION	NAME	CONNECTION
SPKRP	Unconnected	INB1	Unconnected
SPKRVDD	Always connect	INA2/MICEXTN	Unconnected
SPKLVDD	Always connect	LRCLKS2	Unconnected
SPKLP	Unconnected	MCLK	Always connect
RECN/RXINN	Unconnected	SDINS2	AGND
HPVDD	Unconnected	$\overline{IRQ}$	Unconnected
C1P	Unconnected	MIC1P/DIGMICDATA	Unconnected
HPGND	AGND	INA1/MICEXTP	Unconnected
SPKRN	Unconnected	DGND	Always connect
SPKRGND	Always connect	BCLKS2	Unconnected
SPKLGND	Always connect	SDA	Always connect
SPKLN	Unconnected	SCL	Always connect
RECP/RXINP	Unconnected	REG	Always connect
C1N	Unconnected	REF	Always connect
HPL	Unconnected	MIC1N/DIGMICCLK	Unconnected
HPVSS	Unconnected	MIC2P	Unconnected
SDINS1	AGND	SDOUTS2	Unconnected
LRCLKS1	Unconnected	DVDDS2	DVDD
HPSNS	AGND	DVDD	Always connect
INB2	Unconnected	AVDD	Always connect
HPR	Unconnected	PVDD	Always connect
DVDDS1	DVDD	AGND	Always connect
SDOUTS1	Unconnected	MICBIAS	Unconnected
BCLKS1	Unconnected	MIC2N	Unconnected
JACKSNS	Unconnected		

推荐的PCB布线

MAX98089EWY采用63焊球WLP封装。图43所示为如何利用3层PCB连接全部有效焊球的例子。为确保不断开地回路，利用第2层作为第1层和第3层之间的连接层，并将其余区域作为接地区域。

LAYER 1

LAYER 2

LAYER 3

图43. 推荐的MAX98089EWY布线

电源旁路、布局和接地

适当的布局和接地对获得最佳性能至关重要。设计IC的PCB时，适当的电路隔离可以将IC的模拟部分与数字部分分开。这样保证了模拟音频走线不会出现在数字走线附近。

在PCB的专用层上使用大面积连续接地层可以最小化环路面积。采用尽可能短的走线将AGND、DGND、HPGND、SPKLGND和SPKRGND直接连接至接地区域。适当的接地可改善音频性能、最大程度降低通道之间的串扰，并可防止数字噪声耦合至模拟音频信号。

以最短的走线长度将MICBIAS、REG和REF上的旁路电容直接连接至接地区域。还要确保连接至AGND的通路长度最短。将AVDD直接旁路至AGND。

以最短的通路长度，将端接至接地层的所有数字I/O端子连接至DGND。将DVDD、DVDDS1和DVDDS2直接旁路至DGND。

使C1P和C1N之间的电容尽量靠近IC，以将C1P至C1N的走线长度降至最短。C1P和C1N之间增加的电感和电容降低耳机放大器的输出功率。利用电容旁路HPVDD和HPVSS，电容靠近HPVSS，采用短走线连接至HPGND。关闭HPVSS的去耦将电源纹波最小化、耳机放大器输出功率最大化。

HPSNS检测耳机插孔上的地噪声，并将相同噪声加至输出音频信号，从而使输出(耳机输出减去地)无噪声。将HPSNS连接至耳机插孔屏蔽，确保精确检测耳机地噪声。

分别将SPKLVDD和SPKRVDD旁路至SPKLGND和SPKRGND，走线尽量短。将SPKLP、SPKLN、SPKRP和SPKRN连接至立体声扬声器，走线尽量短。降低走线长度最小化辐射EMI。在PCB上将SPKLP/SPKLN和SPKRP/SPKRN布置为差分对，将环路面积最小化，进而将电路电感最小化。如果在扬声器输出上使用滤波元件，确保使其尽量靠近IC，保证最大作用。将任何接地有源元件与SPKLGND和SPKRGND的连接走线长度最小化，进一步减小EMI。

把麦克风至IC的麦克风信号以差分对方式布线，确保正和负信号尽可能靠近、并且具有相同的走线长度。当使用单端麦克风或其它单端音频源时，在尽量靠近音频源的位置将麦克风负输入接地，然后将正和负走线作为差分对。

现备有一个评估板(EV kit)，可作为IC的PCB布局实例。利用该评估板可快速设置IC，并提供了易于使用的软件，用于控制其内部寄存器。

WLP应用信息

关于WLP结构、尺寸、载带信息、PCB工艺、焊球布局以及推荐的回流温度特性的最新应用信息，以及可靠性测试结果的最新信息，请参见应用笔记1891：*晶片级封装(WLP)及其应用*。图44所示为MAX98089EWY使用的WLP焊球尺寸。

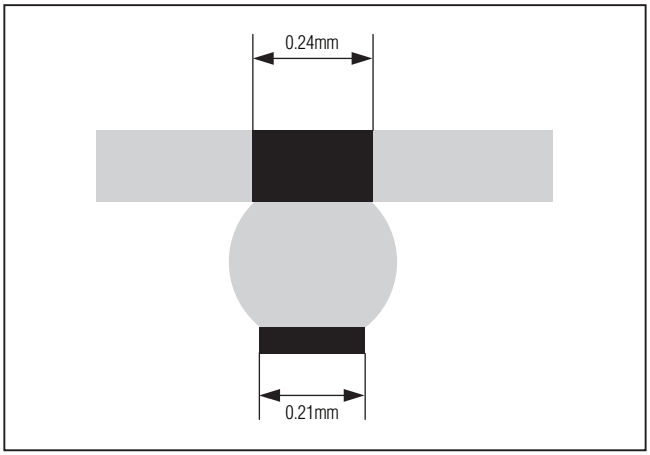


图44. MAX98089EWY WLP焊球尺寸

定购信息

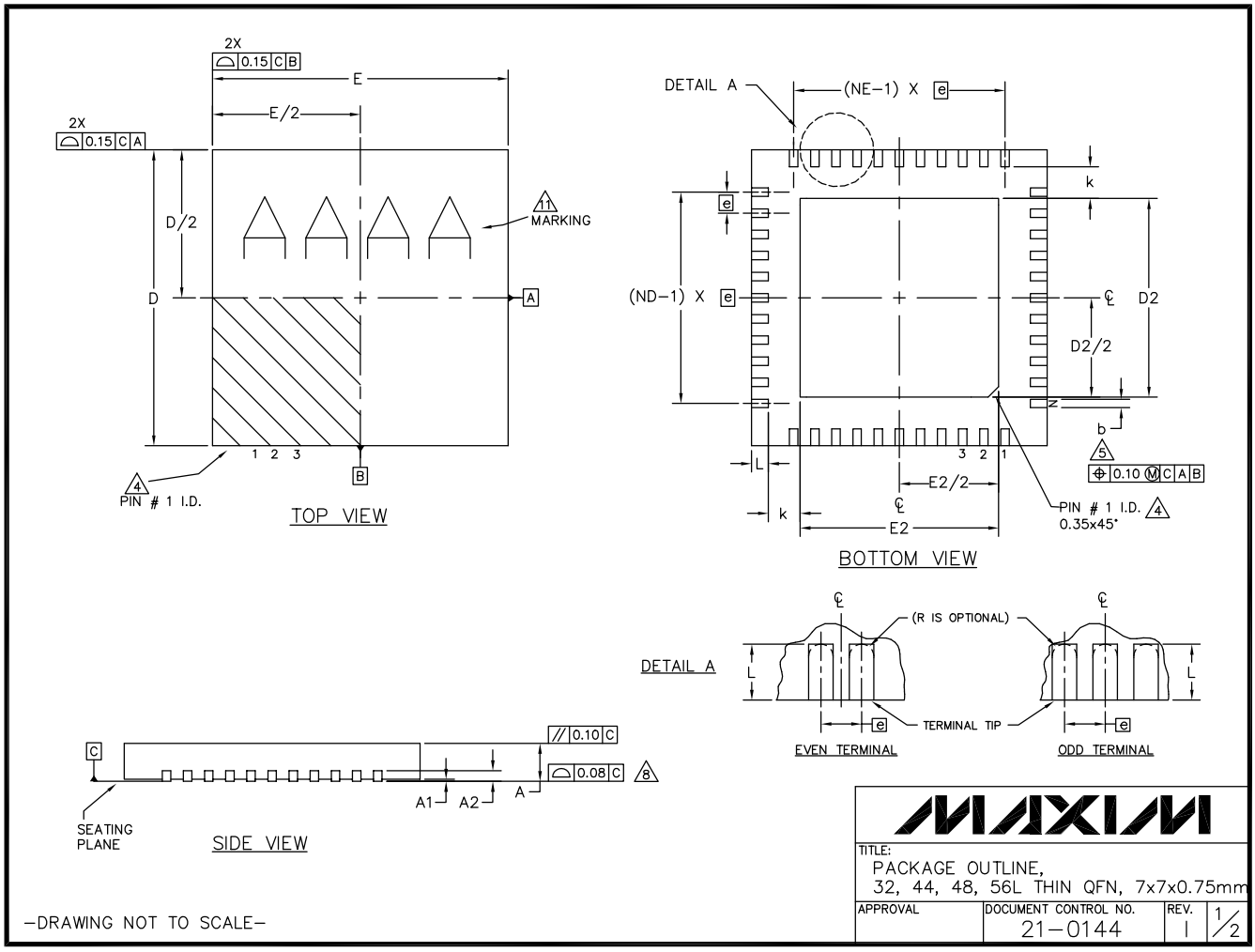
PART	TEMP RANGE	PIN-PACKAGE
MAX98089EWY+T	-40°C to +85°C	63 WLP
MAX98089ETN+T	-40°C to +85°C	56 TQFN-EP*

T = 卷带包装。
+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*

封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
56 TQFN	T5677+1	**21-0144**	**90-0042**
63 WLP	W633A3+1	**21-0462**	—



封装信息(续)

如需最近的封装外形信息和焊盘布局(占位面积)，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877-4	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877M-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877M-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877MN-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877N-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677MN-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-2	–	5.40	5.50	5.60	5.40	5.50	5.60	–

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-3/-4/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

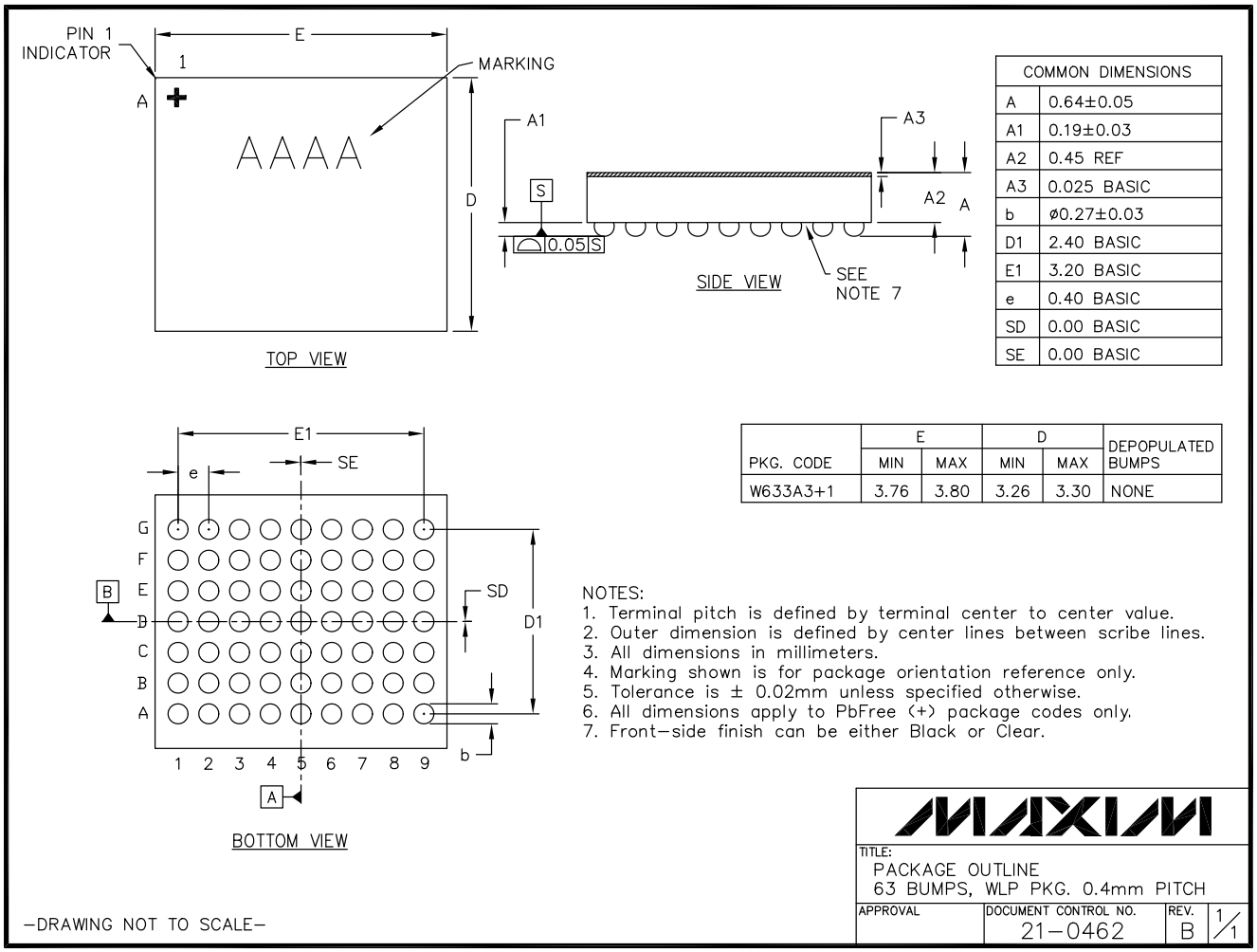
MAXIM

TITLE:
PACKAGE OUTLINE,
32, 44, 48, 56L THIN QFN, 7x7x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	I	2/2

封装信息(续)

如需最近的封装外形信息和焊盘布局(占位面积)，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。



COMMON DIMENSIONS	
A	0.64±0.05
A1	0.19±0.03
A2	0.45 REF
A3	0.025 BASIC
b	ø0.27±0.03
D1	2.40 BASIC
E1	3.20 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W633A3+1	3.76	3.80	3.26	3.30	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front-side finish can be either Black or Clear.

MAXIM

TITLE:
PACKAGE OUTLINE
63 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0462	B	1/1

修订历史

修订号	修订日期	说明	修改页
0	6/11	最初版本。	—
1	3/12	在*Electrical Characteristics*表中为DAC至接收放大器通路部分增加了输出失调电压一栏；更新了侧音部分。	13, 14, 77, 78, 114

Maxim北京办事处
北京8328信箱 邮政编码100083
免费电话：800 810 0310
电话：010–6211 5199
传真：010–6211 5299