EVALUATION KIT AVAILABLE

19-0576; Rev 1; 8/08

MAX7456

集成了EEPROM的单通道、单色随屏显示器

概述

MAX7456单通道、单色随屏显示(OSD)发生器省去了外部视频驱动器、同步分离器、视频开关以及EEPROM，有效降低系统成本。MAX7456采用符合NTSC和PAL制式的256个用户可编程字符，适合全球市场。MAX7456能够方便地以任意字符、尺寸显示各种信息，例如公司标识、常用图形、时间、日期等。MAX7456预先装载了256个字符和图形，并可通过SPI™接口进行在线编程。

MAX7456提供28引脚TSSOP封装，工作于扩展级(-40°C至+85°C)温度范围。

应用

安全监控系统

安全监控摄像机

工业应用

室内娱乐系统

消费类电子

引脚配置在数据资料的最后给出。

SPI是Motorola, Inc.的商标。

特性

- ♦ 256个用户定义字符或图形存储于EEPROM
- ♦ 字符大小为12 x 18象素
- ♦ 闪烁、反色和背景控制字符
- ♦ 可逐行设置亮度
- ♦ 最多显示16行 x 30列字符
- ♦ 视频驱动器输出带有衰减补偿
- ♦ LOS、$\overline{VSYNC}$、$\overline{HSYNC}$和时钟输出
- ♦ 内置同步发生器
- ♦ 兼容于NTSC和PAL
- ♦ SPI兼容串行接口
- ♦ 出厂时带有预先编程的字符组

定购信息

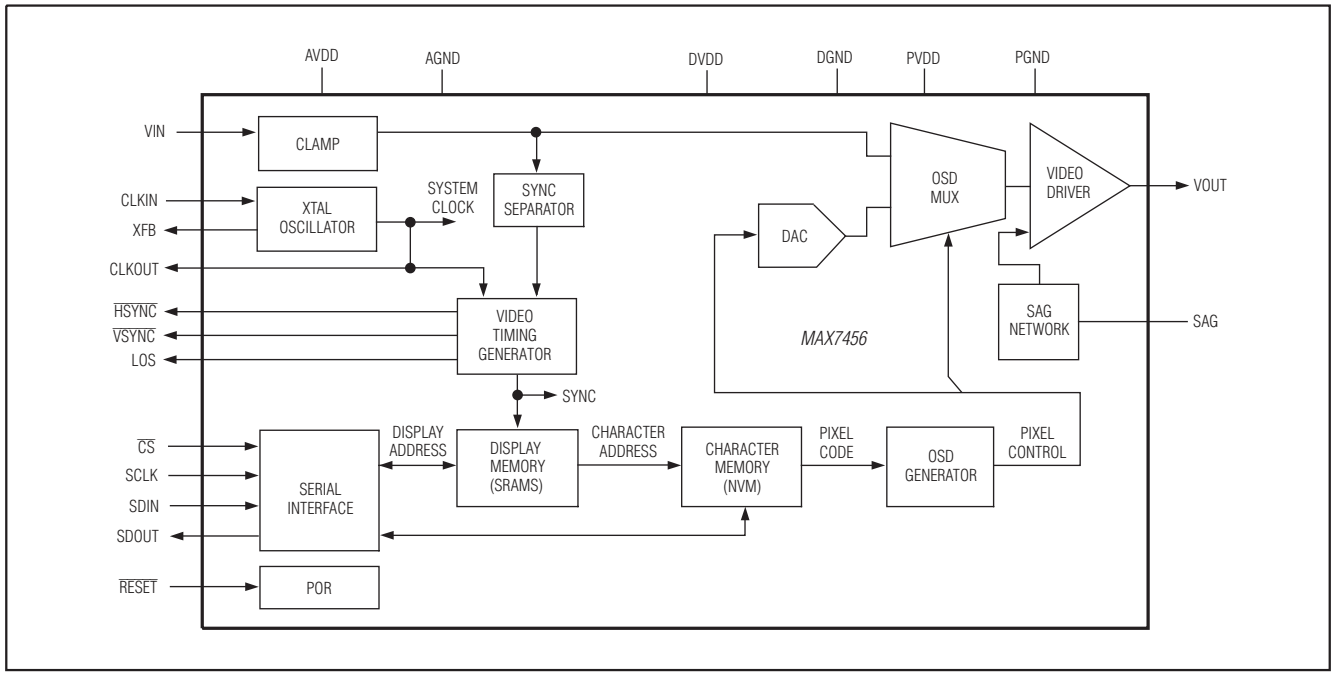
PART	PIN-PACKAGE	LANGUAGE
MAX7456EUI+	28 TSSOP-EP*	English/ Japanese

**EP = 裸焊盘。*

+表示无铅/符合RoHS标准的封装。

***注：** 该器件工作于-40°C至+85°C温度范围。*

简化功能框图



本文是英文数据资料的译文，文中可能存在翻译上的不准确或错误。如需进一步确认，请在您的设计中参考英文资料。

有关价格、供货及订购信息，请联络Maxim亚洲销售中心：10800 852 1249 (北中国区)，10800 152 1249 (南中国区)，或访问Maxim的中文网站：china.maximintegrated.com。

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.3V to +6V
DVDD to DGND .....-0.3V to +6V
PVDD to PGND .....-0.3V to +6V
AGND to DGND .....-0.3V to +0.3V
AGND to PGND .....-0.3V to +0.3V
DGND to PGND .....-0.3V to +0.3V
VIN, VOUT, SAG to AGND .....-0.3V to (V_{AVDD} + 0.3V)
$\overline{HSYNC}$, $\overline{VSYNC}$, LOS to AGND .....-0.3V to +6V
$\overline{RESET}$ to AGND .....-0.3V to (V_{AVDD} + 0.3V)
CLKIN, CLKOUT, XFB to DGND .....-0.3V to (V_{DVDD} + 0.3V)
SDIN, SCLK, $\overline{CS}$, SDOUT to DGND .....-0.3V to (V_{DVDD} + 0.3V)
Maximum Continuous Current into V_{OUT} .....±100mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (derate 27mW/°C above +70°C) 2162mW*
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

**As per JEDEC51 Standard (Multilayer Board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +4.75V to +5.25V, V_{PVDD} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{AVDD} = V_{DVDD} = V_{PVDD} = +5V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Analog Supply Voltage	V_{AVDD}		4.75	5	5.25	V
Digital Supply Voltage	V_{DVDD}		4.75	5	5.25	V
Driver Supply Voltage	V_{PVDD}		4.75	5	5.25	V
Analog Supply Current	I_{AVDD}	V_{IN} = 1V_{P-P} (100% white flat field signal), VOUT load, R_L = 150Ω		24	35	mA
Digital Supply Current	I_{DVDD}	V_{IN} = 1V_{P-P} (100% white flat field signal), VOUT load, R_L = 150Ω		25	30	mA
Driver Supply Current	I_{PVDD}	V_{IN} = 1V_{P-P} (100% white flat field signal), VOUT load, R_L = 150Ω		58	80	mA
NONVOLATILE MEMORY						
Data Retention		T_A = +25°C		100		Years
Endurance		T_A = +25°C		100,000		Stores
DIGITAL INPUTS ($\overline{CS}$, SDIN, $\overline{RESET}$, SCLK)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYS}			50		mV
Input Leakage Current		V_{IN} = 0 or V_{DVDD}			±10	µA
Input Capacitance	C_{IN}			5		pF
DIGITAL OUTPUTS (SDOUT, CLKOUT, $\overline{VSYNC}$, $\overline{HSYNC}$, LOS)						
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA (SDOUT, CLKOUT)	2.4			V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.45	V
Tri-State Leakage Current		SDOUT, $\overline{CS}$ = V_{DVDD}			±10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +4.75V to +5.25V, V_{PVDD} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{AVDD} = V_{DVDD} = V_{PVDD} = +5V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUT (CLKIN)						
Clock Frequency				27		MHz
Clock-Pulse High			14			ns
Clock-Pulse Low			14			ns
Input High Voltage			0.7 x V_{DVDD}			V
Input Low Voltage					0.3 x V_{DVDD}	V
Input Leakage Current		V_{IN} = 0V or V_{DVDD}			±50	µA
CLOCK OUTPUT (CLKOUT)						
Duty Cycle		5pF and 10kΩ to DGND	40	50	60	%
Rise Time		5pF and 10kΩ to DGND		3		ns
Fall Time		5pF and 10kΩ to DGND		3		ns
VIDEO CHARACTERISTICS						
DC Power-Supply Rejection		V_{AVDD} = V_{DVDD} = V_{PVDD} = 5V; V_{IN} = 1V_{P-P}, measured at VOUT		40		dB
AC Power-Supply Rejection		V_{AVDD} = V_{DVDD} = V_{PVDD} = 5V; V_{IN} = 1V_{P-P}, measured at VOUT; f = 5MHz; power-supply ripple = 0.2V_{P-P}		30		dB
Short-Circuit Current		VOUT to PGND			230	mA
Line-Time Distortion	LTD	Figures 1a, 1b			0.5	%
Output Impedance	Z_{OUT}	Figures 1a, 1b		0.2		Ω
Gain		Figures 1a, 1b	1.89	2.0	2.11	V/V
Black Level		At VOUT, Figures 1a, 1b			AGND + 1.5	V
Input-Voltage Operating Range	V_{IN}	Figures 1a, 3 (Note 2)	0.5		1.2	V_{P-P}
Input-Voltage Sync Detection Range	V_{INSD}	Figures 1a, 3 (Note 3)	0.5		2.0	V_{P-P}
Maximum Output-Voltage Swing	V_{OUT}	Figures 1a, 1b	2.4			V_{P-P}
Output-Voltage Sync Tip Level				0.7		V
Large Signal Bandwidth (0.2dB)	BW	V_{OUT} = 2V_{P-P}, Figures 1a, 1b		6		MHz
VIN to VOUT Delay				30		ns
Differential Gain	DG			0.5		%
Differential Phase	DP			0.5		Degrees
OSD White Level		VOUT 100% white level with respect to black level	1.25	1.33	1.45	V
Horizontal Pixel Jitter		Between consecutive horizontal lines		24		ns
Video Clamp Settling Time				32		Lines

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +4.75V to +5.25V, V_{PVDD} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{AVDD} = V_{DVDD} = V_{PVDD} = +5V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSD CHARACTERISTICS						
OSD Rise Time		OSD insertion mux register OSDM[5,4,3] = 011b		60		ns
OSD Fall Time		OSD insertion mux register OSDM[5,4,3] = 011b		60		ns
OSD Insertion Mux Switch Time		OSD insertion mux register OSDM[2,1,0] = 011b		75		ns

TIMING CHARACTERISTICS

(V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +4.75V to +5.25V, V_{PVDD} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{AVDD} = V_{DVDD} = V_{PVDD} = +5V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING						
SCLK Period	t_{CP}		100			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS0}		30			ns
$\overline{CS}$ Fall After SCLK Rise Hold	t_{CSH0}		0			ns
$\overline{CS}$ Rise to SCLK Setup	t_{CSS1}		30			ns
$\overline{CS}$ Rise After SCLK Hold	t_{CSH1}		0			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		100			ns
SDIN to SCLK Setup	t_{DS}		30			ns
SDIN to SCLK Hold	t_{DH}		0			ns
SDOUT Valid Before SCLK	t_{DO1}	20pF to ground	25			ns
SDOUT Valid After SCLK	t_{DO2}	20pF to ground	0			ns
$\overline{CS}$ High to SDOUT High Impedance	t_{DO3}	20pF to ground	300			ns
$\overline{CS}$ Low to SDOUT Logic Level	t_{DO4}	20pF to ground	20			ns
$\overline{HSYNC}$, $\overline{VSYNC}$, AND LOS TIMING						
LOS, $\overline{VSYNC}$, and $\overline{HSYNC}$ Valid before CLKOUT Rising Edge	t_{DOV}	20pF to ground		30		ns
VOUT Sync to $\overline{VSYNC}$ Falling Edge Delay	$t_{VOUT-VSF}$	NTSC external sync mode, Figure 4		375		ns
		PAL external sync mode, Figure 6		400		

TIMING CHARACTERISTICS (continued)

(V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +4.75V to +5.25V, V_{PVDD} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{AVDD} = V_{DVDD} = V_{PVDD} = +5V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOUT Sync to $\overline{VSYNC}$ Rising Edge Delay	$t_{VOUT-VSR}$	NTSC external sync mode, Figure 4		400		ns
		PAL external sync mode, Figure 6		425		
$\overline{VSYNC}$ Falling Edge to VOUT Sync Delay	$t_{VSF-VOUT}$	NTSC internal sync mode, Figure 5		40		ns
		PAL internal sync mode, Figure 7		45		
$\overline{VSYNC}$ Rising Edge to VOUT Sync Delay	$t_{VSR-VOUT}$	NTSC internal sync mode, Figure 5		32		ns
		PAL internal sync mode, Figure 7		30		
VOUT Sync to $\overline{HSYNC}$ Falling Edge Delay	$t_{VOUT-HSF}$	NTSC and PAL external sync mode, Figure 8		310		ns
VOUT Sync to $\overline{HSYNC}$ Rising Edge Delay	$t_{VOUT-HSR}$	NTSC and PAL external sync mode, Figure 8		325		ns
$\overline{HSYNC}$ Falling Edge to VOUT Sync Delay	$t_{HSF-VOUT}$	NTSC and PAL internal sync mode, Figure 9		115		ns
$\overline{HSYNC}$ Rising Edge to VOUT Sync Delay	$t_{HSR-VOUT}$	NTSC and PAL internal sync mode, Figure 9		115		ns
All Supplies High to $\overline{CS}$ Low	t_{PUD}	Power-up delay		50		ms
NVM Write Busy	t_{NVW}			12		ms

Note 1: See the standard test circuits of Figure 1. R_L = 75Ω, unless otherwise specified. All digital input signals are timed from a voltage level of (V_{IH} + V_{IL}) / 2. All parameters are tested at T_A = +85°C and values through temperature range are guaranteed by design.

Note 2: The input-voltage operating range is the input range over which the output signal parameters are guaranteed (Figure 3).

Note 3: The input-voltage sync detection range is the input composite video range over which an input sync signal is properly detected and the OSD signal appears at VOUT. However, the output voltage specifications are not guaranteed for input signals exceeding the maximum specified in the input operating voltage range (Figure 3).

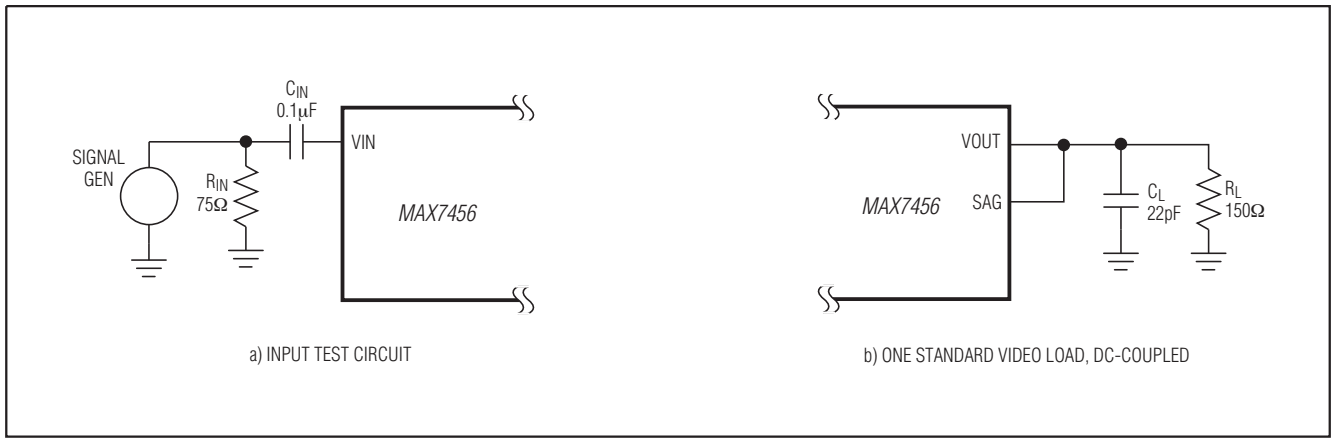


图1. 标准测试电路

典型工作特性

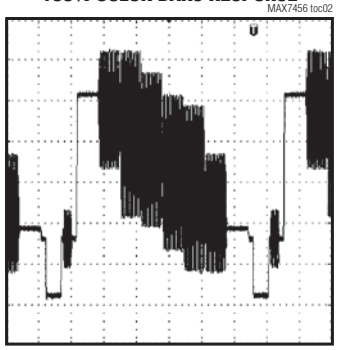
(V_{AVDD} = +5V, V_{DVDD} = +5V, V_{PVDD} = +5V, T_A = +25°C, unless otherwise noted. See the *Typical Operating Circuit* of Figure 2, if applicable.)

IMAGE WITH ON-SCREEN GRAPHICS

MAX7456 toc01

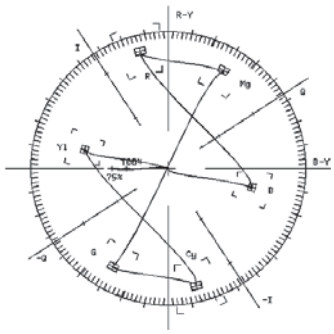
100% COLOR BARS RESPONSE

MAX7456 toc02



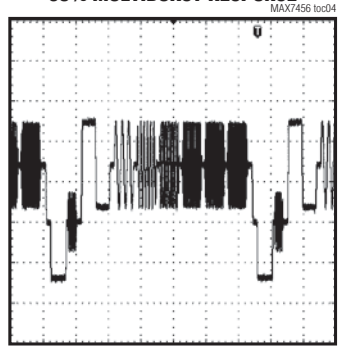
75% COLOR BARS VECTOR DIAGRAM

MAX7456 toc03



60% MULTIBURST RESPONSE

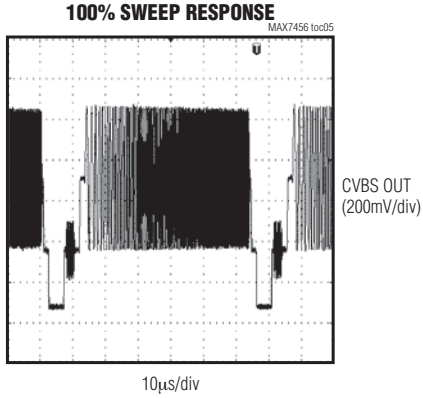
MAX7456 toc04



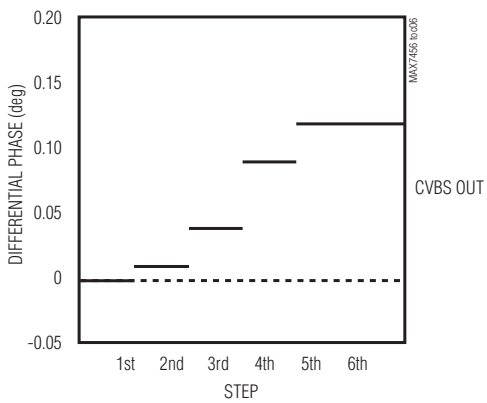
典型工作特性(续)

(V_{AVDD} = +5V, V_{DVDD} = +5V, V_{PVDD} = +5V, T_A = +25°C, unless otherwise noted. See the *Typical Operating Circuit* of Figure 2, if applicable.)

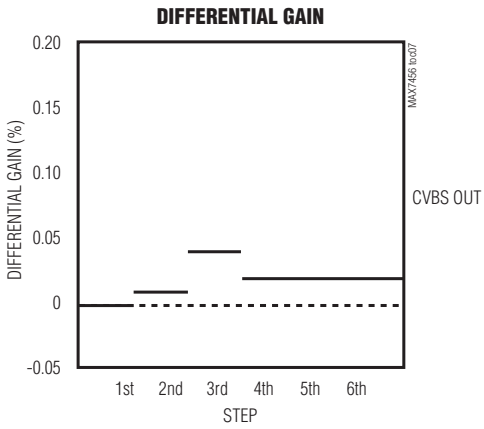
100% SWEEP RESPONSE



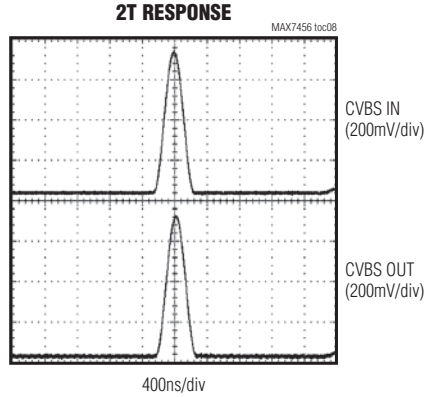
DIFFERENTIAL PHASE



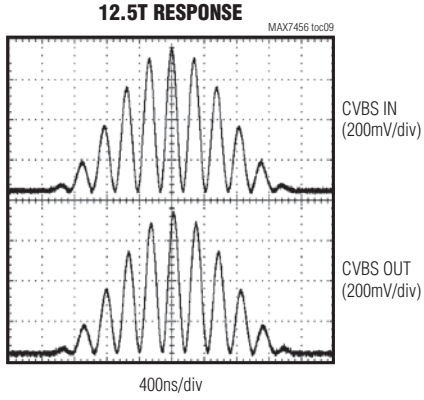
DIFFERENTIAL GAIN



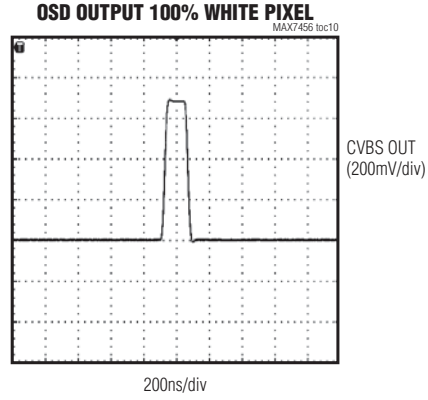
2T RESPONSE



12.5T RESPONSE



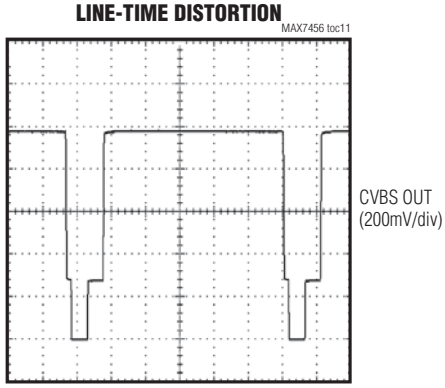
OSD OUTPUT 100% WHITE PIXEL



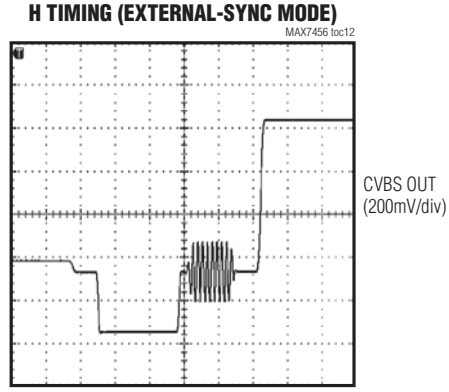
典型工作特性(续)

(V_{AVDD} = +5V, V_{DVDD} = +5V, V_{PVDD} = +5V, T_A = +25°C, unless otherwise noted. See the *Typical Operating Circuit* of Figure 2, if applicable.)

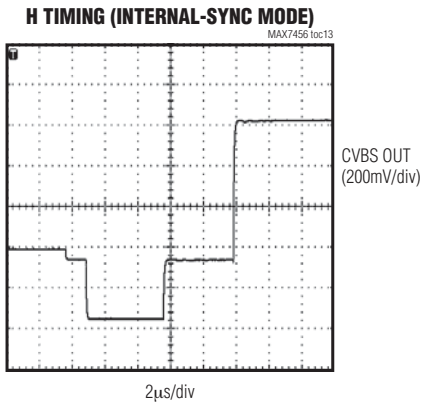
LINE-TIME DISTORTION



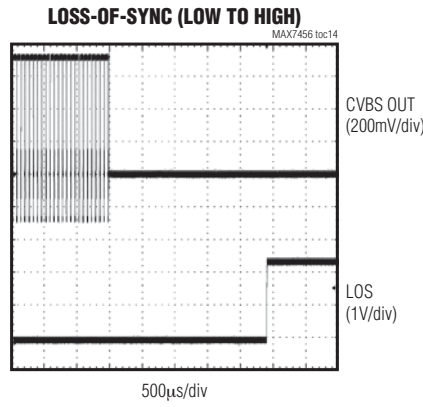
H TIMING (EXTERNAL-SYNC MODE)



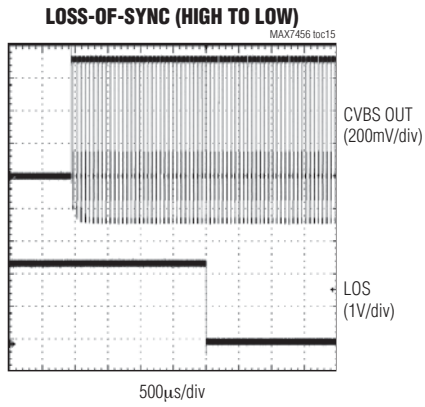
H TIMING (INTERNAL-SYNC MODE)



LOSS-OF-SYNC (LOW TO HIGH)



LOSS-OF-SYNC (HIGH TO LOW)



引脚说明

引脚	名称	功能
1, 2, 13–16, 27, 28	N.C.	不连接。内部未连接。
3	DVDD	数字电源输入，用一个0.1µF电容旁路至DGND。
4	DGND	数字地。
5	CLKIN	晶体连接1。在CLKIN和XFB之间连接一个并联谐振、基频模式晶体构成晶体振荡器，或使用27MHz系统参考时钟直接驱动CLKIN。
6	XFB	晶体连接2。在CLKIN和XFB之间连接一个并联谐振、基频模式晶体构成晶体振荡器，如果使用27MHz系统参考时钟驱动CLKIN，将XFB悬空。
7	CLKOUT	时钟输出。27MHz逻辑电平输出的系统时钟。
8	$\overline{CS}$	低电平有效片选输入。当$\overline{CS}$为高电平时，SDOUT变为高阻抗。
9	SDIN	串行数据输入。数据在SCLK上升沿移入。
10	SCLK	串行时钟输入。为数据输入到SDIN和从SDOUT输出提供时钟，占空比必须在40%至60%之间。
11	SDOUT	串行数据输出。数据在SCLK下降沿输出。当$\overline{CS}$为高电平时，变为高阻抗。
12	LOS	同步丢失输出(开漏)。当VIN同步脉冲丢失32个连续周期时，LOS变为高电平。当接收到32个连续有效同步脉冲时，LOS变为低电平。通过1kΩ上拉电阻连接至DVDD或另一个符合接收器件的电源正极。
17	$\overline{VSYNC}$	场同步输出(开漏)。视频输入场同步期间，$\overline{VSYNC}$变为低电平。$\overline{VSYNC}$可以从VIN恢复，也可以在内同步模式下内部产生。通过1kΩ上拉电阻连接至DVDD或者另一个符合接收器件的电源正极。
18	$\overline{HSYNC}$	行同步输出(开漏)。视频输入行同步期间，$\overline{HSYNC}$变为低电平。$\overline{HSYNC}$可以从VIN恢复，也可以在内同步模式下内部产生。通过1kΩ上拉电阻连接至DVDD或另一个符合接收器件的电源正极。
19	$\overline{RESET}$	系统复位输入。最小$\overline{RESET}$脉冲宽度为50ms。$\overline{RESET}$上升沿100µs后，所有SPI寄存器被复位至默认值。在此期间，不能对寄存器进行读写访问。$\overline{RESET}$上升沿20µs后，显示存储器所有位置都被复位至默认值00H。
20	AGND	模拟地。
21	AVDD	模拟电源输入，用一个0.1µF电容旁路至AGND。
22	VIN	PAL或者NTSC CVBS视频输入。
23	PGND	驱动器地，在一个点连接至AGND。
24	PVDD	驱动器电源输入，用一个0.1µF电容旁路至PGND。
25	SAG	电压衰减修正输入，如果不使用须连接至VOUT，参考图1b。
26	VOUT	视频输出。
—	EP	裸焊盘。内部连接至AGND。将EP连接至AGND层以提高散热性能。不要将EP用作唯一的地连接。

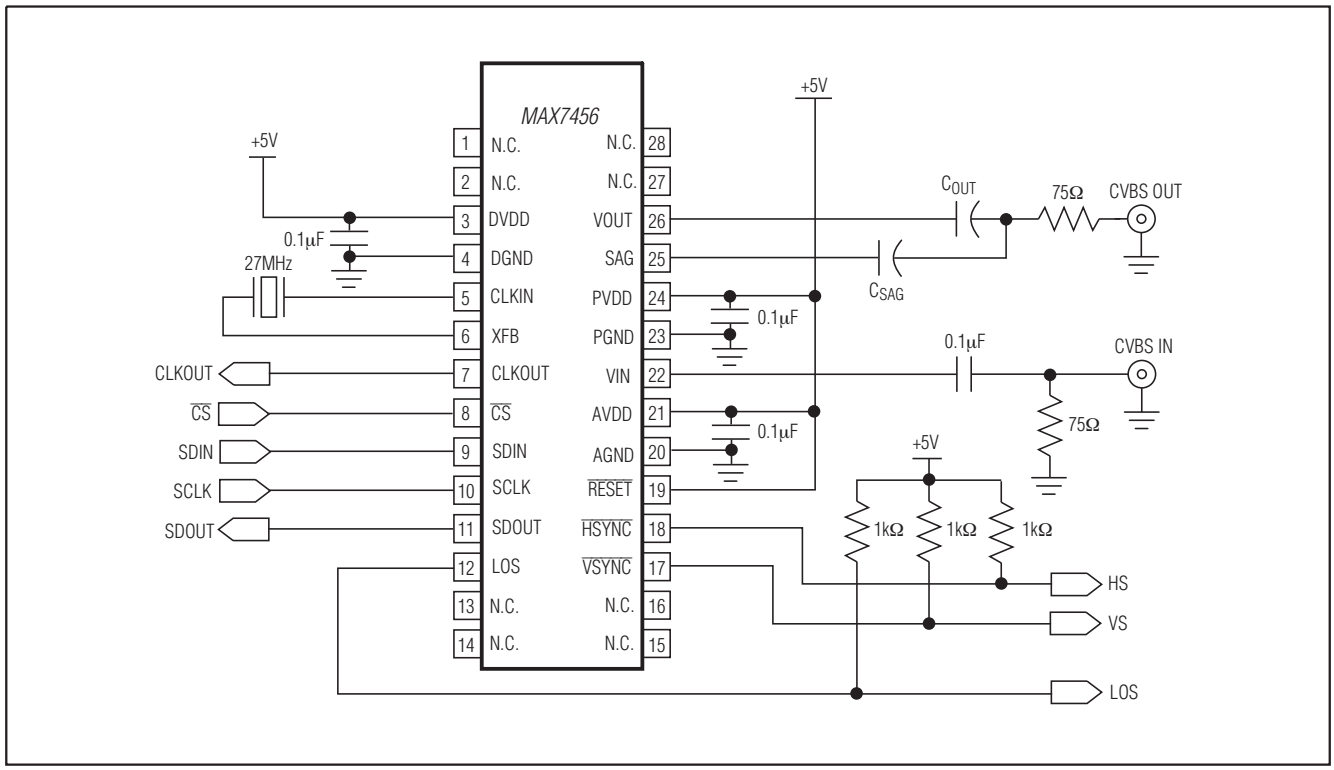


图2. 典型工作电路

详细说明

MAX7456单通道单色随屏显示(OSD)发生器集成了产生用户定义的OSD并加载到输出信号所需的全部功能。MAX7456能够接收NTSC或者PAL复合视频信号。器件包括输入钳位、同步分离器、视频时序发生器、OSD插入复用器、非易失字符存储器、显示存储器、OSD发生器、晶体振荡器以及读/写OSD数据的SPI兼容接口和视频驱动器等(请参考*简化功能框图*)。此外，MAX7456还为系统同步提供场同步($\overline{VSYNC}$)、行同步($\overline{HSYNC}$)和同步丢失(LOS)输出信号。时钟输出信号(CLKOUT)支持多个器件的菊型链接。

请参考*MAX7456寄存器说明*部分，了解本数据资料中使用的寄存器符号。

256个用户定义12 x 18象素字符组具有预装入，并与输入视频流复合，产生带有OSD视频输出的CVBS信号。在NVM中，最多可以重设256个12 x 18象素字符。在NTSC制式中，显示13行 x 30个字符。在PAL制式中，显示16行 x 30个字符。没有输入视频信号时，使用MAX7456的内部视频时序发生器，仍然可以显示OSD图像。

视频输入

MAX7456的VIN可接收标准NTSC或者PAL CVBS信号。必须用一个0.1µF电容对视频信号输入进行交流耦合，并在内部钳位。需要0.1µF输入耦合电容确保规定的线时间失真(LTD)和视频钳位稳定时间。视频钳位稳定时间随输入耦合电容同比例变化，而LTD随电容反比例变化。

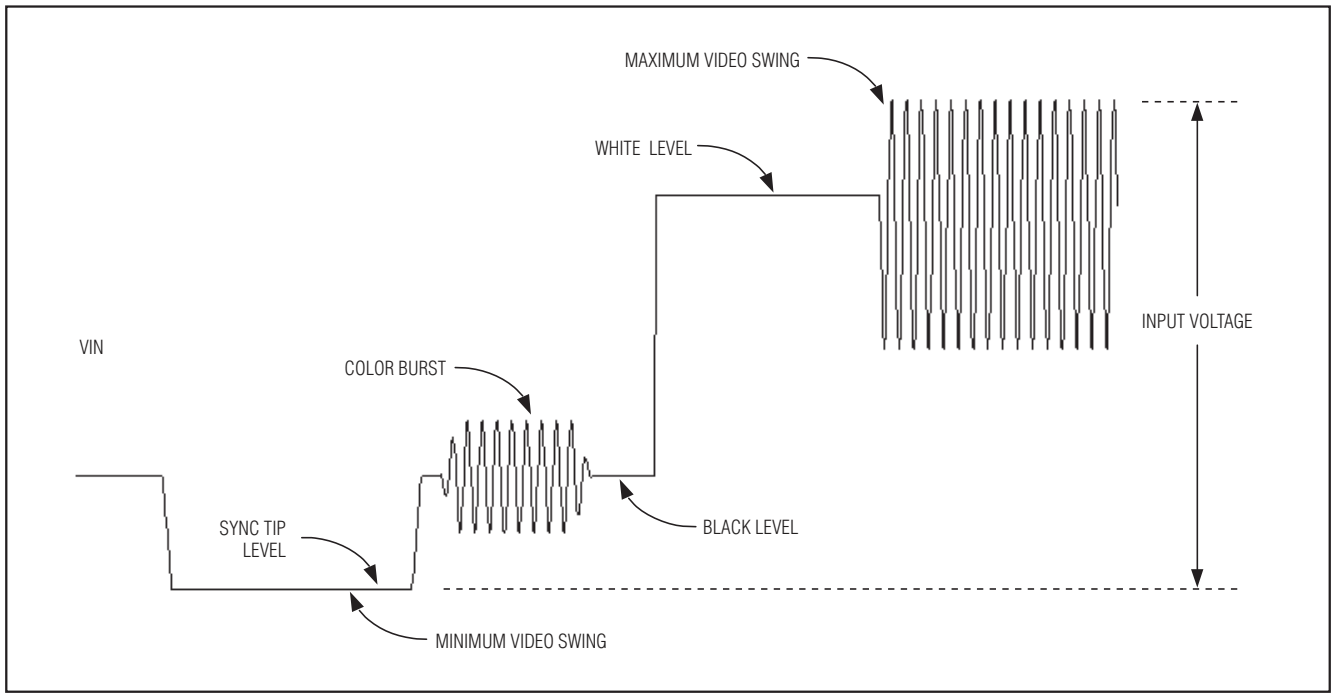


图3. 术语定义

输入钳位

MAX7456的钳位是直流重建电路，在逐行基础上，使用输入耦合电容校正输入信号的直流偏移，将VIN的同步头钳位在约550mV。在VIN端建立的直流电平可用于片内同步检测和视频处理功能。该电路还消除了低频噪声，例如60Hz杂音或其它加入的低频噪声。

同步分离器

同步分离器检测视频输入的复合同步脉冲，提取出时序信息，产生$\overline{\text{HSYNC}}$和$\overline{\text{VSYNC}}$信号；还用于内部OSD同步和同步丢失(LOS)检测。如果在VIN上32条连续行周期没有探测到同步信号，LOS变为高电平，如果探测到32个连续行同步信号，则变为低电平。在LOS状态期间，当VM0[5] = 0 (视频模式0寄存器，第5位)时，只有OSD出现在VOUT上。此时，输入图像在VOUT被设置为由VM1[6:4]确定的灰度级。表1列出了所有同步模式。

表1. 视频同步模式

VIDEO MODE	VIN	$\overline{\text{VSYNC}}$	$\overline{\text{HSYNC}}$	LOS	VOUT
Auto Sync Select Mode VM0[5, 4] = 0x	Video	Active	Active	Low	V_{IN} + OSD
	No input	Active	Active	High	OSD only
External Sync Select VM0[5, 4] = 10	Video	Active	Active	Low	V_{IN} + OSD
	No input	Inactive (high)	Inactive (high)	High	DC
Internal Sync Select VM0[5, 4] = 11	Video	Active	Active	High	OSD only
	No input	Active	Active	High	OSD only

X = 无关。

视频时序发生器

视频时序发生器是数字电路，产生所有的内部和外部(VSYNC和HSYNC)时序信号。VSYNC和HSYNC可以和VIN同步，或在内部同步模式下独立于输入运行。视频时序发生器能够使用同一个27MHz晶体产生NTSC或者PAL时序(请参考图4至图9)。

晶体振荡器

内部晶体振荡器产生视频时序发生器使用的系统时钟。振荡器使用一个27MHz晶体，也可以由CLKIN端外部27MHz TTL时钟驱动。外部时钟模式下，在CLKIN端连接一个27MHz TTL输入时钟，XFB端悬空。

显示存储器(SRAM)

显示存储器存储了480个字符地址，这些地址指向存储在NVM字符存储器中的字符。用户可以通过SPI兼容串口设置显示存储器的内容。显示存储器地址对应于监视器的固定位置(参考图10)。在场消隐期间写入显示存储器，可防止OSD图像的瞬时变暗。可将VSYNC作为主机处理器中断，启动写入显示存储器操作，以实现上述功能。

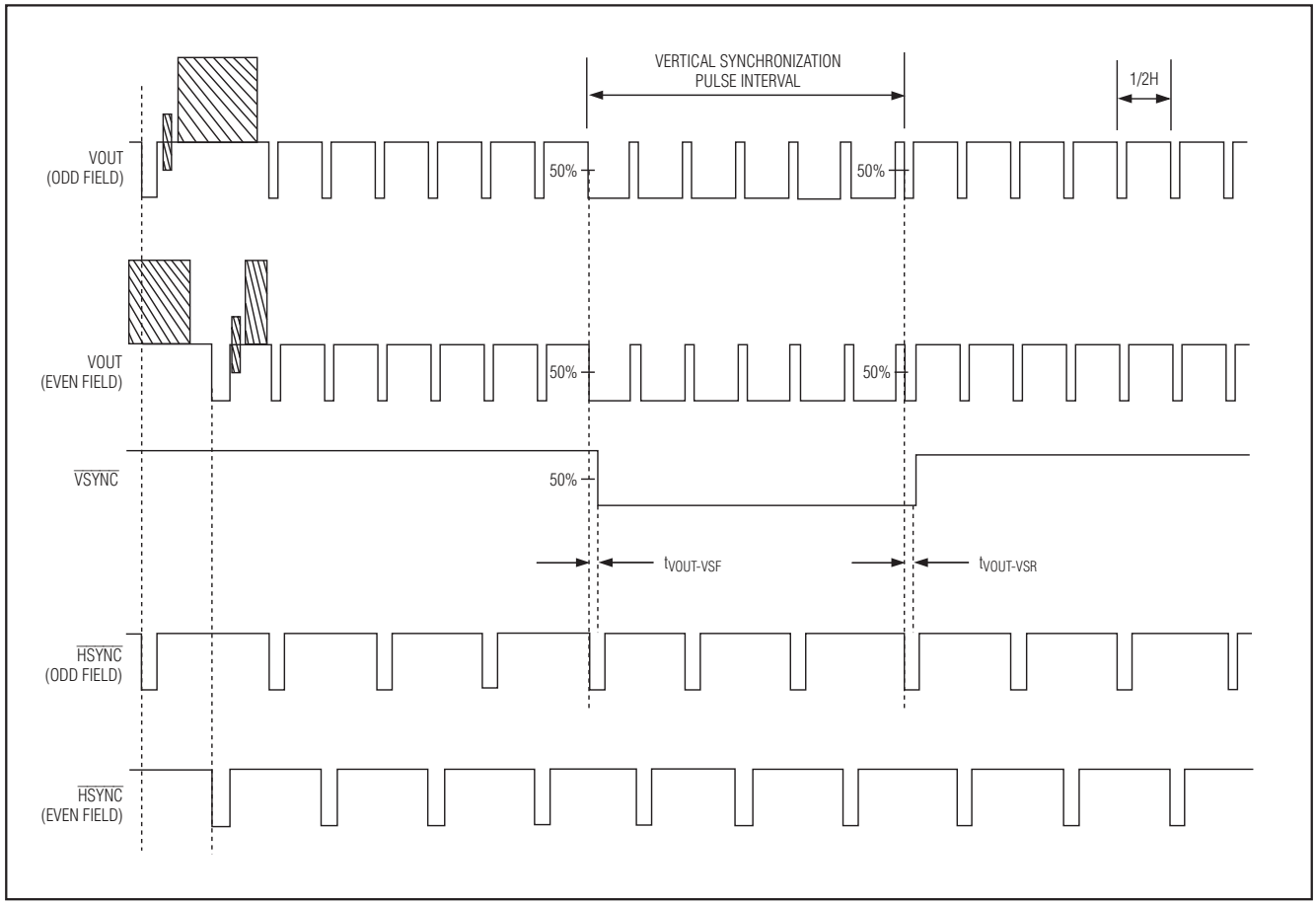


图4. VOUT、VSYNC和HSYNC时序(NTSC，外同步模式)

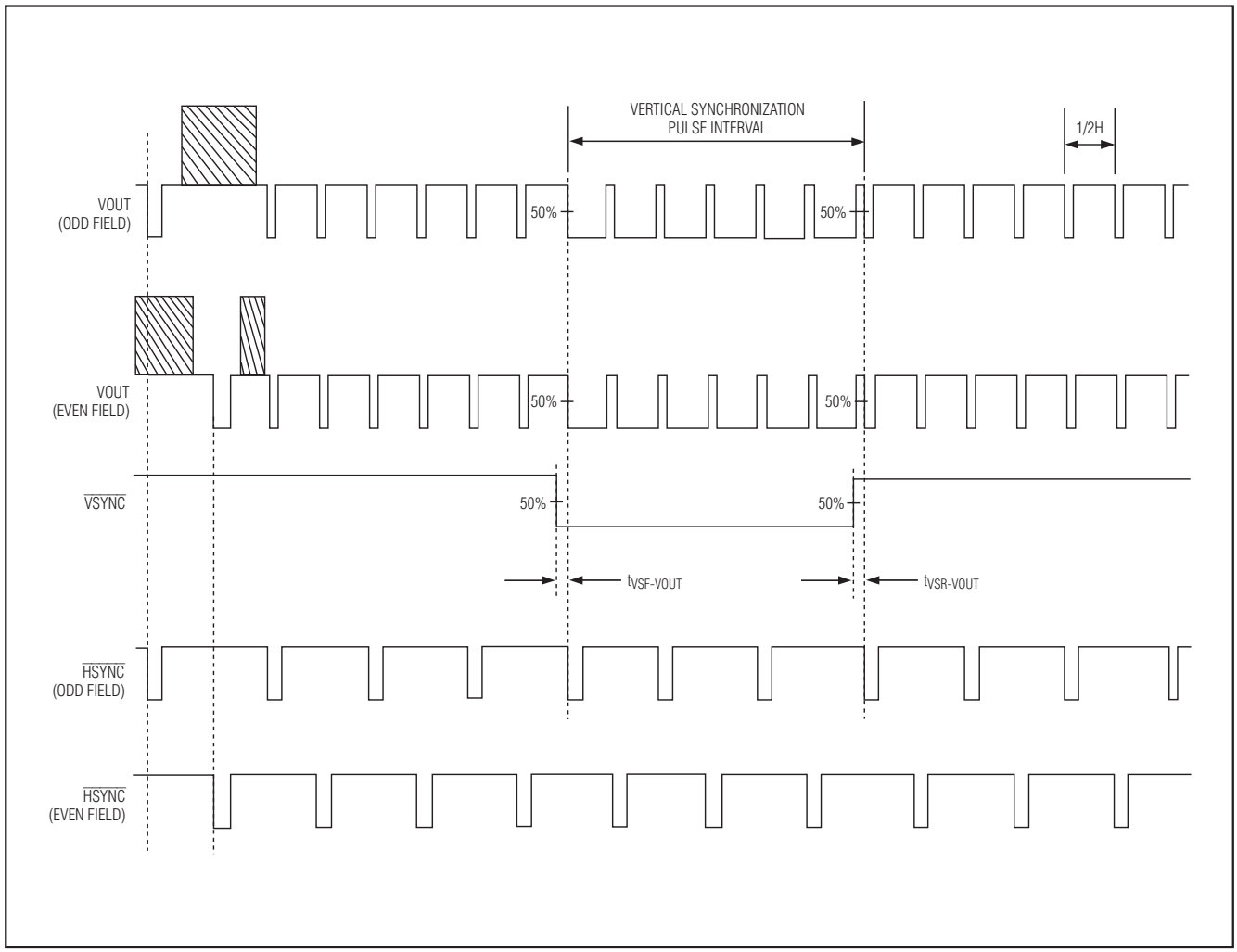


图5. VOUT、VSYNC和HSYNC时序(NTSC，内同步模式)

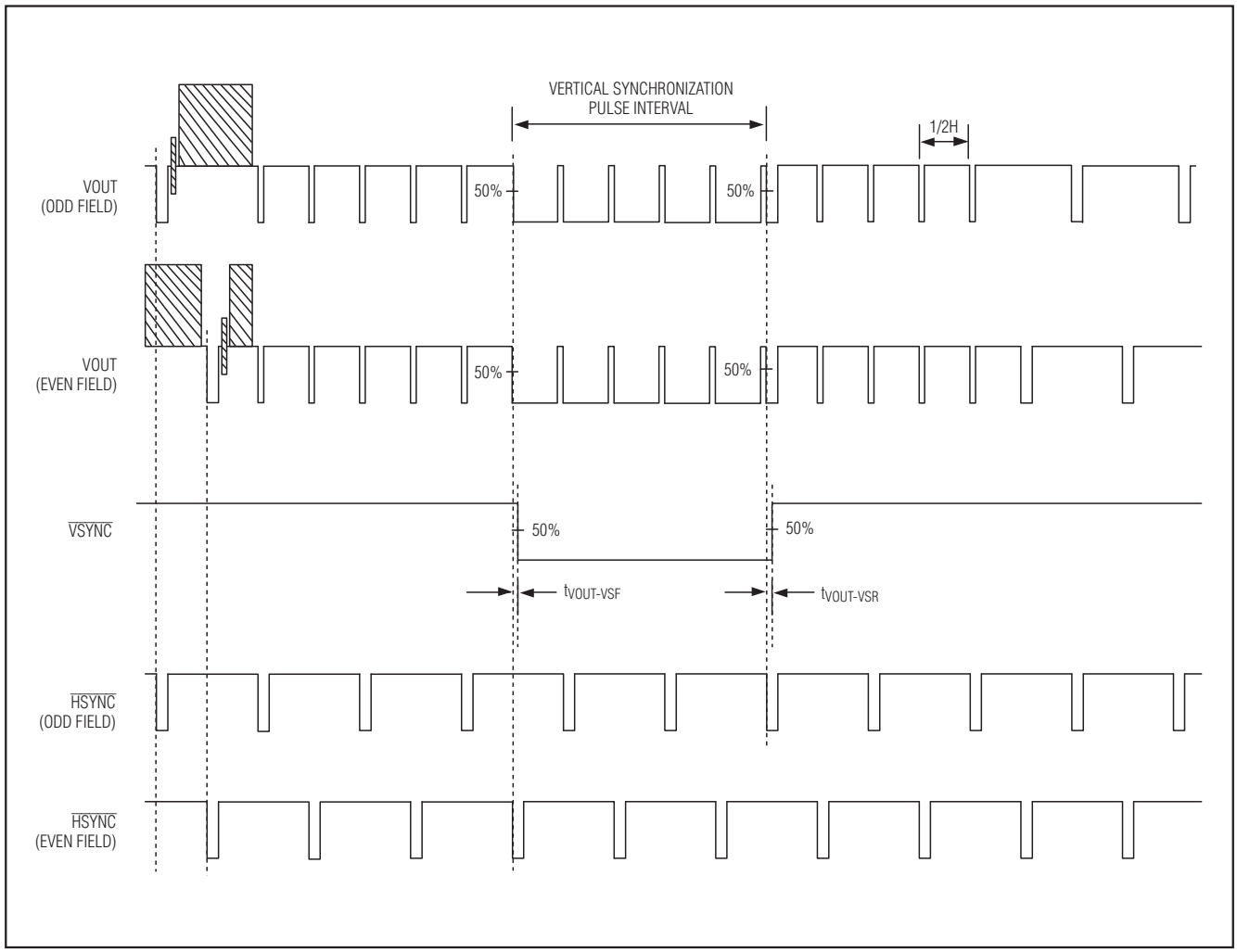


图6. VOUT、VSYNC和HSYNC时序(PAL，外同步模式)

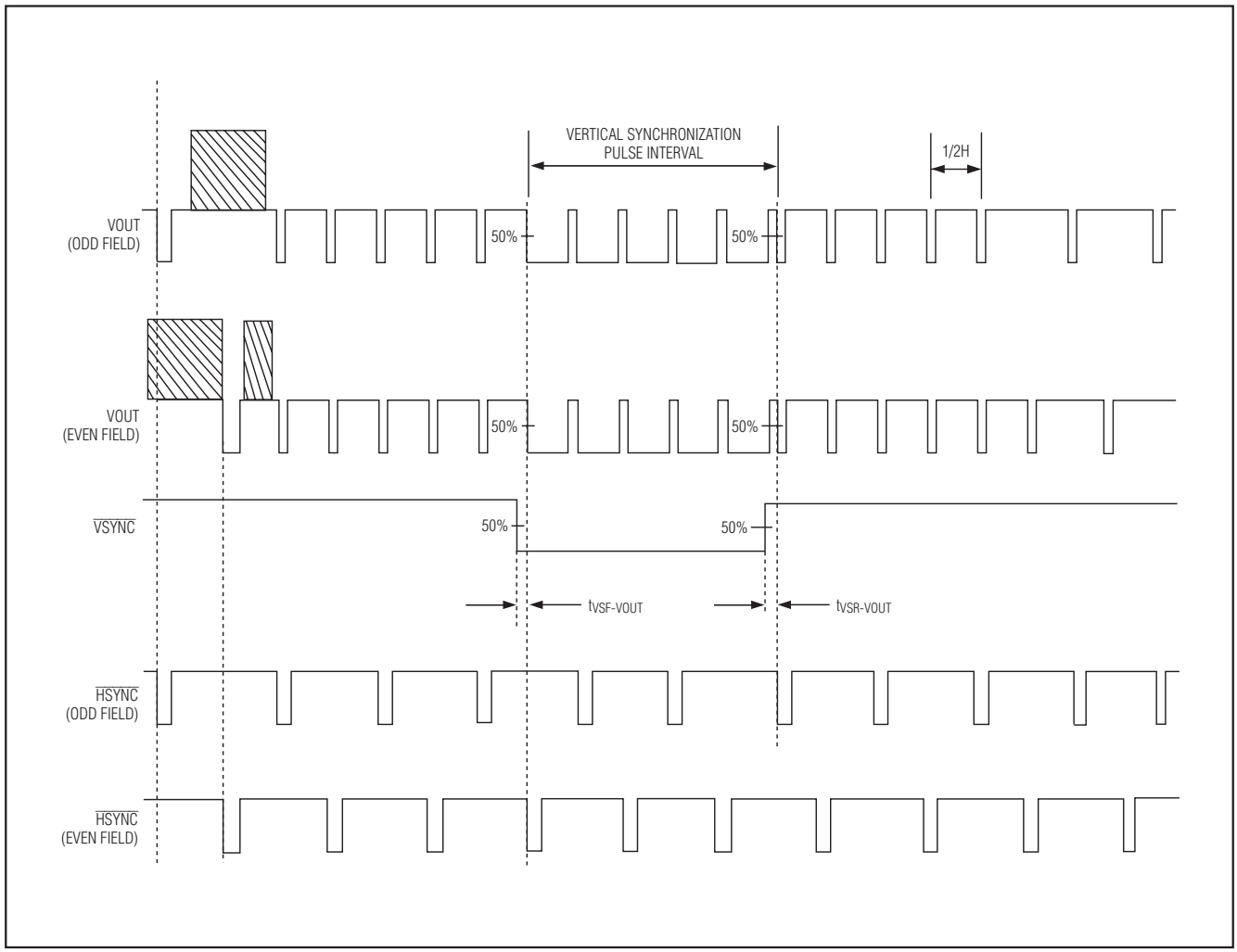


图7. VOUT、VSYNC和HSYNC时序(PAL，内同步模式)

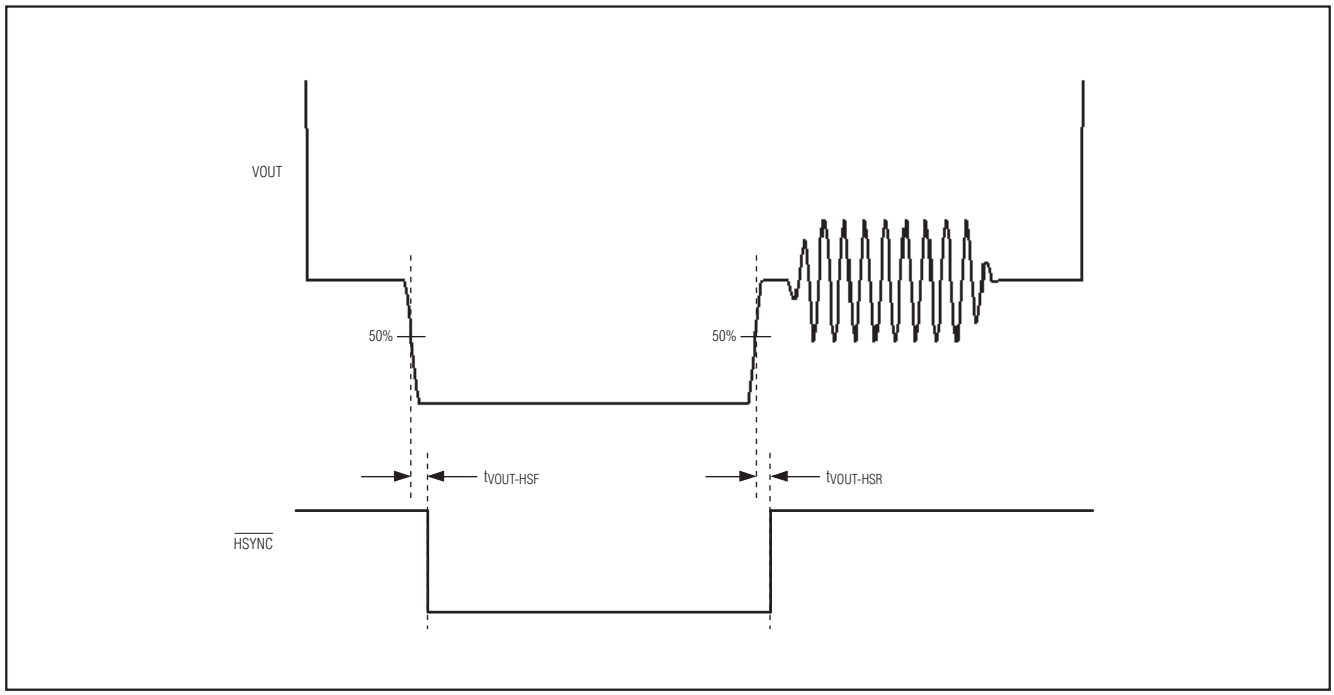


图8. VOUT和HSYNC行同步时序(NTSC和PAL，外同步模式)

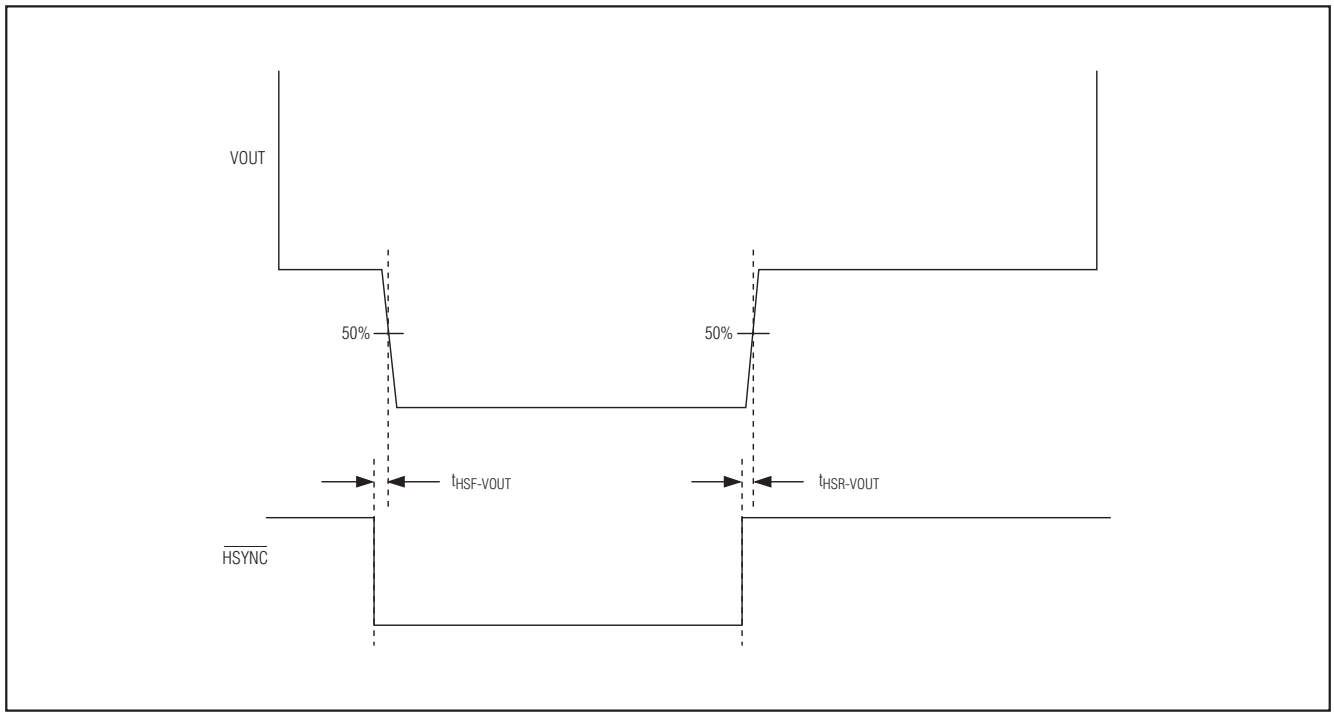


图9. VOUT和HSYNC行同步时序(NTSC和PAL，内同步模式)

字符存储器(NVM)

字符存储器是256行 x 64字节宽非易失存储器(NVM)，存储字符或者图形，在工厂中预装入了图12所示的字符。用户可通过SPI兼容串口设置字符存储器中的内容。每一行都包含一个OSD字符的描述。每一字符由12个行 x 18列象素组成，每个象素点由具有三种状态的2位数据表示，三种状态为：白色、黑色或者透明。因此，每个字符需要54字节的象素数据(图11)。

NVM需要一次读写所有字符(64字节)，通过被称为镜像RAM的存储器行实现。64字节临时镜像RAM包含有所选字符(CMAH[7:0])的所有象素数据，用作NVM读写操作的缓冲(图13)。总是通过镜像RAM访问NVM，所以需要两个操作步骤。向NVM写入字符时，用户首先利用54个8位SPI写操作写入镜像RAM，然后执行一条镜像RAM写命令。类似的，读取一个字符的象素时，先将字符的象素数据读入镜像RAM，再从镜像RAM将所需的象素数据读至SPI端口。

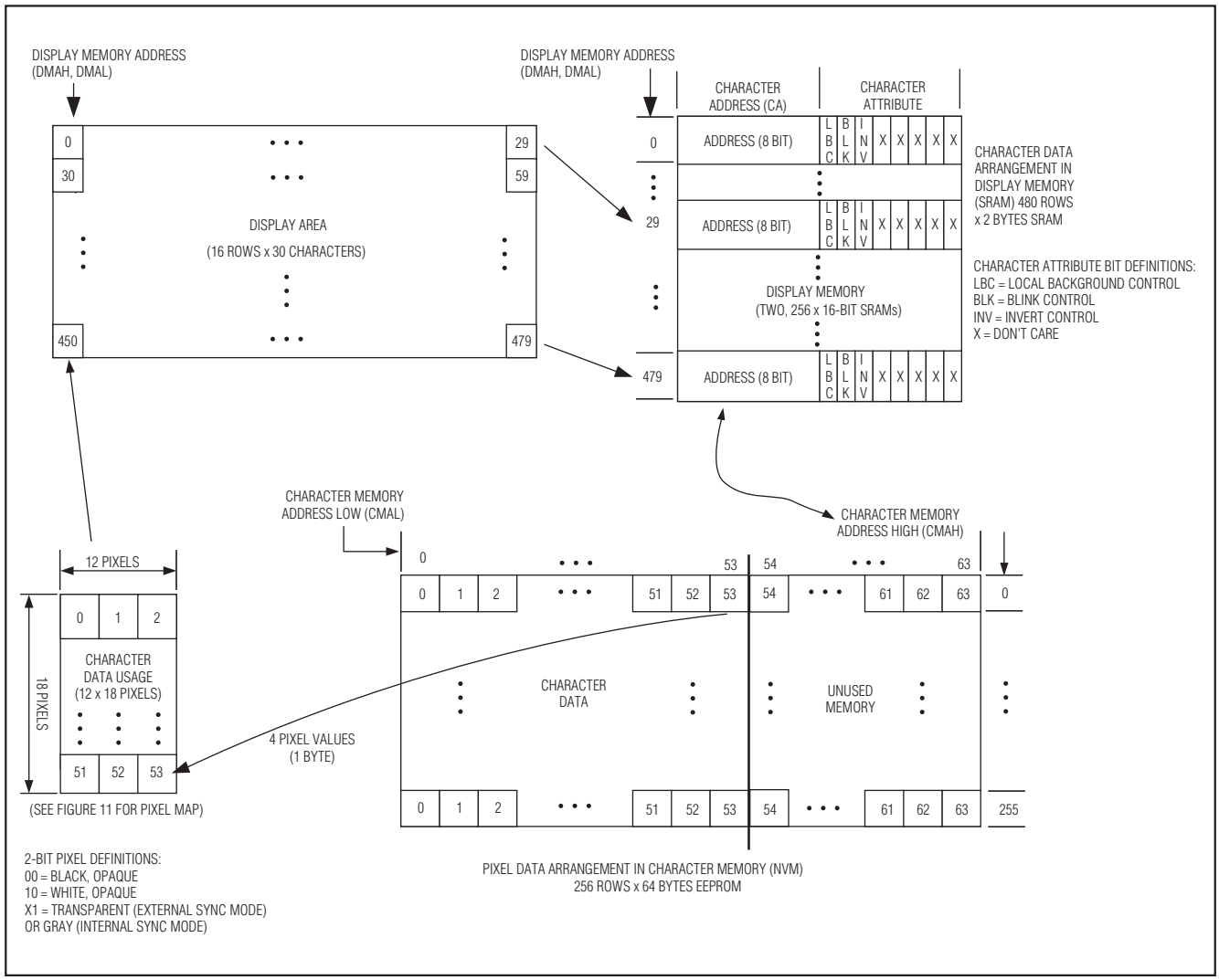


图10. 各种参数定义

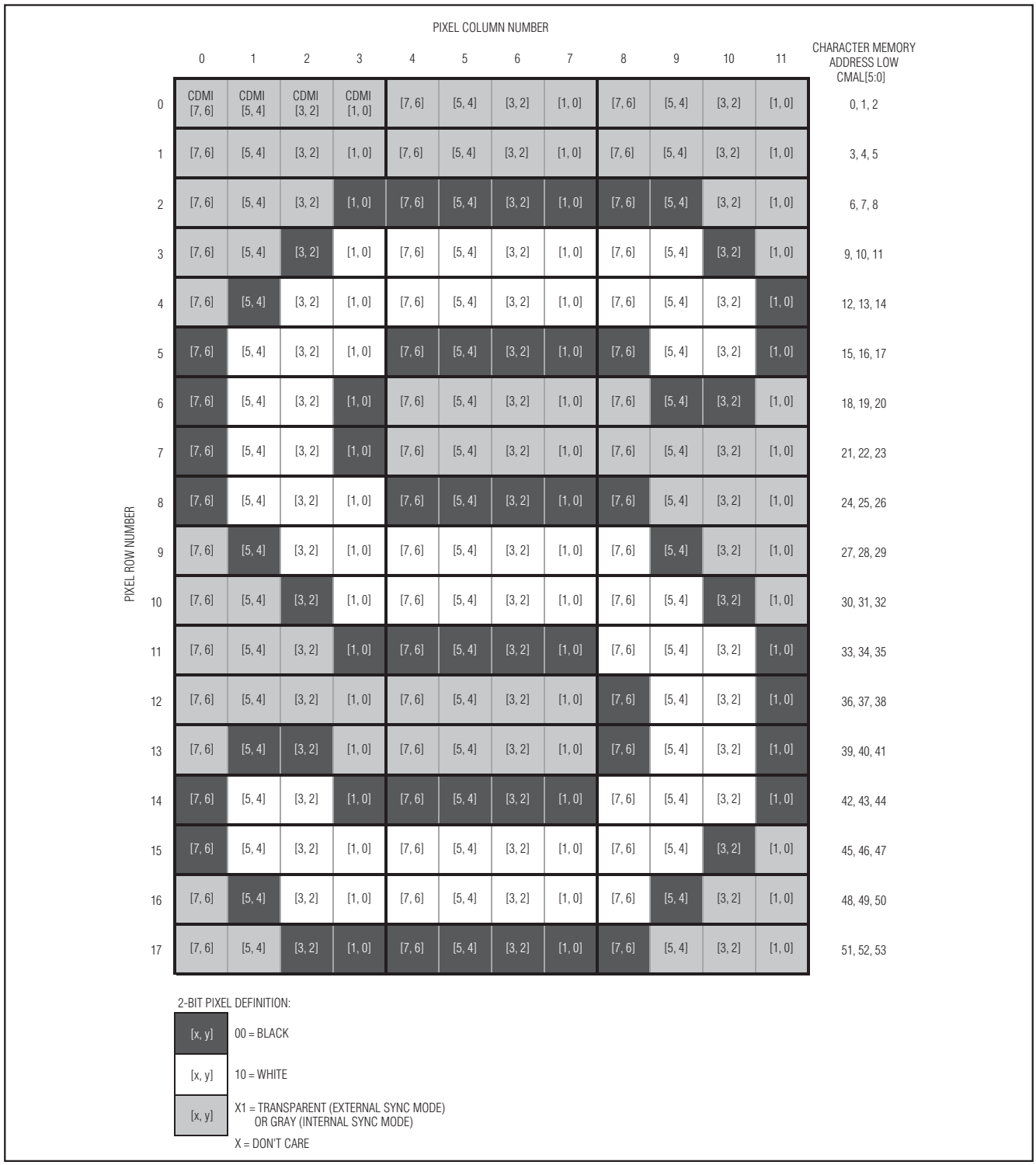


图11. 字符数据使用(象素映射)

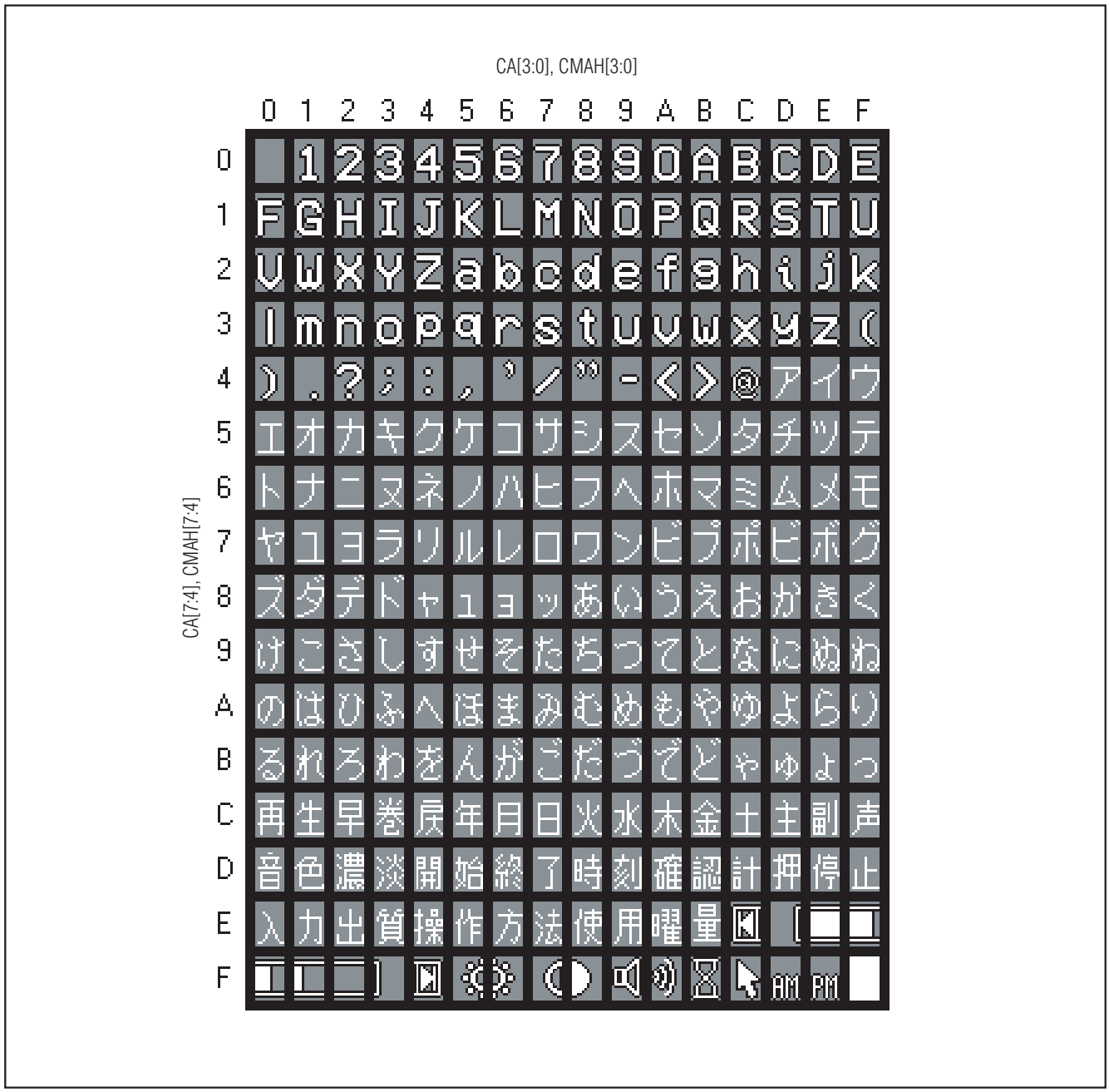


图12. 字符地址映射(默认字符集)

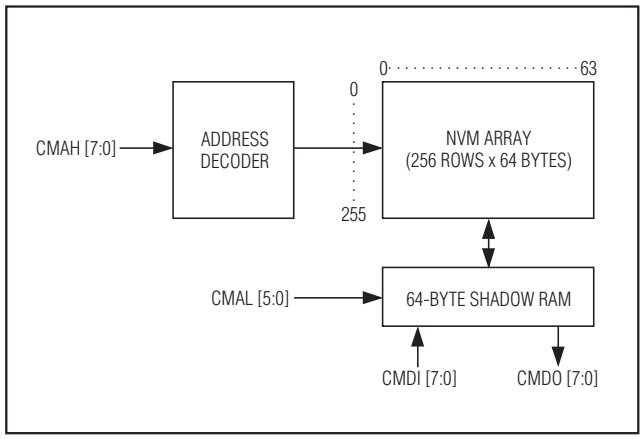


图13. NVM结构

随屏显示(OSD)发生器

OSD发生器根据字符存储器和行亮度寄存器(RB0–RB15)的内容，设置每一象素的亮度。

OSD插入复用器

OSD插入复用器在OSD象素和输入视频信号之间进行选择。OSD图像锐度由OSD插入复用器(OSDM)寄存器中的OSD上升和下降时间位以及OSD插入复用器开关时间位控制。该寄存器控制OSD图像锐度和色彩串扰/亮度串扰之间的均衡。减小时间设置可锐化象素，但是有可能增强色彩串扰/亮度串扰。最优设置取决于实际应用的需求，因此，可由用户设置。

视频输出驱动器

MAX7456包含增益为2倍的视频输出驱动器。驱动器最大输出摆幅为2.4V_{P-P}，信号带宽高达6MHz (衰减小于等于0.2dB)。驱动器输出可驱动两个150Ω标准视频负载。

电压衰减修正

通过电压衰减修正能够降低输出耦合电容的电路要求和物理尺寸，并将线时失真降到可接受的水平。电压衰减修正对具有对150Ω背向匹配电阻的同轴电缆和输出耦合电容组成的高通滤波器进行低频补偿。该电路的截止点必须足够低至能通过场同步间隔(PAL小于25Hz，NTSC小于30Hz)，以避免场倾斜。传统上，截止点小于5Hz，耦合电容必须非常大，典型为大于330µF。MAX7456降低了该电容值，并用两个较小的电容(C_{OUT}和C_{SAG})替代，有效降低了耦合电容的成本和体积，同时获得了可接受的线时失真(表2)。如果不使用，将SAG连接至VOUT。

表2. SAG修正电容值

C_{OUT} (µF)	C_{SAG} (µF)	LINE-TIME DISTORTION (% typ)
470	—	0.2
100	—	0.4
100	22	0.3
47	47	0.3
22	22	0.4
10	10	0.6

串行接口

SPI兼容串口设置工作模式和OSD数据。读功能支持写校验和读取状态(STAT)、显示存储器数据输出(DMDO)和字符存储器数据输出(CMDO)寄存器。

读写操作

MAX7456支持高达10MHz的接口时钟(SCLK)。图15所示为数据写入，图16为从MAX7456读取数据。拉低$\overline{CS}$使能串口。在SCLK上升沿数据输入SDIN。当$\overline{CS}$变为高电平时，数据被锁存至输入寄存器。如果$\overline{CS}$在传输中间变为高电平，则本次操作失败(即，数据没有被写入到寄存器中)。$\overline{CS}$变为低电平后，器件等待第一个输入到SDIN中的字节，以确定所执行数据传输的类型。

SPI命令为16位长，高8位(MSB)代表寄存器地址，低8位(LSB)代表数据(图15和图16)。这种配置有两个例外情况：

1) 显示存储器访问所使用的自动递增写入模式是一个8位操作(图21)。当执行显示存储器自动递增写入操作时，8位地址是内部产生的，串口只需要8位数据。
2) 在16位工作模式时，从显示存储器读取字符数据是24位操作(8位地址以及16位数据)，参考图20。

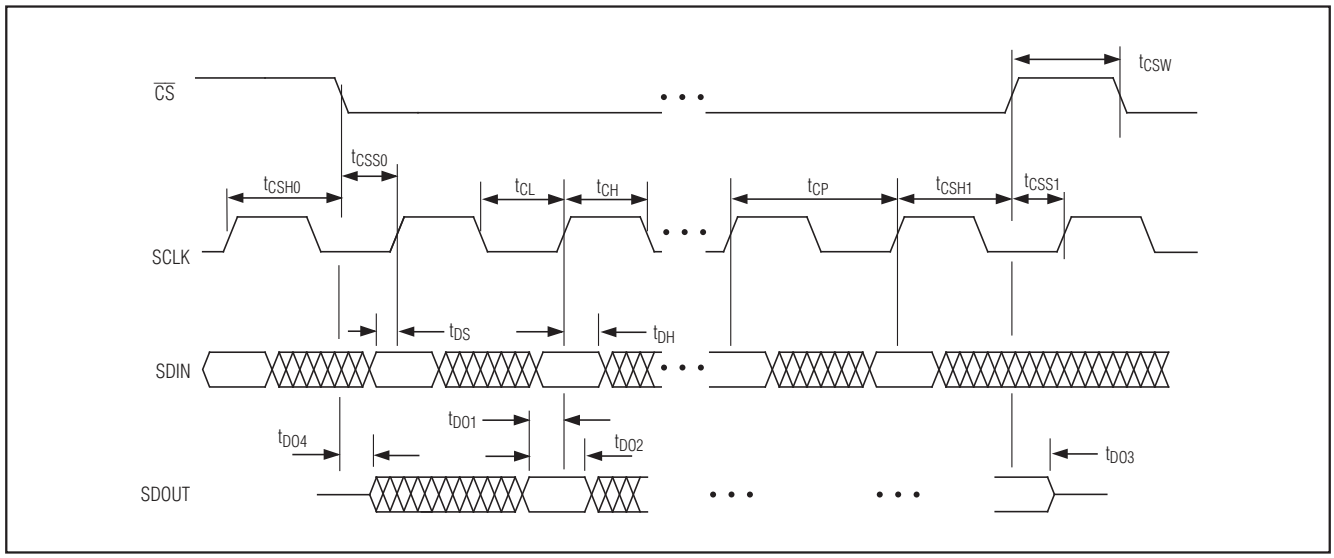


图14. 串口时序详述

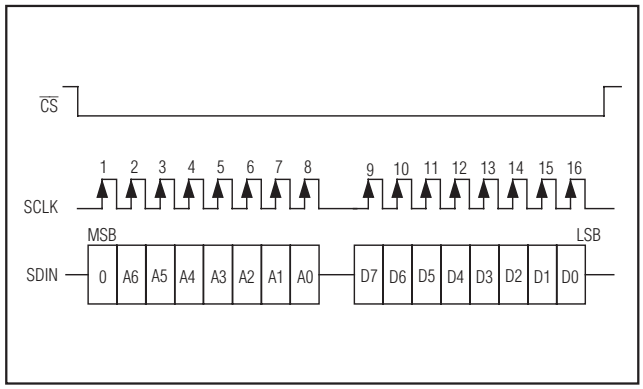


图15. 写操作

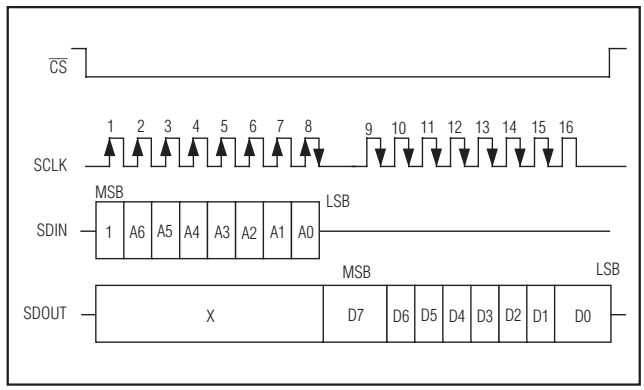


图16. 读操作

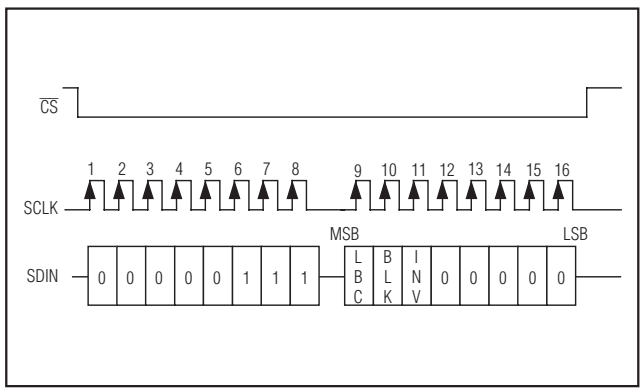


图17. 在8位工作模式下，写入字符属性字节

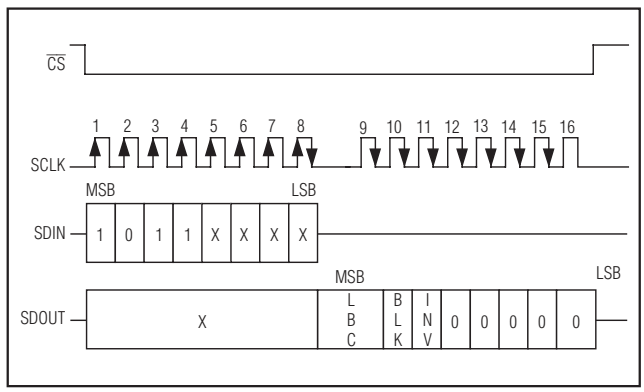


图18. 在8位工作模式下，读取字符属性字节

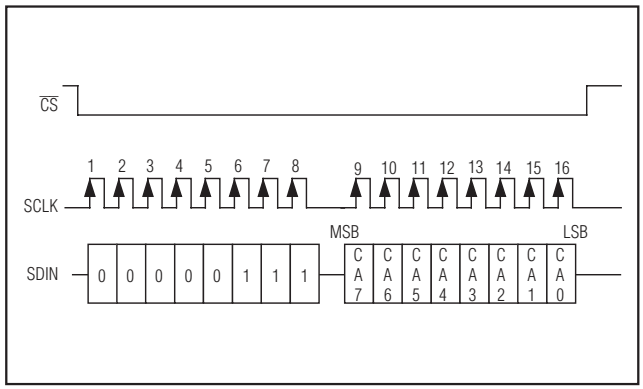


图19. 在8位和16位工作模式下，写入字符地址字节

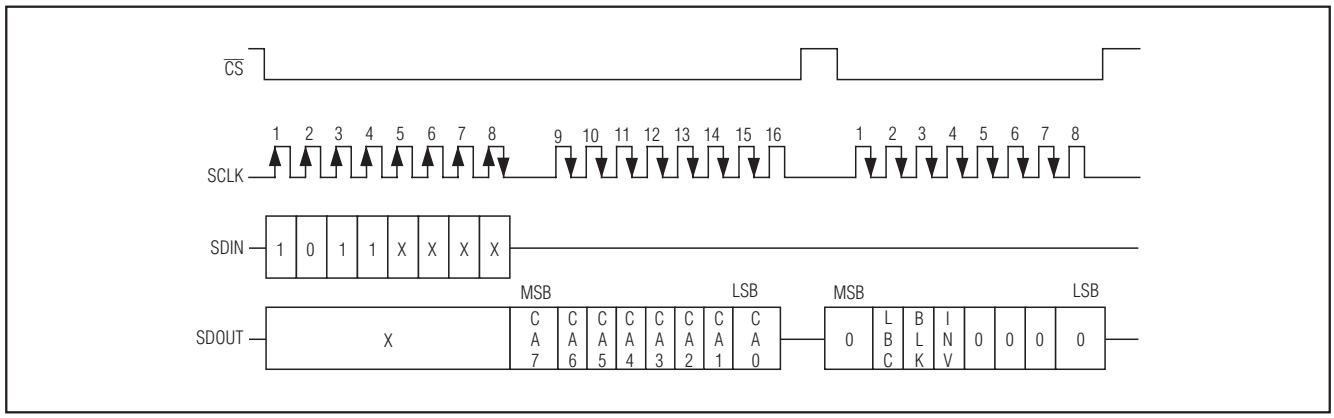


图20. 在16位工作模式下，读取字符地址和字符属性字节

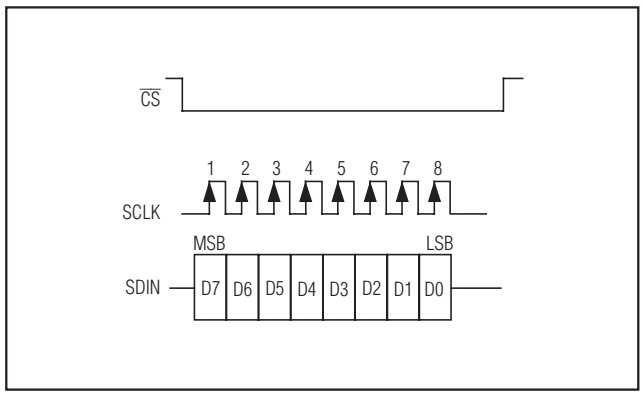


图21. 自动递增模式下的写操作

复位

上电复位

MAX7456的上电复位电路(POR)提供一个内部复位信号，在电源电压稳定后开始工作。内部复位信号将所有寄存器复位至默认值，清除显示存储器。寄存器复位过程需要100µs，为避免出现不期望的结果，在这期间不允许进行读/写操作。一般在供电电压稳定，并且27MHz时钟信号稳定50ms后，显示存储器复位，OSD使能。用户在这段时间中应避免SPI操作，以防止出现不期望的结果。50ms (典型值)后，可查询STAT[6]确认复位时序是否完成(图22)。

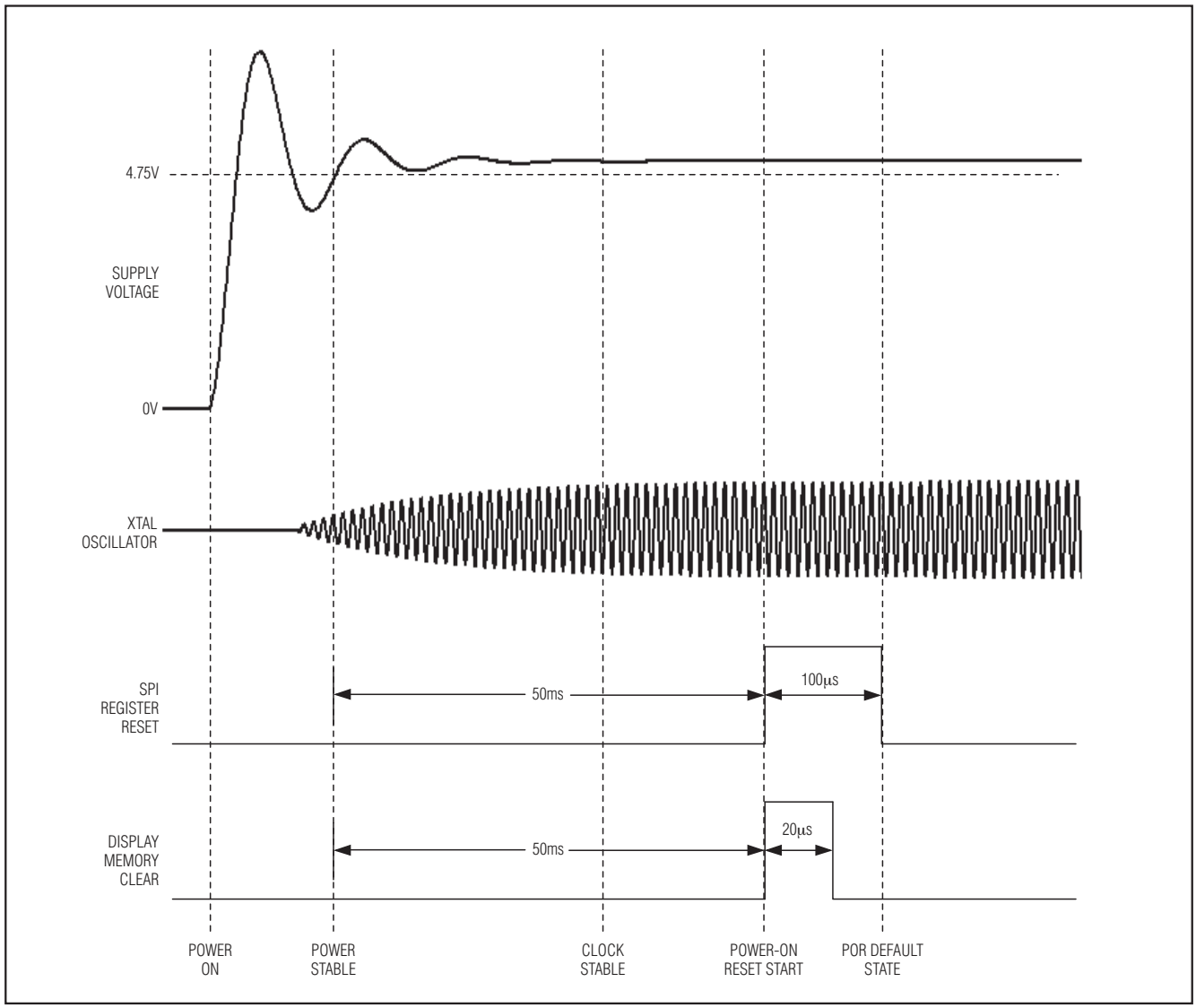


图22. 上电复位顺序

软件复位

MAX7456具有一个软件复位位(VM0[1])，当该位被置为高电平时，显示存储器被清除，除了OSD黑电平寄存器(OSDBL)，所有的寄存器复位为默认值。100µs (典型值)后，可查询STAT[6]确认复位过程是否完成。

硬件复位

MAX7456提供一个硬件复位输入($\overline{\text{RESET}}$)，其功能和POR相同。当$\overline{\text{RESET}}$被驱动至低电平时，所有寄存器复位至默认值，不能进行读/写操作。建立复位过程需要≥ 50ms宽的$\overline{\text{RESET}}$脉冲，在这期间不允许其他操作。$\overline{\text{RESET}}$上升沿100µs后，所有SPI寄存器被复位至默认值。$\overline{\text{RESET}}$上升沿20µs后，显示存储器的所有位置都被复位至默认值00H。$\overline{\text{RESET}}$优先级高于软件复位位。$\overline{\text{RESET}}$完毕后，可查询STAT[6]确认复位序列是否完成。

MAX7456寄存器说明

通过表3列出了所有的SPI寄存器来访问MAX7456操作，包括显示存储器和字符存储器访问等。通过SPI端口不能直接访问显示和字符存储器。请参考*应用信息*部分，了解对访问存储器所需的SPI操作步骤说明。

本数据资料采用的寄存器格式为REGISTER_NAME [BIT_NUMBERS]。例如，视频模式0寄存器的第1位表述为VM0[1]。

表3. 寄存器映射

WRITE ADDRESS	READ ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
00H	80H	VM0	Video Mode 0
01H	81H	VM1	Video Mode 1
02H	82H	HOS	Horizontal Offset
03H	83H	VOS	Vertical Offset
04H	84H	DMM	Display Memory Mode
05H	85H	DMAH	Display Memory Address High
06H	86H	DMAL	Display Memory Address Low
07H	87H	DMDI	Display Memory Data In
08H	88H	CMM	Character Memory Mode
09H	89H	CMAH	Character Memory Address High
0AH	8AH	CMAL	Character Memory Address Low
0BH	8BH	CMDI	Character Memory Data In
0CH	8CH	OSDM	OSD Insertion Mux
10H	90H	RB0	Row 0 Brightness
11H	91H	RB1	Row 1 Brightness
12H	92H	RB2	Row 2 Brightness
13H	93H	RB3	Row 3 Brightness
14H	94H	RB4	Row 4 Brightness
15H	95H	RB5	Row 5 Brightness
16H	96H	RB6	Row 6 Brightness
17H	97H	RB7	Row 7 Brightness
18H	98H	RB8	Row 8 Brightness
19H	99H	RB9	Row 9 Brightness
1AH	9AH	RB10	Row 10 Brightness
1BH	9BH	RB11	Row 11 Brightness
1CH	9CH	RB12	Row 12 Brightness
1DH	9DH	RB13	Row 13 Brightness
1EH	9EH	RB14	Row 14 Brightness
1FH	9FH	RB15	Row 15 Brightness
6CH	ECH	OSDBL	OSD Black Level
—	AxH	STAT	Status
—	BxH	DMDO	Display Memory Data Out
—	CxH	CMDO	Character Memory Data Out

X = 无关。

视频模式0寄存器(VM0)

写地址 = 00H，读地址 = 80H。

读/写访问：无限制。

写入该寄存器时，必须满足以下条件：

1) STAT[5] = 0，字符存储器(NVM)不忙。

2) DMM[2] = 0，显示存储器(SRAM)没有处于被清除的过程中。

BIT	DEFAULT	FUNCTION
7	0	Don't Care
6	0	Video Standard Select 0 = NTSC 1 = PAL
5, 4	00	Sync Select Mode (Table 1) 0x = Autosync select (external sync when LOS = 0 and internal sync when LOS = 1) 10 = External 11 = Internal
3	0	Enable Display of OSD Image 0 = Off 1 = On
2	0	Vertical Synchronization of On-Screen Data 0 = Enable on-screen display immediately 1 = Enable on-screen display at the next $\overline{VSYNC}$
1	0	Software Reset Bit When this bit is set, all registers are set to their default values and the display memory is cleared. When a stable 27MHz clock is present, this bit is automatically cleared internally after typically 100µs. The user does not need to write a 0 afterwards. SPI operations should not be performed during this time or unpredictable results may occur. The status of the bit can be checked by reading this register after typically 100µs. This register is not accessible for writing until the display memory clear operation is finished (typically 20µs).
0	0	Video Buffer Enable 0 = Enable 1 = Disable (VOUT is high impedance)

X = 无关。

视频模式1寄存器(VM1)

写地址 = 01H，读地址 = 81H。

读/写访问：无限制。

BIT	DEFAULT	FUNCTION
7	0	Background Mode (See Table 4) 0 = The Local Background Control bit (see DMM[5] and DMDI[7]) sets the state of each character background. 1 = Sets all displayed background pixels to gray. The gray level is specified by bits VM1[6:4] below. This bit overrides the local background control bit. **Note:** In internal sync mode, the background mode bit is set to 1.
6, 5, 4	100	Background Mode Brightness (% of OSD White Level) 000 = 0% 001 = 7% 010 = 14% 011 = 21% 100 = 28% 101 = 35% 110 = 42% 111 = 49%
3, 2	01	Blinking Time (BT) 00 = 2 fields (33ms in NTSC mode, 40ms in PAL mode) 01 = 4 fields (67ms in NTSC mode, 80ms in PAL mode) 10 = 6 fields (100ms in NTSC mode, 120ms in PAL mode) 11 = 8 fields (133ms in NTSC mode, 160ms in PAL mode)
1, 0	11	Blinking Duty Cycle (On : Off) 00 = BT : BT 01 = BT : (2 x BT) 10 = BT : (3 x BT) 11 = (3 x BT) : BT

水平位置寄存器(HOS)

写地址 = 02H，读地址 = 82H。

读/写访问：无限制(图23)。

BIT	DEFAULT	FUNCTION
7, 6	00	Don't Care
5–0	10 0000	Horizontal Position Offset (OSD video is not inserted into the horizontal blanking interval) 00 0000 = Farthest left (-32 pixels) ⋮ 10 0000 = No horizontal offset ⋮ 11 1111 = Farthest right (+31 pixels)

垂直位置寄存器(VOS)

写地址 = 03H，读地址 = 83H。

读/写访问：无限制(图23)。

BIT	DEFAULT	FUNCTION
7, 6, 5	000	Don't Care
4–0	1 0000	Vertical Position Offset (OSD video can be vertically shifted into the vertical blanking lines) 0 0000 = Farthest up (+16 pixels) • • • 1 0000 = No vertical offset • • • 1 1111 = Farthest down (-15 pixels)

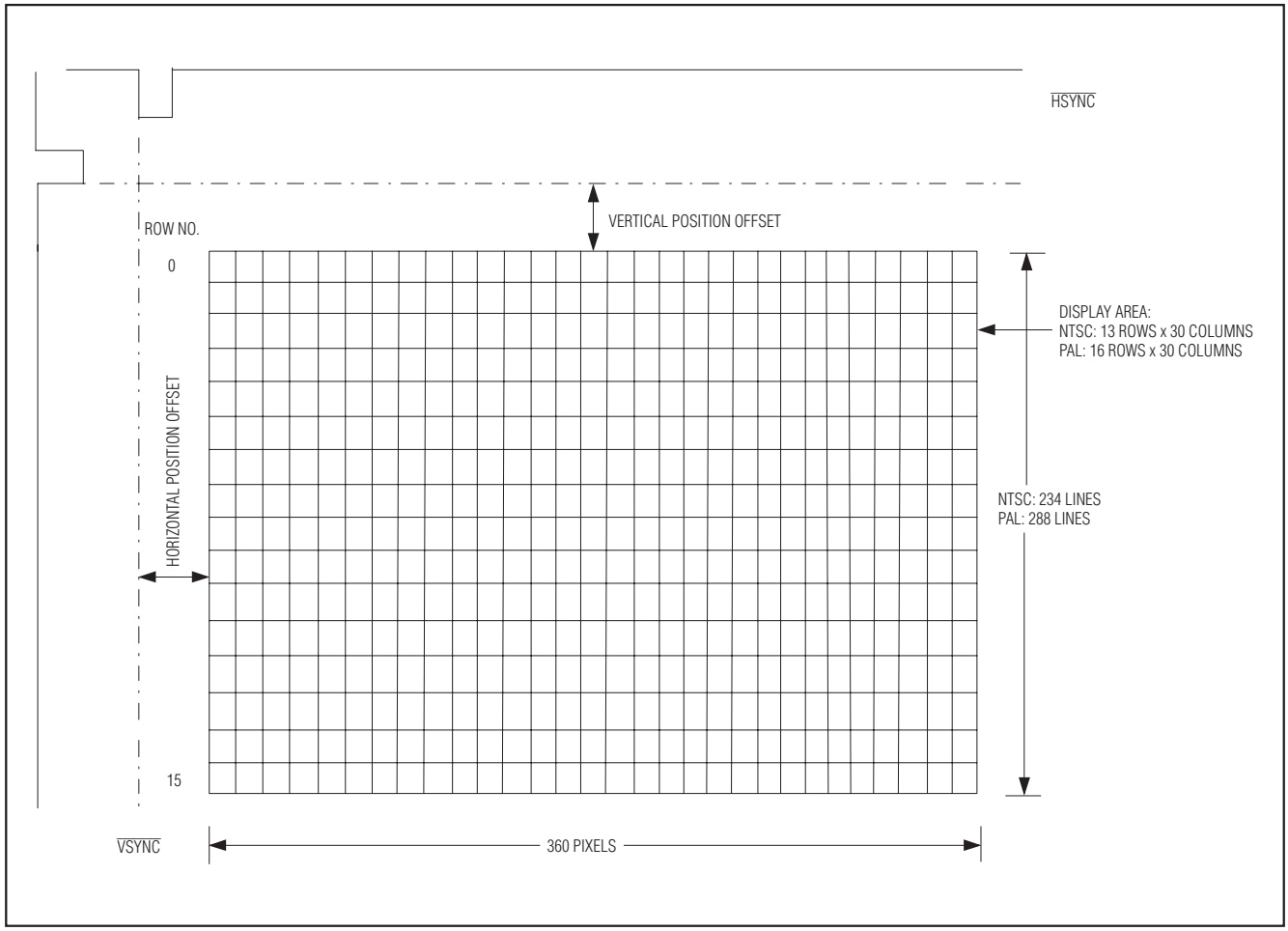


图23. 字符显示区

显示存储器模式寄存器(DMM)

写地址 = 04H，读地址 = 84H。

读/写访问：无限制。

写入该寄存器时，必须满足以下条件：

DMM[2] = 0，显示存储器没有处于清除过程。

BIT	DEFAULT	FUNCTION
7	0	Don't Care
6	0	Operation Mode Selection 0 = 16-bit operation mode The 16-bit operation mode increases the speed at which the display memory can be updated. When writing to the display memory, the attribute byte is not entered through the SPI-compatible interface. It is entered automatically by copying DMM[5:3] to a character's attribute byte when a new character is written, thus reducing the number of SPI write operations per character from two to one (Figure 19). When in this mode, all characters written to the display memory have the same attribute byte. This mode is useful because successive characters commonly have the same attribute. This mode is distinct from the 8-bit operation mode where a character attribute byte must be written each time a character address byte is written to the display memory (see Table 5). When reading data from the display memory, both the Character Address byte and Character Attribute byte are transferred with the SPI-compatible interface (Figure 18). 1 = 8-bit operation mode The 8-bit operation mode provides maximum flexibility when writing characters to the display memory. This mode enables writing individual Character Attribute bytes for each character (see Table 5). When writing to the display memory, DMAH[1] = 0 directs the data to the Character Address byte and DMAH[1] = 1 directs the Character Attributes byte to the data. This mode is distinct from the 16-bit operation mode where the attribute bits are automatically copied from DMM[5:3] when a character is written.
5	0	Local Background Control Bit, LBC (see Table 4) Applies to characters written in 16-bit operating mode. 0 = Sets the background pixels of the character to the video input (VIN) when in external sync mode. 1 = Sets the background pixels of the character to the background mode brightness level defined by VM1[6:4] in external or internal sync mode. **Note:** In internal sync mode, the local background control bit behaves as if it is set to 1.
4	0	Blink Bit, BLK Applies to characters written in 16-bit operating mode. 0 = Blinking off 1 = Blinking on **Note:** Blinking rate and blinking duty cycle data in the Video Mode 1 (VM1) register are used for blinking control. In external sync mode: when the character is not displayed, VIN is displayed. In internal sync mode: when the character is not displayed, background mode brightness is displayed (see VM1[6:4]).
3	0	Invert Bit, INV Applies to characters written in 16-bit operating mode (see Figure 24). 0 = Normal (white pixels display white, black pixels display black) 1 = Invert (white pixels display black, black pixels display white)

显示存储器模式寄存器(DMM) (续)

BIT	DEFAULT	FUNCTION
2	0	Clear Display Memory 0 = Inactive 1 = Clear (fill all display memories with zeros) **Note:** This bit is automatically cleared after the operation is completed (the operation requires 20µs). The user does not need to write a 0 afterwards. The status of the bit can be checked by reading this register. This operation is automatically performed: a) On power-up b) Immediately following the rising edge of $\overline{\text{RESET}}$ c) Immediately following the rising edge of $\overline{\text{CS}}$ after VM0[1] has been set to 1
1	0	Vertical Sync Clear Valid only when clear display memory = 1, (DMM[2] = 1) 0 = Immediately applies the clear display-memory command, DMM[2] = 1 1 = Applies the clear display-memory command, DMM[2] = 1, at the next $\overline{\text{VSYNC}}$ time
0	0	Auto-Increment Mode Auto-increment mode increases the speed at which the display memory can be written by automatically incrementing the character address for each successive character written. This mode reduces the number of SPI commands, and thus the time needed to write a string of adjacent characters. This mode is useful when writing strings of characters written from left-to-right, top-to-bottom, on the display (see Table 5). 0 = Disabled 1 = Enabled When this bit is enabled for the first time, data in the Display Memory Address (DMAH[0] and DMAL[7:0]) registers are used as the starting location to which the data is written. When performing the auto-increment write for the display memory, the 8-bit address is internally generated, and therefore only 8-bit data is required by the SPI-compatible interface (Figure 21). The content is to be interpreted as a Character Address byte if DMAH[1] = 0 or a Character Attribute byte if DMAH[1] = 1. This mode is disabled by writing the escape character 1111 1111. If the Clear Display Memory bit is set, this bit is reset internally.

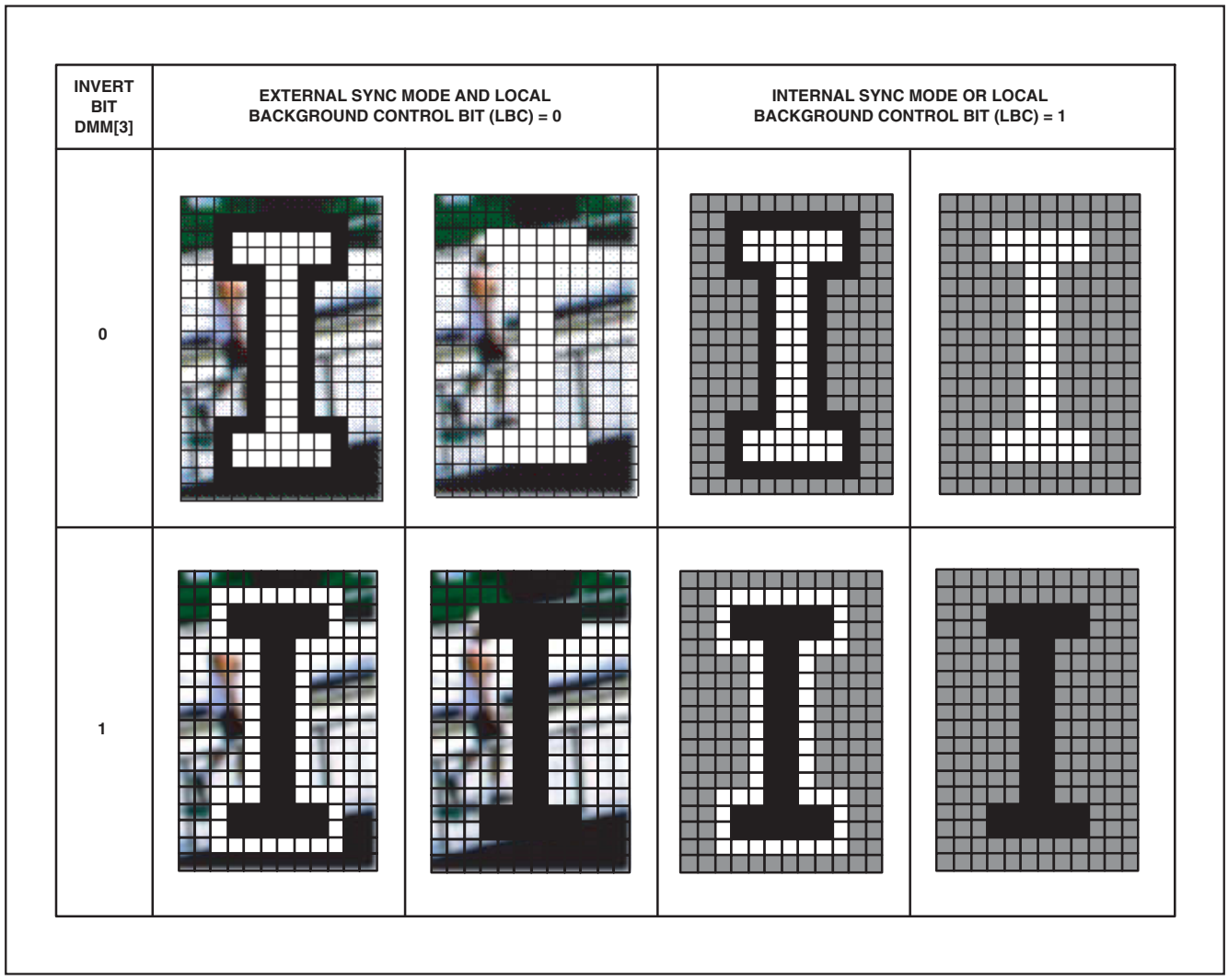


图24. 字符属性位实例：反色和本地背景控制

表4. 字符背景控制

SYNC MODE	BACKGROUND MODE, VM1[7]	LOCAL BACKGROUND CONTROL BIT, LBC DMM[5], DMDI[7]	CHARACTER BACKGROUND PIXEL
External	0	0	Input Video
	0	1	Gray
	1	X	Gray
Internal	X	X	Gray

X = 无关。

显示存储器地址高位寄存器(DMAH)

写地址 = 05H，读地址 = 85H。

读/写访问：无限制。

写入该寄存器时，必须满足以下条件：

DMM[2] = 0，显示存储器没有处于清除过程。

BIT	DEFAULT	FUNCTION
7–2	0000 00	Don't Care
1	0	Byte Selection Bit This bit is valid only when in the 8-bit operation mode (DMM[6] = 1). 0 = Character Address byte is written to or read (DMDI[7:0] contains the Character Address byte). 1 = Character Attribute byte is written to or read (DMDI[7:0] contains the Character Attribute byte).
0	0	Display Memory Address Bit 8 This bit is the MSB of the display-memory address. The display-memory address sets the location of a character on the display (Figure 10). The lower order 8 bits of the display-memory address is found in DMAL[7:0].

显示存储器地址低位寄存器(DMAL)

写地址 = 06H，读地址 = 86H。

读/写访问：无限制。

写入该寄存器时，必须满足以下条件：

DMM[2] = 0，显示存储器没有处于清除过程。

BIT	DEFAULT	FUNCTION
7–0	0000 0000	Display Memory Address Bits 7–0 This byte is the lower 8 bits of the display-memory address. The display-memory address sets the location of a character on the display (Figure 10). The MSB of the display-memory address is DMAH[0].

显示存储器数据输入寄存器(DMDI)

写地址 = 07H，读地址 = 87H。

读/写访问：无限制。

写入该寄存器时，必须满足以下条件：

DMM[2] = 0，显示存储器没有处于清除过程。

BIT	DEFAULT	FUNCTION
7–0	0000 0000	Character Address or Character Attribute byte to be stored in the display memory. 8-Bit Operation Mode (DMM[6] = 1) If DMAH[1] = 0, the content is to be interpreted as a Character Address byte, where Bits 7–0 = Character Address bits, CA[7:0] (Figure 12). If DMAH[1] = 1, the content is to be interpreted as a Character Attribute byte where Bit 7 = Local Background Control bit, LBC (Figure 24 and Table 4) Bit 6 = Blink bit, BLK Bit 5 = Invert bit, INV (see Figure 24) Bit 4–0 = 0 (The LBC, BLK, and INV bits are described in the Display Memory Mode register.) 16-Bit Operation Mode (DMM[6] = 0) The content is always interpreted as a Character Address byte where bits 7–0 = CA[7:0] (Figure 12). Auto-Increment Mode (DMM[0] = 1) The character address CA[7:0] = FFH is reserved for use as an escape character that terminates the auto-increment mode. Therefore, the character located at address FFH is not available for writing to the display memory when in auto-increment mode. In all other modes, character FFH is available.

字符存储器模式寄存器(CMM)

写地址 = 08H，读地址 = 88H。

读/写访问：无限制。

写入该寄存器时，必须满足以下条件：

1) STAT[5] = 0，字符存储器(NVM)不忙。

2) VM0[3] = 0，OSD被禁止。

BIT	DEFAULT	FUNCTION
7–0	0000 0000	Only whole characters (54 bytes) can be written to or read from the nonvolatile character memory (NVM) at one time. This is done through the (64 byte) shadow RAM (Figure 13). The shadow RAM is accessed through the SPI port one byte at a time. The shadow RAM is written to and read from NVM by the following procedures: **Writing to NVM** 1010 XXXX = Write to NVM array from shadow RAM. The 64 bytes from shadow RAM are written to the NVM array at the character-memory address location (CMAH, CMAL) (Figure 13). The character memory is busy for approximately 12ms during this operation. During this time, STAT[5] is automatically set to 1. The Character Memory Mode register is cleared and STAT[5] is reset to 0 after the write operation has been completed. The user does not need to write zeros afterwards. **Reading from NVM** 0101 XXXX = Read from NVM array into shadow RAM. The 64 bytes corresponding to the character-memory address (CMAH, CMAL) are read from the NVM array into the shadow RAM (Figure 13). The character memory is busy for approximately 0.5µs during this operation. The CMM register is cleared after the operation is completed. The user does not need to write zeros afterwards. During this time, STAT[5] is automatically set to 1. STAT[5] is reset to 0 when the read operation has been complete. If the display has been enabled (VM0[3] = 1) or the character memory is busy (STAT[5] = 1), NVM read/write operation commands are ignored and the corresponding registers are not updated. However, all the registers can be read at any time. For all the character-memory operations, the character address is formed with Character Memory Address High (CMAH[7:0]) and Character Memory Address Low (CMAL[7:0]) register bits (Figures 11, 12, and 13).

X = 无关。

字符存储器地址高位寄存器(CMAH)

写地址 = 09H，读地址 = 89H。

读/写访问：无限制。

写入该寄存器时，必须满足以下条件：

1) STAT[5] = 0，字符存储器(NVM)不忙。

2) VM0[3] = 0，OSD被禁止。

BIT	DEFAULT	FUNCTION
7–0	0000 0000	Character Memory Address Bits These 8 bits point to a character in the character memory (256 characters total in NVM) (Figures 10 and 12).

字符存储器地址低位寄存器(CMAL)

写地址 = 0AH，读地址 = 8AH。

读/写访问：无限制。

写入该寄存器时，必须满足以下条件：

1) STAT[5] = 0，字符存储器(NVM)不忙。

2) VM0[3] = 0，OSD被禁止。

BIT	DEFAULT	FUNCTION
7, 6	00	Don't Care
5–0	00 0000	Character Memory Address Bits These 6 bits point to one of the 64 bytes (only 54 used) that represent a 4-pixel group in the character (Figures 10 and 11).

字符存储器数据输入寄存器(CMDI)

写地址 = 0BH，读地址 = 8BH。

读/写访问：无限制。

写入该寄存器时，必须满足以下条件：

1) STAT[5] = 0，字符存储器(NVM)不忙。

2) VM0[3] = 0，OSD被禁止。

BIT	DEFAULT	FUNCTION
7, 6	NA	Leftmost pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
5, 4	NA	Left center pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
3, 2	NA	Right center pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
1, 0	NA	Rightmost pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)

NA = 不适用。

OSD插入复用寄存器(OSDM)

写地址 = 0CH，读地址 = 8CH。

读/写访问：无限制。

BIT	DEFAULT	FUNCTION
7, 6	00	Don't Care
5, 4, 3	011	OSD Rise and Fall Time—typical transition times between adjacent OSD pixels 000: 20ns (maximum sharpness/maximum crosscolor artifacts) 001: 30ns 010: 35ns 011: 60ns 100: 80ns 101: 110ns (minimum sharpness/minimum crosscolor artifacts)
2, 1, 0	011	OSD Insertion Mux Switching Time–typical transition times between input video and OSD pixels 000: 30ns (maximum sharpness/maximum crosscolor artifacts) 001: 35ns 010: 50ns 011: 75ns 100: 100ns 101: 120ns (minimum sharpness/minimum crosscolor artifacts)

第N行亮度寄存器(RB0–RB15)

地址 = 10H + 行号；写地址 = 10H至1FH，读地址 = 90H至9FH，读/写访问：无限制。

第一行的行号为0，最后一行的行号在NTSC制式中为13，在PAL制式中为15 (请参考图23)。

BIT	DEFAULT	FUNCTION
7–4	0000	Don't Care
3, 2	00	Character Black Level —All the characters in row N use these brightness levels for the black pixel, in % of OSD white level. 00 = 0% 01 = 10% 10 = 20% 11 = 30%
1, 0	01	Character White Level —All the characters in row N use these brightness levels for the white pixel, in % of OSD white level. 00 = 120% 01 = 100% 10 = 90% 11 = 80%

OSD黑电平寄存器(OSDBL)

写地址 = 6CH，读地址 = ECH。

读/写访问：该寄存器含有4个工厂预设的位[3:0]，不能对其进行修改。因此，修改第4位时，首先读取该寄存器，修改第4位，然后写回更新后的字节。

BIT	DEFAULT	FUNCTION
7–5	000	Don't Care
4	1	OSD Image Black Level Control This bit enables the alignment of the OSD image black level with the input image black level at VOUT. Always enable this bit following power-on reset to ensure the correct OSD image brightness. 0 = Enable automatic OSD black level control 1 = Disable automatic OSD black level control
0–3	xxxx	These bits are factory preset. To ensure proper operation of the MAX7456, do not change the values of these bits.

xxxx = 工厂预设—可能是16个值的任何一个。这一数值被永久存储在MAX7456中，上电复位或者硬件复位后，总是被恢复为工厂预设值。

状态寄存器(STAT)

读地址 = AxH。

读/写访问：只读。

BIT	DEFAULT	FUNCTION
7	NA	Don't Care
6	NA	Reset Mode 0 = Clear when power-up reset mode is complete. Occurs 50ms (typ) following stable V_{DD} (Figure 22) 1 = Set when in power-up reset mode
5	NA	Character Memory Status 0 = Available to be written to or read from 1 = Unavailable to be written to or read from
4	NA	$\overline{\text{VSYNC}}$ Output Level 0 = Active during vertical sync time 1 = Inactive otherwise
3	NA	$\overline{\text{HSYNC}}$ Output Level 0 = Active during horizontal sync time 1 = Inactive otherwise
2	NA	Loss-of-Sync (LOS) 0 = Sync Active. Asserted after 32 consecutive input video lines. 1 = No Sync. Asserted after 32 consecutive missing input video lines.
1	NA	0 = NTSC signal is not detected at VIN 1 = NTSC signal is detected at VIN
0	NA	0 = PAL signal is not detected at VIN 1 = PAL signal is detected at VIN

NA = 不适用。
X = 无关。

显示存储器数据输出寄存器(DMDO)

读地址 = BxH。

读/写访问：只读。

写入该寄存器时，必须满足以下条件：

DMM[2] = 0，显示存储器没有处于清除过程。

BIT	DEFAULT	FUNCTION
7–0	NA	Character Address or Character Attribute byte to be read from the display memory. 8-Bit Operation Mode (DMM[6] = 1): If DMAH[1] = 0, the content is to be interpreted as a Character Address byte, where Bits 7–0 = Character Address bits, CA[7:0] (Figure 12) If DMAH[1] = 1, the content is to be interpreted as a Character Attribute byte where Bit 7 = Local Background Control bit, LBC (see Figure 24 and Table 4) Bit 6 = Blink bit, BLK Bit 5 = Invert bit, INV (see Figure 24) Bit 4–0 = 0 The LBC, BLK, and INV bits are described in the Display Memory Mode register. 16-Bit Operation Mode (DMM[6] = 0): The content is to be interpreted as a Character Address byte, where Bits 7–0 = CA[7:0] (see Figure 12) followed by a Character Attribute byte, where Bit 7 = 0 Bit 6 = Local Background Control bit, LBC (see Figure 24 and Table 4) Bit 5 = Blink bit, BLK Bit 4 = Invert bit, INV (see Figure 24) Bit 3–0 = 0 The LBC, BLK, and INV bits are described in the Display Memory Mode register.

NA = 不适用。
X = 无关。

字符存储器数据输出寄存器(CMDO)

读地址 = CxH。

读/写访问：只读。

写入该寄存器时，必须满足以下条件：

1) STAT[5] = 0，字符存储器(NVM)不忙。

2) VM0[3] = 0，OSD被禁止。

BIT	DEFAULT	FUNCTION
7, 6	NA	Leftmost pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
5, 4	NA	Left center pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
3, 2	NA	Right center pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
1, 0	NA	Rightmost pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)

NA = 不适用。
X = 无关。

应用信息

字符存储器操作

一次只能从NVM字符存储器写入或者读取全部字符(54字节的象素数据)。这可以通过(64字节)镜像RAM实现(请参考图13)。通过SPI端口，每次访问镜像RAM的一个字节。通过一条SPI命令从NVM写入或者读取镜像RAM。

向NVM字符存储器写入字符字节的步骤

写入一个新字符：

1) 写入VM0[3] = 0，禁止OSD图像显示。
2) 写入CMAH[7:0] = xxH，选择要写入的字符(0–255) (图10和图13)。
3) 写入CMAL[7:0] = xxH，选择要写入字符中的4个象素字节(0–63) (图10和图13)。
4) 写入CMDI[7:0] = xxH，设置字符所选部分的象素值(图11和图13)。
5) 重复步骤3和步骤4，直到字符数据的所有54个字节被装入到镜像RAM中。
6) 写入CMM[7:0] = 1010xxxx，从镜像RAM写入到NVM阵列中(图13)。在这一操作过程中，字符存储器忙时间大约为12ms。可以读取STAT[5]确认NVM写过程是否完成。
7) 写入VM0[3] = 1，使能OSD图像显示。

修改已有的字符：

1) 写入VM0[3] = 0，禁止OSD图像显示。
2) 写入CMAH[7:0] = xxH，选择要修改的字符(0–255) (图10和图13)。
3) 写入CMM[7:0] = 0101xxxx，将字符数据从NVM读入到镜像RAM中(图13)。
4) 写入CMAL[7:0] = xxH，选择要修改的字符中的4个象素字节(0–63) (图10和图13)。
5) 读取CMDO[7:0] = xxH，读取要修改的4个象素数据字节(图11和图13)。
6) 根据要求修改4象素字节。
7) 写入CMDI[7:0] = xxH，将修改后的4象素数据字节写回到镜像RAM中(图11和图13)。
8) 根据需要重复步骤4到步骤7，直到所有的象素装入到镜像RAM中。
9) 写入CMM[7:0] = 1010xxxx，将镜像RAM数据写入到NVM中(图13)。在这一操作过程中，字符存储器忙的时间典型为12ms。可以读取STAT[5]确认NVM写过程是否完成。
10) 写入VM0[3] = 1，使能OSD图像显示。

从字符存储器读取字符字节的步骤

1) 写入VM0[3] = 0，禁止OSD图像。
2) 写入CMAH[7:0] = xxH，选择要读取的字符(0–255) (图10和图13)。
3) 写入CMM[7:0] = 0101xxxx，将字符数据从NVM读入到镜像RAM中(图13)。
4) 写入CMAL[7:0] = xxH，选择要读取的字符中的4个象素字节(0–63) (图10和图13)。
5) 读取CMDO[7:0] = xxH，读取数据的所选4个象素字节(图11和图13)。
6) 重复步骤4和步骤5，读取4象素数据的其他字节。
7) 写入VM0[3] = 1，使能OSD图像显示。

显示存储器操作

以下两个步骤支持对OSD图像的查看。读写显示存储器时不需要这些步骤：

1) 写入VM0[3] = 1，使能OSD图像显示。
2) 写入OSDBL[4] = 0，使能自动OSD黑电平控制。这保证了正确的OSD图像亮度。该寄存器含有4个工厂预设的位[3:0]，不能修改这些位。因此，修改第4位时，首先读取OSDBL[7:0]，修改第4位，然后写回更新后的字节。

清除显示存储器步骤

写入DMM[2] = 1，以启动清除显示存储器操作。这一操作一般需要20µs。在清除操作完成之前，不能再次写入显示存储器模式寄存器。操作完成后，DMM[2]被自动复位至零。

在8位模式下，写入显示存储器的步骤

向显示存储器写入字符时，8位工作模式最灵活。这一模式支持为每一字符写入单独的字符属性字节(请参考表5)。这一模式不同于16位工作模式，在16位工作模式下，当写入一个字符时，从DMM[5:3]自动复制其字符属性字节(图19)。

写入DMM[6] = 1，选择8位工作模式。

向显示存储器写入字符地址字节：

1) 写入DMAH[1] = 0，以写入字符地址字节。
2) 写入DMAH[0] = x，以选择MSB，写入DMAL[7:0] = xxH，以选择要写入字符数据地址的低位数据。该地址确定了字符在显示器上的位置(请参考图10)。
3) 将要写入显示存储器的字符地址字节(CA[7:0])写入到DMDI[7:0]中(请参考图10、图12和图19)。

向显示存储器写入字符属性字节：

1) 写入DMAH[1] = 1，以写入字符属性字节。
2) 写入DMAH[0] = x，选择MSB，写入DMAL[7:0] = xxH，以选择要写入字符数据地址的低位数据。该地址确定了字符在显示器上的位置(图10)。
3) 将要写入显示存储器的字符属性字节写入到DMDI[7:0]中(请参考图10和图19)。

在16位模式下，写入显示存储器的步骤

16位工作模式提高了显示存储器刷新率。这是因为，写入一个新字符时，将DMM[5:3]自动复制到字符属性字节，从而把每个字符SPI写操作的次数由两次降到一次(图19)。在这一模式下，所有写入显示存储器的字符都有相同的属性字节。该模式很有用，因为连续字符通常有相同的属性。该模式不同于8位工作模式，8位工作模式下，当字符地址字节每次写入到显示存储器时，必须写入字符属性字节(请参考表5)。

1) 写入DMM[6] = 0，选择16位工作模式。
2) 写入DMM[5:3] = xxx，设置本地背景控制(LBC)、闪烁(BLK)和反色(INV)属性位，在16位工作模式时，这些设置将应用于写入到显示存储器的所有字符上。
3) 写入DMAH[0] = x，选择要写入字符数据地址的MSB，写入DMAL[7:0] = xxH，选择低位地址。该地址确定字符在显示器上的位置(请参考图10)。
4) 将要写入到显示存储器的字符地址字节(CA[7:0])写入到DMDI[7:0]中。一并存储这些字节和来自DMM[5:3]的字符属性字节(图12和图19)。

在自动递增模式中，写入显示存储器的步骤

自动递增模式自动递增每一连续写入字符的字符地址，从而提高了写入显示存储器的速度。在显示器上从左至右，从上至下写字符串时，可采用该模式。这一模式减少了SPI命令的数量(请参考表5)。

8位工作模式时：

1) 写入DMAH[1] = 0，选择是否写入字符地址字节；写入DMAH[1] = 1，选择是否写入字符属性字节。
2) 自动递增模式下，写入DMAH[0] = X，选择起始地址的MSB；写入DMAL[7:0] = XX，选择起始地址的低位地址数据。该地址确定首个字符在显示器上的位置(请参考图10和图21)。
3) 写入DMM[0] = 1，设置自动递增模式。
4) 写入DMM[6] = 1，设置8位工作模式。
5) 按特定字符顺序写入CA数据，将文本显示在屏幕上，此为单字节操作。自动递增模式下，自动设置DMDI[7:0]的地址。写操作之后，显示存储器地址自动递增，直至显示存储器地址末尾。
6) 写入CA = FFh，结束自动递增模式。

注意：在自动递增模式下，不能使用存储在CA[7:0] = FFh的字符。自动递增模式结束之前，读操作无效。

16位工作模式时：

1) 自动递增模式下，写入DMAH[0] = X，选择起始地址的MSB；写入DMAL[7:0] = XX，选择起始地址的低位地址数据。该地址确定首个字符在显示器上的位置(请参考图10和图21)。
2) 写入DMM[0] = 1，设置自动递增模式。
3) 写入DMM[6] = 0，设置16位工作模式。
4) 写入DMM[5:3] = XXX，设置将应用于所有字符的本地背景控制(LBC)、闪烁(BLK)和反色(INV)属性位。

5) 按特定字符顺序写入CA数据，将文本显示在屏幕上。这些将同来自DMM[5:3]的字符属性字节一并存储，请参考图19。此为单字节操作。自动递增模式下，自动设置DMDI[7:0]的地址。写操作之后，显示存储器地址自动递增，直至显示存储器地址末尾。

6) 写入CA = FFh，结束自动递增模式。

注意：在自动递增模式下，不能使用存储在CA[7:0] = FFh的字符。自动递增模式结束之前，读操作无效。

8位模式下，读取显示存储器的步骤

1) 写入DMM[6] = 1，选择8位工作模式。
2) 写入DMAH[1] = 0，读取字符地址字节，或者写入DMAH[1] = 1，读取字符属性字节。
3) 写入DMAH[0]，选择需要读取数据的地址MSB (图10)。
4) 写入DMAL[7:0]，选择需要读取数据地址的MSB以外的低位数据(图10)。
5) 读取DMDO[7:0]，从显示存储器中的所选位置读取数据(图10)。

16位模式下，读取显示存储器的步骤

1) 写入DMM[6] = 0，选择16位工作模式。
2) 写入DMAH[0] = x，选择要读取字符数据地址的MSB，写入DMAL[7:0] = xxH，选择地址的低位数据。该地址确定字符在显示器上的位置(请参考图10)。
3) 读取DMDO[15:0]，从显示存储器中所选位置读取字符地址字节和字符属性字节。第一个数据字节是字符地址(CA[7:0])，第二个字节包含字符属性位(图20)。注意，读取操作时，字符属性字节的位排列不同于写入操作时的位排列。请参考*显示存储器数据输出寄存器(DMDO)*部分和图20，了解读取操作时对属性位中位排列说明。

注意：如果内部显示存储器读操作请求和SPI显示存储操作同时发生，则忽略内部读操作请求，在这段时间内，字符显示可能会瞬时变暗。请参考*同步OSD更新*部分。

同步OSD更新

如果内部显示存储器读操作请求和SPI显示存储器操作同时发生，字符显示会瞬时变暗。在场消隐间隔期间写入显示存储器可以防止OSD图像瞬时变暗。使用$\overline{\text{VSYNC}}$作为主机处理器中断，启动向显示存储器进行写操作以实现这一功能。或者，在写入显示存储器之前，可同步禁止OSD图像，写入之后再同步使能(请参考VM0[3:2])。

具有公共时钟的多个OSD

MAX7456提供一个TTL时钟输出(CLKOUT)，可驱动另一个MAX7456的CLKIN引脚。使用外部时钟驱动器可驱动两个或者多个MAX7456元件。这种安排可通过一片带有晶振的MAX7456为多个MAX7456元件提供时钟信号，降低系统成本(图25).

表5. 显示存储器访问模式和SPI操作

OPERATING MODE	AUTO-INCREMENT MODE DISABLED DMM[0] = 0	No. OF READ OPERATIONS	No. OF WRITE OPERATIONS	AUTO-INCREMENT MODE ENABLED DMM[0] = 1	No. OF WRITE OPERATIONS
16-Bit Mode DMM[6] = 0	One-time setup	2	1	One-time setup	6
	Per character	3	3	Per character	1
8-Bit Mode DMM[6] = 1	One-time setup	1	1	One-time setup	6
	Per character	6	6	Per character	1

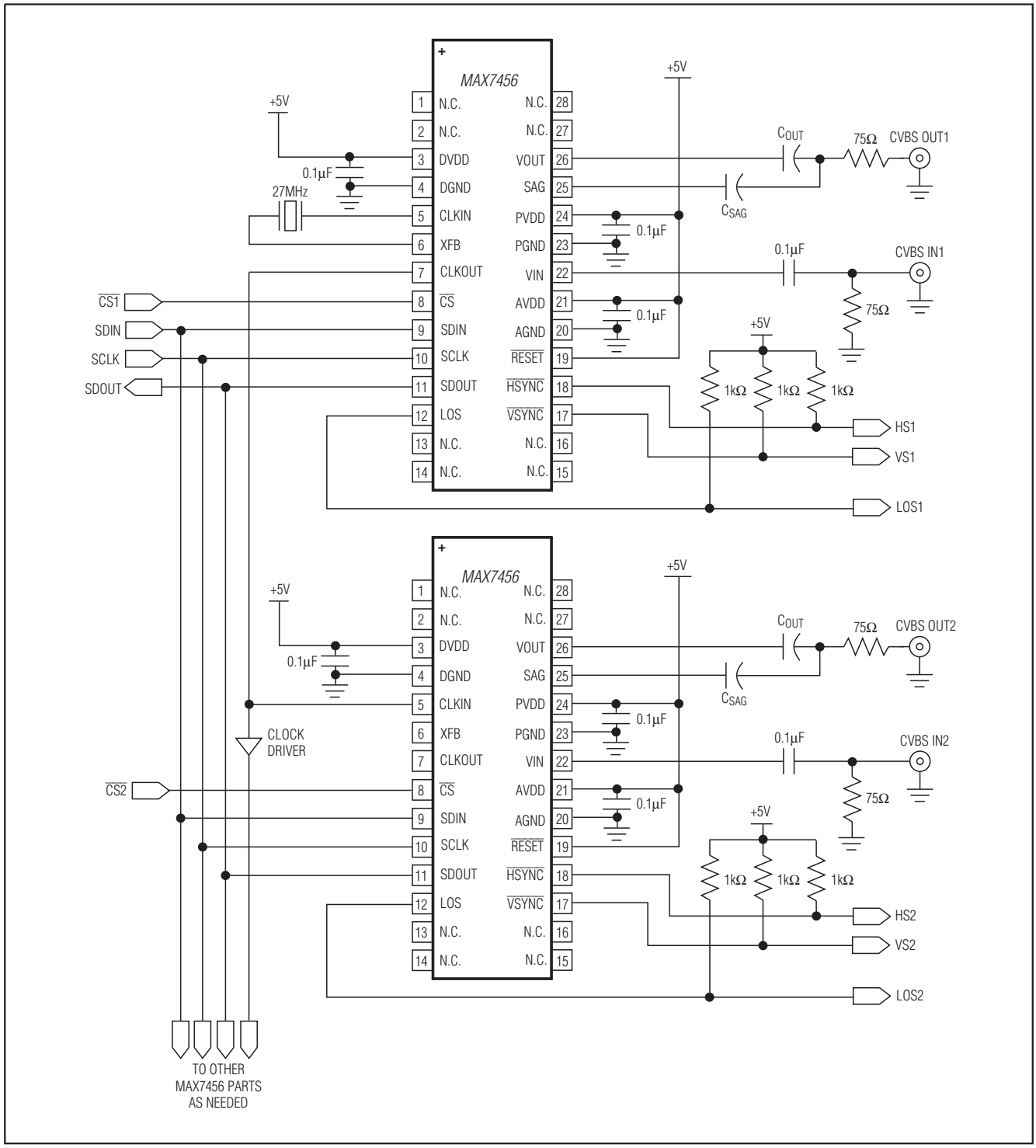


图25. 典型的具有菊形链接时钟的多个OSD

时钟晶体选择

选择一个27MHz并联谐振的基频模式晶体，不需要外部负载电容。片内包含了Pierce振荡器需要的所有电容。

电源和旁路

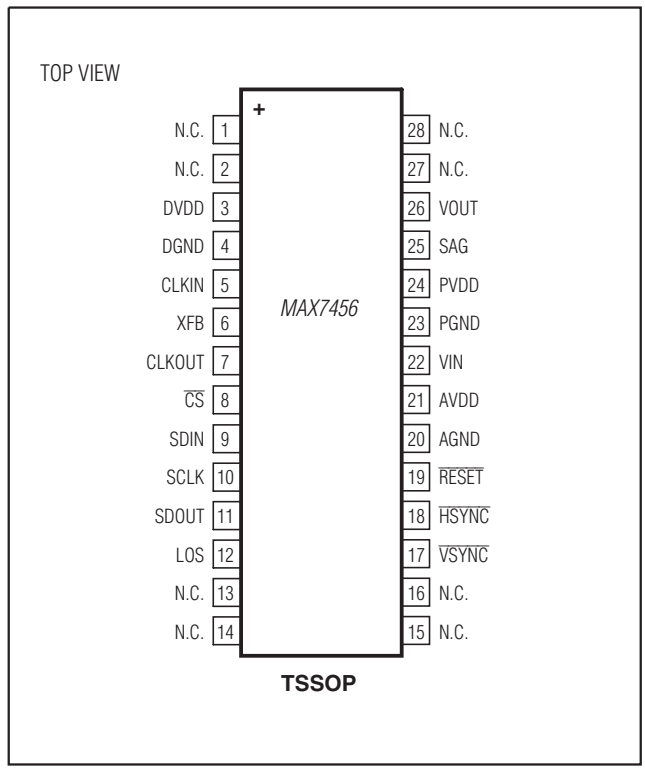
MAX7456采用三条独立的电源线路。每一电源电压必须在+4.75V至+5.25V范围内。将数字电源和模拟电源以及视频驱动器电源线路分开，以防止高频数字噪声耦合至视频输出。所有三个电源都应有同样的直流电压。采用0.1µF电容将每一电源旁路至地，应尽可能靠近IC引脚放置该电容。器件没有电源排序要求。

布局考虑

为实现最佳性能，应尽可能缩短VIN和VOUT走线。将所有交流耦合电容和75Ω匹配电阻靠近器件放置，电阻端接于可靠的模拟地平面。由于MAX7456 TSSOP封装下面有裸焊盘(EP)，因此，在封装下面不要走线，以防止出现短路。参考MAX7456评估板作为PCB布局实例。

为达到散热目的，应将EP连接至PCB元件侧同样尺寸的焊盘。将该焊盘通过几个镀孔连接至焊接侧覆铜层，以便器件散热。焊接侧铜焊盘区面积应比EP区大。建议将EP连接至地，但不是必须的。不要把EP作为器件的唯一地连接。

引脚配置

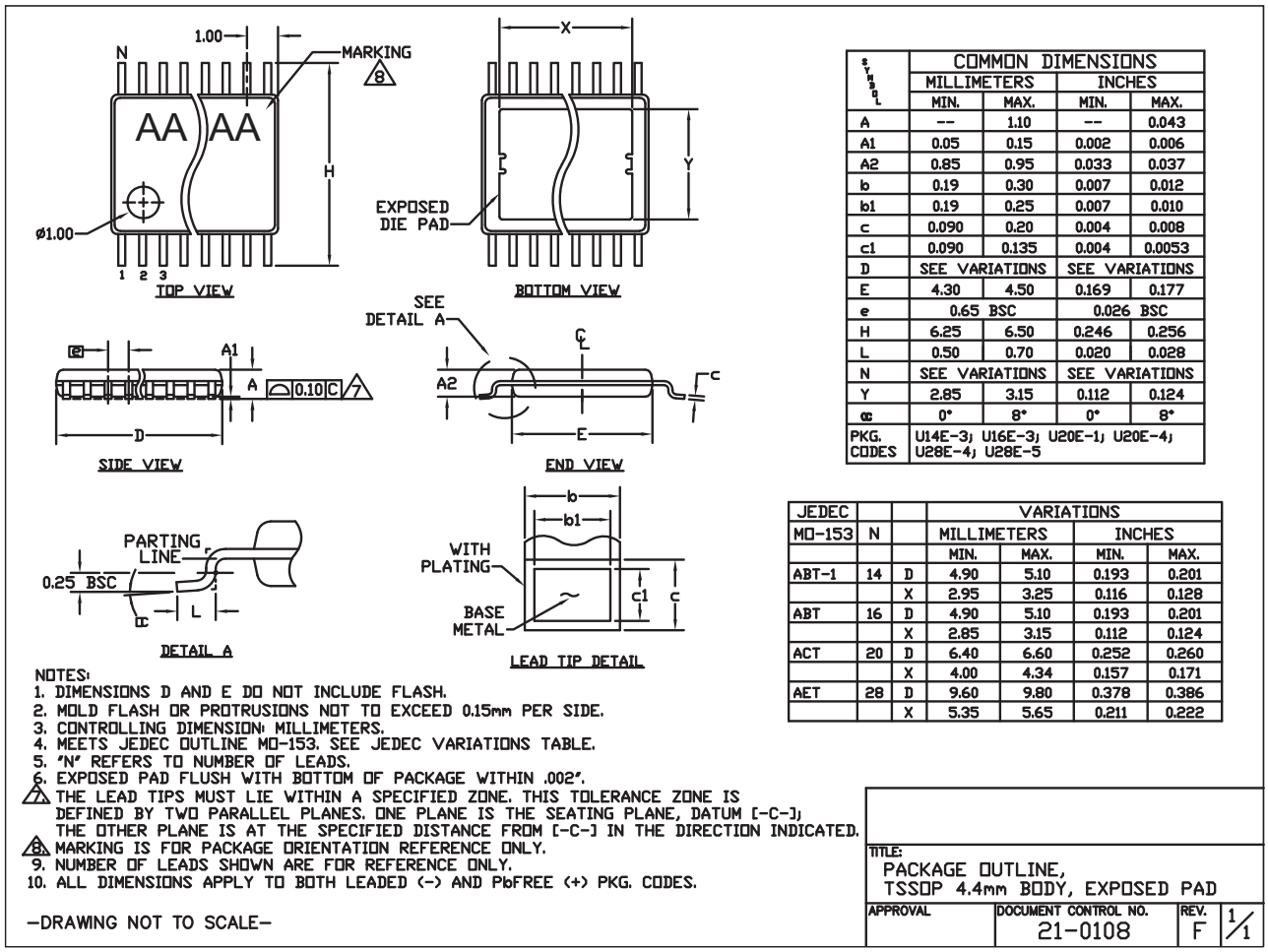


芯片信息

PROCESS: BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局，请查询 www.maxim-ic.com.cn/packages。



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.05	0.15	0.002	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°
PKG. CODES	U14E-3; U16E-3; U20E-1; U20E-4; U28E-4; U28E-5			

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
10. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, TSSOP 4.4mm BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0108	F	1/1

封装类型	封装编码	文档编号
20 TSSOP-EP	U28E-5	21-0108

修订历史

修订次数	修订日期	说明	修改页
0	8/07	最初版本。	—
1	8/08	更新了*在自动递增模式中，写入显示存储器的步骤*部分。	39, 40

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