19-0869; Rev 2; 5/10

可提供评估板

# 完备的直接变频调谐器，用于DVB-S2系统

MAX2112

## 概述

MAX2112低成本、直接变频调谐器IC为卫星机顶盒和VSAT应用而设计。该IC适用于8PSK和数字视频广播(DVB-S2)应用。

MAX2112使用宽带I/Q下变频器直接将卫星信号从LNB变频至基带，工作频率范围扩展到925MHz至2175MHz。

该器件包含LNA、RF可变增益放大器、I和Q下变频混频器、截止频率可编程的基带低通滤波器和数控可变增益基带放大器。RF和基带可变增益放大器相配合，能够提供大于80dB的增益控制范围。该IC完全符合所有DVB-S2解调器的规范要求。

MAX2112包含完整的单片VCO和N分频频率合成器。另外，片内晶体振荡器提供缓冲输出，用于驱动额外的调谐器和解调器。通过2线串行接口实现合成器的编程和器件配置。IC能够自动选择VCO (VAS)，以自动选择适当的VCO。在多调谐器应用中，该器件可以配置为两个2线接口地址的其中之一。提供低功耗待机模式，关断信号通路，但参考时钟振荡器、数字接口和缓冲器保持有效状态，能够在单调谐器和多调谐器应用中有效降低功耗。

MAX2112是目前最先进的DBS调谐器，低噪声系数省去了外部LNA。只需少数无源器件即可构成完备的DVB-S2 RF前端方案。该调谐器提供微小的28引脚、薄型QFN封装。

## 应用

DirecTV和碟形网络DBS

DVB-S2

VSAT

## 特性

- ♦ 925MHz至2175MHz的频率范围
- ♦ 单片VCO
  - 低相位噪声：10kHz时-97dBc/Hz
  - 无需校准
- ♦ 宽动态范围：-75dBm至0dBm
- ♦ 集成带宽可调的低通滤波器：4MHz至40MHz
- ♦ +3.3V ±5%单电源供电
- ♦ 低功耗待机模式
- ♦ 用于多调谐器应用的地址引脚
- ♦ 差分I/Q接口
- ♦ $I^2C$ 2线串行接口
- ♦ 微小的28引脚、TQFN封装

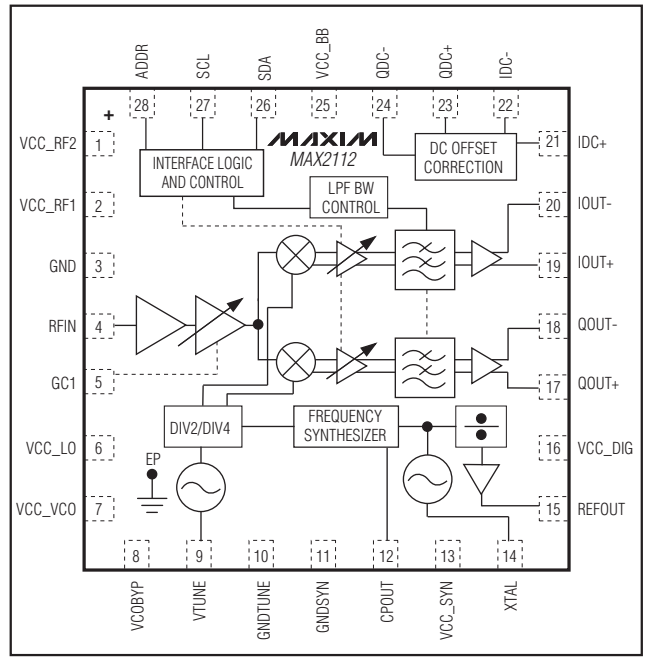
## 定购信息

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX2112CTI+ | 0°C to +70°C | 28 Thin QFN-EP* |
| MAX2112ETI+ | -40°C to +85°C | 28 Thin QFN-EP* |

*EP = 裸焊盘。*

*+表示无铅(Pb)/符合RoHS标准的封装。*

## 引脚配置/功能框图



## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND .....-0.3V to +3.9V
All Other Pins to GND .....-0.3V to ($V_{CC}$ + 0.3V)
RF Input Power: RFIN .....+10dBm
VCOBYP, CPOUT, XTAL, REFOUT, IOUT_, QOUT_ , IDC_, QDC_ to GND Short-Circuit Protection .....10s
Continuous Power Dissipation ($T_A$ = +70°C)
28-Pin Thin QFN (derated 34.5mW/°C above +70°C) ...2.75W
Operating Temperature Range (MAX2112CTI+) .....0°C to +70°C
Operating Temperature Range (MAX2112ETI+) ...-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**CAUTION!** ESD SENSITIVE DEVICE

## DC ELECTRICAL CHARACTERISTICS

(MAX2112 Evaluation Kit: $V_{CC}$ = +3.13V to +3.47V, $T_A$ = 0°C to +70°C (MAX2112CTI+), $T_A$ = -40°C to +85°C (MAX2112ETI+), $V_{GC1}$ = +0.5V (max gain), default register settings except BBG[3:0] = 1011. No input signals at RF, baseband I/Os are open circuited. Typical values measured at $V_{CC}$ = +3.3V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **SUPPLY** | | | | | |
| Supply Voltage | | 3.13 | 3.3 | 3.47 | V |
| Supply Current | Receive mode, bit STBY = 0 | | 100 | 160 | mA |
| | Standby mode, bit STBY = 1 | | 3 | | |
| **ADDRESS SELECT INPUT (ADDR)** | | | | | |
| Digital Input Voltage High, $V_{IH}$ | | 2.4 | | | V |
| Digital Input Voltage Low, $V_{IL}$ | | | | 0.5 | V |
| Digital Input Current High, $I_{IH}$ | | | | 50 | µA |
| Digital Input Current Low, $I_{IL}$ | | -50 | | | µA |
| **ANALOG GAIN-CONTROL INPUT (GC1)** | | | | | |
| Input Voltage Range | Maximum gain = 0.5V | 0.5 | | 2.7 | V |
| Input Bias Current | | -50 | | +50 | µA |
| **VCO TUNING VOLTAGE INPUT (VTUNE)** | | | | | |
| Input Voltage Range | | 0.4 | | 2.3 | V |
| **2-WIRE SERIAL INPUTS (SCL, SDA)** | | | | | |
| Clock Frequency | | | | 400 | kHz |
| Input Logic-Level High | | 0.7 x $V_{CC}$ | | | V |
| Input Logic-Level Low | | | | 0.3 x $V_{CC}$ | V |
| Input Leakage Current | Digital inputs = GND or $V_{CC}$ | | ±0.1 | ±1 | µA |
| **2-WIRE SERIAL OUTPUT (SDA)** | | | | | |
| Output Logic-Level Low | $I_{SINK}$ = 1mA | | | 0.4 | V |

## AC ELECTRICAL CHARACTERISTICS

(MAX2112 Evaluation Kit: $V_{CC}$ = +3.13V to +3.47V, $T_A$ = 0°C to +70°C (MAX2112CTI+), $T_A$ = -40°C to +85°C (MAX2112ETI+), default register settings except BBG[3:0] = 1011. Typical values measured at $V_{CC}$ = +3.3V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **MAIN SIGNAL PATH PERFORMANCE** | | | | | |
| Input Frequency Range | (Note 2) | 925 | | 2175 | MHz |
| RF Gain-Control Range (GC1) | 0.5V < $V_{GC1}$ < 2.7V | 65 | 73 | | dB |
| Baseband Gain-Control Range | Bits GC2 = 1111 to 0000 | 13 | 15 | | dB |
| In-Band Input IP3 | (Note 3) | | +2 | | dBm |
| Out-of-Band Input IP3 | (Note 4) | | +15 | | dBm |
| Input IP2 | (Note 5) | | +40 | | dBm |
| Adjacent Channel Protection | (Note 6) | | 25 | | dB |
| Noise Figure | $V_{GC1}$ is set to 0.5V (maximum RF gain) and BBG[3:0] is adjusted to give a $1V_{P-P}$ baseband output level for a -75dBm CW input tone at 1500MHz | | 8 | | dB |
| | Starting with the same BBG[3:0] setting as above, $V_{GC1}$ is adjusted to back off RF gain by 10dB (Note 7) | | 9 | 12 | |
| Minimum RF Input Return Loss | 925MHz < $f_{RF}$ < 2175MHz, in 75Ω system | | 12 | | dB |
| **BASEBAND OUTPUT CHARACTERISTICS** | | | | | |
| Nominal Output Voltage Swing | $R_{LOAD}$ = 2kΩ//10pF | 0.5 | 1 | | $V_{P-P}$ |
| I/Q Amplitude Imbalance | Measured at 500kHz; filter set to 22.27MHz | | | ±1 | dB |
| I/Q Quadrature Phase Imbalance | Measured at 500kHz; filter set to 22.27MHz | | | 3.5 | Degrees |
| Single-Ended I/Q Output Impedance | Real $Z_O$, from 1MHz to 40MHz | | 30 | | Ω |
| Output 1dB Compression Voltage | Differential | | 3 | | $V_{P-P}$ |
| Baseband Highpass -3dB Frequency Corner | 47nF capacitors at IDC_, QDC_ | | 400 | | Hz |
| **BASEBAND LOWPASS FILTERS** | | | | | |
| Filter Bandwidth Range | | 4 | | 40 | MHz |
| Rejection Ratio | At 2 x $f_{-3dB}$ | | 39 | | dB |
| Group Delay | Up to 1dB bandwidth | | 37 | | ns |
| Ratio of In-Filter-Band to Out-of-Filter-Band Noise | $f_{INBAND}$ = 100Hz to 22.5MHz, $f_{OUTBAND}$ = 87.5MHz to 112.5MHz | | 25 | | dB |
| **FREQUENCY SYNTHESIZER** | | | | | |
| RF-Divider Frequency Range | | 925 | | 2175 | MHz |
| RF-Divider Range (N) | | 19 | | 251 | |
| Reference-Divider Frequency Range | | 12 | | 30 | MHz |
| Reference-Divider Range (R) | | 1 | | 1 | |
| Phase-Detector Comparison Frequency | | 12 | | 30 | MHz |
| **VOLTAGE-CONTROLLED OSCILLATOR AND LO GENERATION** | | | | | |
| Guaranteed LO Frequency Range | | 925 | | 2175 | MHz |
| LO Phase Noise | $f_{OFFSET}$ = 10kHz | | -97 | | dBc/Hz |
| | $f_{OFFSET}$ = 100kHz | | -100 | | |
| | $f_{OFFSET}$ = 1MHz | | -122 | | |

## AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2112 Evaluation Kit: $V_{CC}$ = +3.13V to +3.47V, $T_A$ = 0°C to +70°C (MAX2112CTI+), $T_A$ = -40°C to +85°C (MAX2112ETI+), default register settings except BBG[3:0] = 1011. Typical values measured at $V_{CC}$ = +3.3V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **XTAL/REFERENCE OSCILLATOR INPUT AND OUTPUT BUFFER** | | | | | |
| XTAL Oscillator Frequency Range | Parallel-resonance-mode crystal (Note 8) | 12 | | 30 | MHz |
| Input Overdrive level | AC-coupled sine-wave input | 0.5 | 1 | 2.0 | $V_{P-P}$ |
| XTAL Output-Buffer Divider Range | | 1 | | 8 | |
| XTAL Output Voltage Swing | 4MHz to 30MHz, $C_{LOAD}$ = 10pF | 1 | 1.5 | 2 | $V_{P-P}$ |
| XTAL Output Duty Cycle | | | 50 | | % |

**Note 1:** MAX2112CTI+: Min/max values are production tested at $T_A$ = +70°C. Min/max limits at $T_A$ = 0°C and $T_A$ = +25°C are guaranteed by design and characterization.
MAX2112ETI+: Min/max values are production tested at $T_A$ = +85°C. Min/max limits at $T_A$ = -40°C and $T_A$ = +25°C are guaranteed by design and characterization.

**Note 2**: Input gain range specifications met over this band.

**Note 3**: In-band IIP3 test conditions: GC1 set to provide the nominal baseband output drive when mixing down a -23dBm tone at 2175MHz to 5MHz baseband ($f_{LO}$ = 2170MHz). Baseband gain is set to its default value (BBG[3:0] = 1011). Two tones at -26dBm each are applied at 2174MHz and 2175MHz. The IM3 tone at 3MHz is measured at baseband, but is referred to the RF input.

**Note 4**: Out-of-band IIP3 test conditions: GC1 set to provide nominal baseband output drive when mixing down a -23dBm tone at 2175MHz to 5MHz baseband ($f_{LO}$ = 2170MHz). Baseband gain is set to its default value (BBG[3:0] = 1011). Two tones at -20dBm each are applied at 2070MHz and 1975MHz. The IM3 tone at 5MHz is measured at baseband, but is referred to the RF input.

**Note 5**: Input IP2 test conditions: GC1 set to provide nominal baseband output drive when mixing down a -23dBm tone at 2175MHz to 5MHz baseband ($f_{LO}$ = 2170MHz). Baseband gain is set to its default value (BBG[3:0] = 1011). Two tones at -20dBm each are applied at 925MHz and 1250MHz. The IM2 tone at 5MHz is measured at baseband, but is referred to the RF input.

**Note 6**: Adjacent channel protection test conditions: GC1 is set to provide the nominal baseband output drive with a 2110MHz 27.5Mbaud signal at -55dBm. GC2 set for mid-scale. The test signal shall be set for PR = 7/8 and SNR of -8.5dB. An adjacent channel at ±40MHz is added at -25dBm. DVB-S BER performance of 2E-4 shall be maintained for the desired signal. GC2 may be adjusted for best performance.

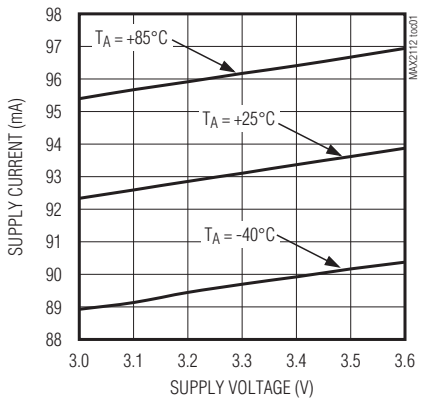
**Note 7**: Guaranteed by design and characterization at $T_A$ = +25°C.

**Note 8**: See Table 16 for crystal ESR requirements.

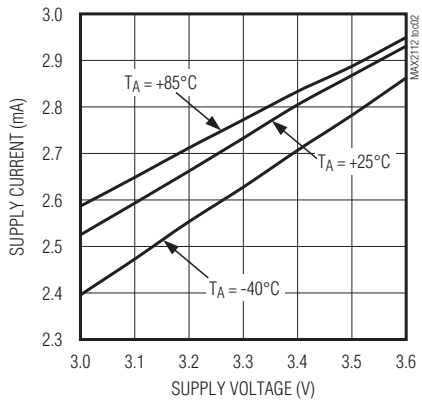
## 典型工作特性

(MAX2112 Evaluation Kit: $V_{CC}$ = +3.3V, $T_A$ = +25°C, baseband output frequency = 5MHz; $V_{GC1}$ = +1.2V, default register settings except BBG[3:0] = 1011.)

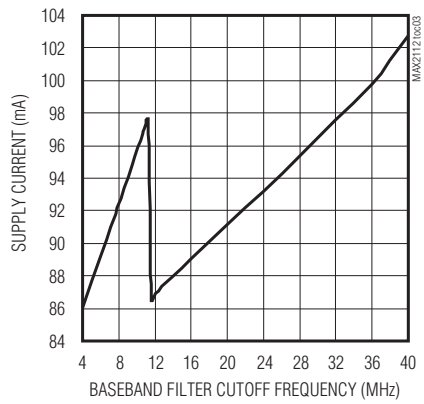
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



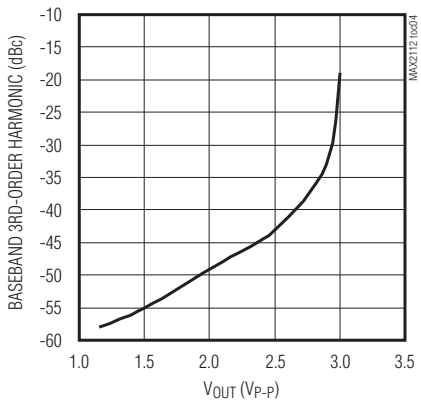

**STANDBY MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE**



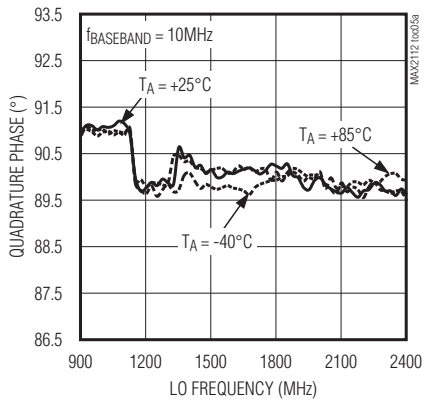

**SUPPLY CURRENT vs. BASEBAND FILTER CUTOFF FREQUENCY**



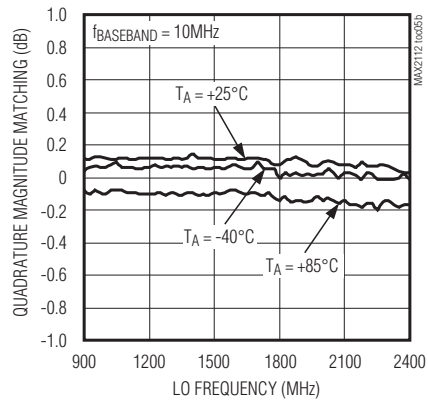

**HD3 vs. $V_{OUT}$**



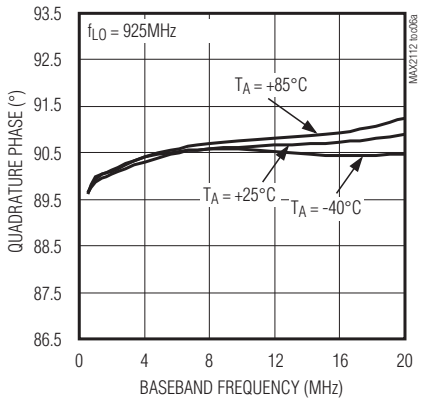

**QUADRATURE PHASE vs. LO FREQUENCY**



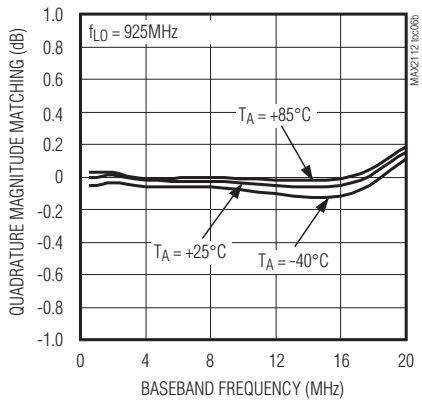

**QUADRATURE MAGNITUDE MATCHING vs. LO FREQUENCY**



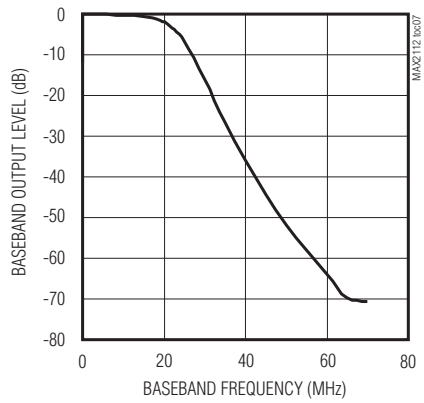

**QUADRATURE PHASE vs. BASEBAND FREQUENCY**




**QUADRATURE MAGNITUDE MATCHING vs. BASEBAND FREQUENCY**



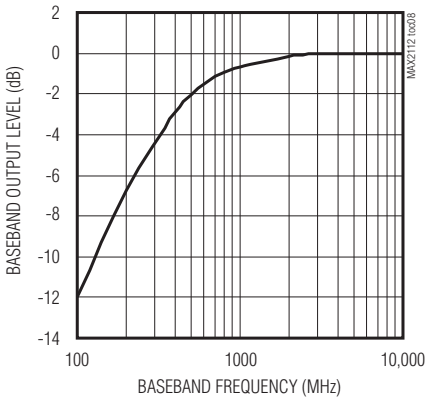

**BASEBAND FILTER FREQUENCY RESPONSE**



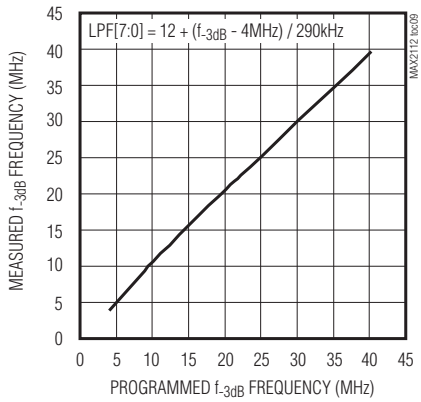
## 典型工作特性(续)

(MAX2112 Evaluation Kit: $V_{CC}$ = +3.3V, $T_A$ = +25°C, baseband output frequency = 5MHz; $V_{GC1}$ = +1.2V, default register settings except BBG[3:0] = 1011.)

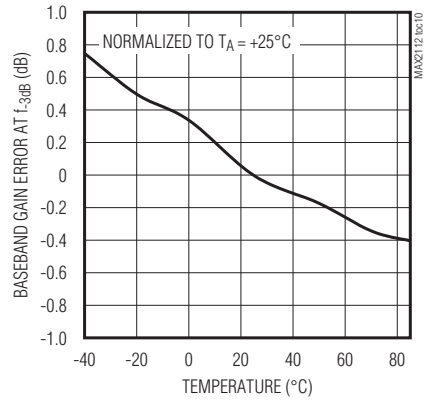
**BASEBAND FILTER HIGHPASS FREQUENCY RESPONSE**



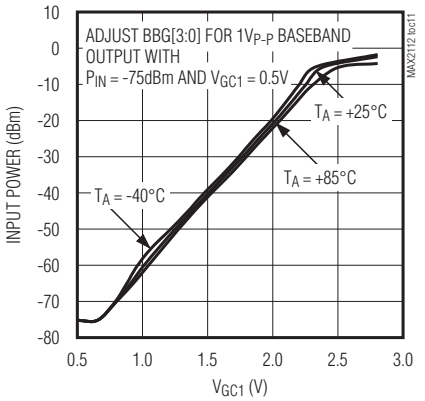

**PROGRAMMED $f_{-3dB}$ FREQUENCY vs. MEASURED $f_{-3dB}$ FREQUENCY**



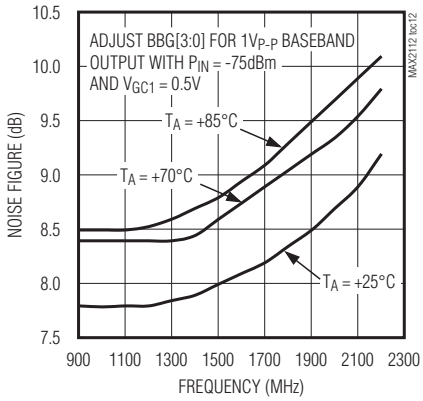

**BASEBAND FILTER 3dB FREQUENCY vs. TEMPERATURE**



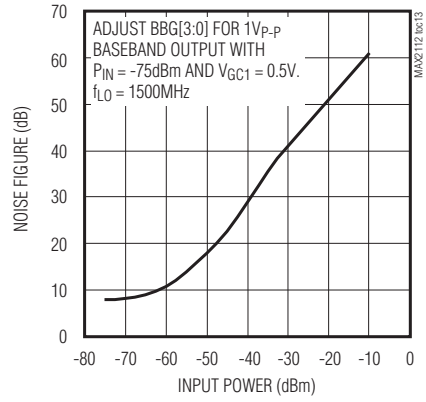

**INPUT POWER vs. $V_{GC1}$**



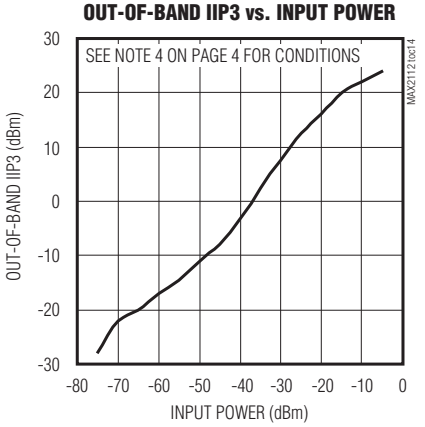

**NOISE FIGURE vs. FREQUENCY**



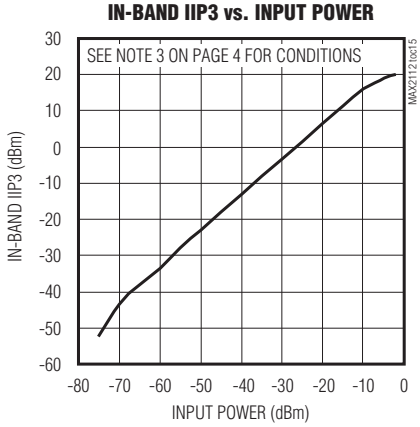

**NOISE FIGURE vs. INPUT POWER**



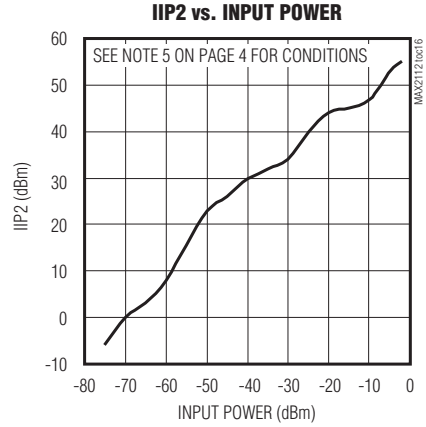

**OUT-OF-BAND IIP3 vs. INPUT POWER**




**IN-BAND IIP3 vs. INPUT POWER**



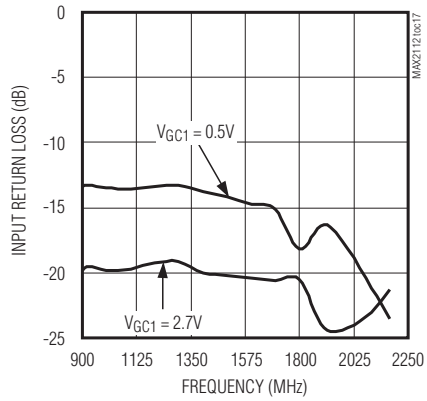

**IIP2 vs. INPUT POWER**



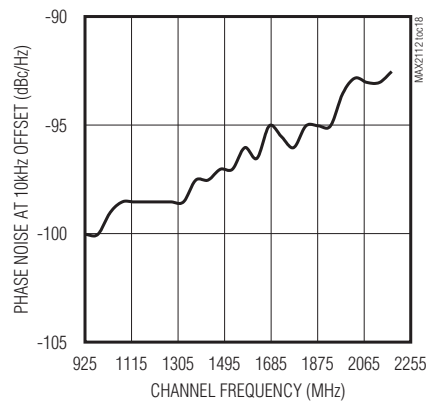
## 典型工作特性(续)

(MAX2112 Evaluation Kit: $V_{CC}$ = +3.3V, $T_A$ = +25°C, baseband output frequency = 5MHz; $V_{GC1}$ = +1.2V, default register settings except BBG[3:0] = 1011.)

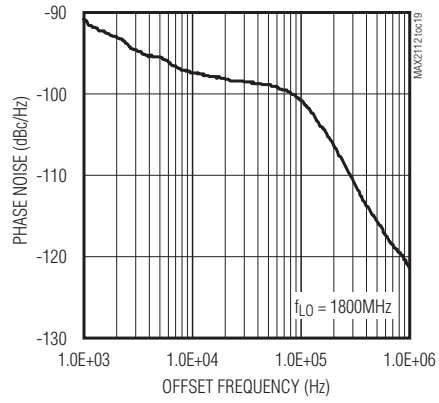
**INPUT RETURN LOSS vs. FREQUENCY**



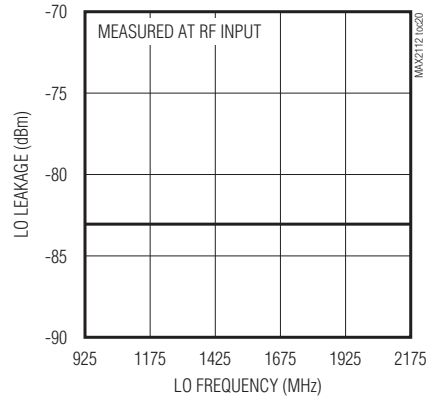

**PHASE NOISE AT 10kHz OFFSET vs. CHANNEL FREQUENCY**



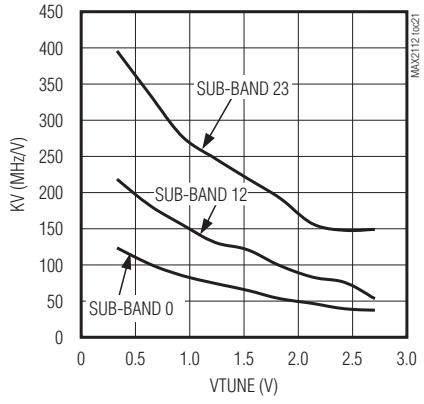

**PHASE NOISE vs. OFFSET FREQUENCY**




**LO LEAKAGE vs. LO FREQUENCY**




**VCO: KV vs. VTUNE**



## 引脚说明

| 引脚 | 名称 | 功能 |
|---|---|---|
| 1 | VCC_RF2 | LNA的直流供电电源。连接到一个+3.3V低噪声电源，在尽可能靠近该引脚的位置安装一个1nF电容，将其旁路到GND。此电容的接地过孔不能与其它接地连线共用。 |
| 2 | VCC_RF1 | LNA的直流供电电源。连接到一个+3.3V的低噪声电源，在尽可能靠近该引脚的位置安装一个1nF电容，将其旁路到GND。此电容的接地过孔不能与其它接地连线共用。 |
| 3 | GND | 地，连接到电路板的地层以保证正常工作。 |
| 4 | RFIN | 宽带75Ω RF输入，通过一个隔直流电容连接到RF信号源。 |
| 5 | GC1 | RF增益控制输入，高阻模拟输入，工作范围为0.5V至2.7V。$V_{GC1}$ = 0.5V对应于最大增益设置。 |
| 6 | VCC_LO | LO发生器的直流供电电源。连接到一个+3.3V的低噪声电源，在尽可能靠近该引脚的位置安装一个1nF电容，将其旁路到GND。此电容的接地过孔不能与其它接地连线共用。 |
| 7 | VCC_VCO | VCO电路的直流供电电源。连接到一个+3.3V的低噪声电源，在尽可能靠近该引脚的位置安装一个1nF电容，将其旁路到GND。此电容的接地过孔不能与其它接地连线共用。 |
| 8 | VCOBYP | 内部VCO偏置旁路，在尽可能靠近该引脚的位置安装一个100nF电容，将其旁路到GND。此电容的接地过孔不能与其它接地连线共用。 |
| 9 | VTUNE | VCO调谐高阻输入。直接将PLL环路滤波器输出连接到该引脚，并使连线尽可能短。 |
| 10 | GNDTUNE | VTUNE地，连接到PCB地层。 |
| 11 | GNDSYN | 频率合成器地，连接到PCB地层。 |
| 12 | CPOUT | 电荷泵输出。该输出端连接到PLL环路滤波器输入，连线要尽可能短。 |
| 13 | VCC_SYN | 频率合成器电路的直流供电电源。连接到一个+3.3V低噪声电源，在尽可能靠近该引脚的位置安装一个1nF电容，将其旁路到GND。此电容的接地过孔不能与其它接地连线共用。 |
| 14 | XTAL | 晶体振荡器连接端，连接一个外部并联谐振模式晶体与1nF电容的串联电路，请参考*典型应用电路*。 |
| 15 | REFOUT | 晶体振荡器缓冲输出。驱动外部电路时必须使用隔直流电容。 |
| 16 | VCC_DIG | 数字逻辑电路的直流供电电源。连接到一个+3.3V低噪声电源，在尽可能靠近该引脚的位置安装一个1nF电容，将其旁路到GND。此电容的接地过孔不能与其它接地连线共用。 |
| 17 | QOUT+ | 正交基带差分输出，通过一个47nF电容交流耦合到解调器输入。 |
| 18 | QOUT- | |
| 19 | IOUT+ | 同相基带差分输出，通过一个47nF电容交流耦合到解调器输入。 |
| 20 | IOUT- | |
| 21 | IDC+ | I通道基带直流失调校准，在IDC-和IDC+之间连接一个47nF陶瓷电容。 |
| 22 | IDC- | |
| 23 | QDC+ | Q通道基带直流失调校准，在QDC-和QDC+之间连接一个47nF陶瓷电容。 |
| 24 | QDC- | |
| 25 | VCC_BB | 基带电路的直流供电电源。连接到一个+3.3V低噪声电源，在尽可能靠近该引脚的位置安装一个1nF电容，将其旁路到GND。此电容的接地过孔不能与其它接地连线共用。 |

## 引脚说明(续)

| 引脚 | 名称 | 功能 |
|---|---|---|
| 26 | SDA | 2线串行数据接口，需要一个≥ 1kΩ电阻上拉到$V_{CC}$。 |
| 27 | SCL | 2线串行时钟接口，需要一个≥ 1kΩ电阻上拉到$V_{CC}$。 |
| 28 | ADDR | 地址，必须连接至地(逻辑0)或电源(逻辑1)。 |
| — | EP | 裸焊盘，均匀地焊接到电路板的地层，以保证正常工作。 |

## 详细说明

### 寄存器说明

MAX2112包括12个用户可配置的寄存器和2个只读寄存器。寄存器配置如表1所示。表1列出了所有寄存器配置，给出了每一位的名称和该位的使用信息。注意：所有寄存器必须在器件上电100µs之后(不得早于)才能被写入。

**表1. 寄存器配置**

| REG NUMBER | REGISTER NAME | READ/ WRITE | REG ADDRESS | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | DATA BYTE | | | | | | | |
| | | | | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| 1 | N-Divider MSB | Write | 0x00 | FRAC 1 | N[14] | N[13] | N[12] | N[11] | N[10] | N[9] | N[8] |
| 2 | N-Divider LSB | Write | 0x01 | N[7] | N[6] | N[5] | N[4] | N[3] | N[2] | N[1] | N[0] |
| 3 | Charge Pump | Write | 0x02 | CPMP[1] 0 | CPMP[0] 0 | CPLIN[1] 0 | CPLIN[0] 1 | F[19] | F[18] | F[17] | F[16] |
| 4 | F-Divider MSB | Write | 0x03 | F[15] | F[14] | F[13] | F[12] | F[11] | F[10] | F[9] | F[8] |
| 5 | F-Divider LSB | Write | 0x04 | F[7] | F[6] | F[5] | F[4] | F[3] | F[2] | F[1] | F[0] |
| 6 | XTAL Divider R-Divider | Write | 0x05 | XD[2] | XD[1] | XD[0] | R[4] | R[3] | R[2] | R[1] | R[0] |
| 7 | PLL | Write | 0x06 | D24 | CPS | ICP | X | X | X | X | X |
| 8 | VCO | Write | 0x07 | VCO[4] | VCO[3] | VCO[2] | VCO[1] | VCO[0] | VAS | ADL | ADE |
| 9 | LPF | Write | 0x08 | LPF[7] | LPF[6] | LPF[5] | LPF[4] | LPF[3] | LPF[2] | LPF[1] | LPF[0] |
| 10 | Control | Write | 0x09 | STBY | X | PWDN 0 | X | BBG[3] | BBG[2] | BBG[1] | BBG[0] |
| 11 | Shutdown | Write | 0x0A | X | PLL 0 | DIV 0 | VCO 0 | BB 0 | RFMIX 0 | RFVGA 0 | FE 0 |
| 12 | Test | Write | 0x0B | CPTST[2] 0 | CPTST[1] 0 | CPTST[0] 0 | X | TURBO 1 | LD MUX[2] 0 | LD MUX[1] 0 | LD MUX[0] 0 |
| 13 | Status Byte-1 | Read | 0x0C | POR | VASA | VASE | LD | X | X | X | X |
| 14 | Status Byte-2 | Read | 0x0D | VCOSBR[4] | VCOSBR[3] | VCOSBR[2] | VCOSBR[1] | VCOSBR[0] | ADC[2] | ADC[1] | ADC[0] |

*X = 无关。* *0 = 设置为“0”，用于工厂测试。* *1 = 设置为“1”，用于工厂测试。*

表2. N分频器MSB寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| FRAC | 7 | 1 | Users must program to 1 upon powering up the device. |
| N[14:8] | 6–0 | 0000000 | Sets the most significant bits of the PLL integer-divide number (N). N can range from 19 to 251. |

表3. N分频器LSB寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| N[7:0] | 7–0 | 00100011 | Sets the least significant bits of the PLL integer-divide number. N can range from 19 to 251. |

表4. 电荷泵寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| CPMP[1:0] | 7–6 | 00 | Charge-pump minimum pulse width. Users must program to 00 upon powering up the device. |
| CPLIN[1:0] | 5–4 | 00 | Controls charge-pump linearity. Users must program to 01 upon powering up the device. |
| F[19:16] | 3–0 | 0010 | Sets the 4 most significant bits of the PLL fractional divide number.<br>Default value is F = 194,180 decimal. |

表5. F分频器MSB寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| F[15:8] | 7–0 | 11110110 | Sets the most significant bits of the PLL fractional-divide number (F).<br>Default value is F = 194,180 decimal. |

表6. F分频器LSB寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| F[7:0] | 7–0 | 10000100 | Sets the least significant bits of the PLL fractional-divide number (F).<br>Default value is F = 194,180 decimal. |

表7. XTAL缓冲器和参考时钟分频寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| XD[2:0] | 7–5 | 000 | Sets the crystal-divider setting.<br>000 = Divide by 1.<br>001 = Divide by 2.<br>011 = Divide by 3.<br>100 = Divide by 4.<br>101 through 110 = All divide values from 5 (101) to 7 (110).<br>111 = Divide by 8. |
| R[4:0] | 4–0 | 00001 | Sets the PLL reference-divider (R) number. Users must program to 00001 upon powering up the device.<br>00001 = Divide by 1; other values are not tested. |

表8. PLL寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| D24 | 7 | 1 | VCO divider setting.<br>0 = Divide by 2. Use for LO frequencies ≥ 1125MHz.<br>1 = Divide by 4. Use for LO frequencies < 1125MHz. |
| CPS | 6 | 1 | Charge-pump current mode.<br>0 = Charge-pump current controlled by ICP bit.<br>1 = Charge-pump current controlled by VCO autoselect (VAS). |
| ICP | 5 | 0 | Charge-pump current.<br>0 = 600µA typical.<br>1 = 1200µA typical. |
| X | 4–0 | X | Don't care. |

表9. VCO寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| VCO[4:0] | 7–3 | 11001 | Controls which VCO is activated when using manual VCO programming mode. This also serves as the starting point for the VCO autoselection (VAS) mode. |
| VAS | 2 | 1 | VCO autoselection (VAS) circuit.<br>0 = Disable VCO selection must be programmed through $I^2C$.<br>1 = Enable VCO selection controlled by autoselection circuit. |
| ADL | 1 | 0 | Enables or disables the VCO tuning voltage ADC latch when the VCO autoselect mode (VAS) is disabled.<br>0 = Disables the ADC latch.<br>1 = Latches the ADC value. |
| ADE | 0 | 0 | Enables or disables VCO tuning voltage ADC read when the VCO autoselect mode (VAS) is disabled.<br>0 = Disables ADC read.<br>1 = Enables ADC read. |

表10. 低通滤波器寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| LPF[7:0] | 7–0 | 01001011 | Sets the baseband lowpass filter 3dB corner frequency.<br>$f_{-3dB}$ = 4MHz + $(LPF[7:0]_{dec}$ - 12) x 290kHz.<br>Default value equates to $f_{-3dB}$ = 22.27MHz typical. |

表11. 控制寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| STBY | 7 | 0 | Software standby control.<br>0 = Normal operation.<br>1 = Disables the signal path and frequency synthesizer leaving only the 2-wire bus, crystal oscillator, XTALOUT buffer, and XTALOUT buffer divider active. |
| X | 6 | X | Don't care. |
| PWDN | 5 | 0 | Factory use only.<br>0 = Normal operation;<br>other value is not tested. |
| X | 4 | X | Don't care. |
| BBG[3:0] | 3-0 | 0000 | Baseband gain setting (1dB typical per step).<br>0000 = Minimum gain (0dB, default).<br>…<br>1111 = Maximum gain (15dB typical). |

表12. 关断寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| X | 7 | X | Don't care. |
| PLL | 6 | 0 | PLL enable.<br>0 = Normal operation.<br>1 = Shuts down the PLL. Value not tested. |
| DIV | 5 | 0 | Divider enable.<br>0 = Normal operation.<br>1 = Shuts down the divider. Value not tested. |
| VCO | 4 | 0 | VCO enable.<br>0 = Normal operation.<br>1 = Shuts down the VCO. Value not tested. |
| BB | 3 | 0 | Baseband enable.<br>0 = Normal operation.<br>1 = Shuts down the baseband. Value not tested. |
| RFMIX | 2 | 0 | RF mixer enable.<br>0 = Normal operation.<br>1 = Shuts down the RF mixer. Value not tested. |
| RFVGA | 1 | 0 | RF VGA enable.<br>0 = Normal operation.<br>1 = Shuts down the RF VGA. Value not tested. |
| FE | 0 | 0 | Front-end enable.<br>0 = Normal operation.<br>1 = Shuts down the front-end. Value not tested. |

表13. 测试寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| CPTST[2:0] | 7–5 | 000 | Charge-pump test modes.<br>000 = Normal operation (default). |
| X | 4 | X | Don't care. |
| TURBO | 3 | 0 | Charge-pump fast lock.<br>Users must program to 1 after powering up the device. |
| LDMUX[2:0] | 2–0 | 000 | REFOUT output.<br>000 = Normal operation. Other values are not tested. |

表14. 状态字节1寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | FUNCTION |
|---|---|---|
| POR | 7 | Power-on reset status.<br>0 = Chip status register has been read with a stop condition since last power-on.<br>1 = Power-on reset (power cycle) has occurred. Default values have been loaded in registers. |
| VASA | 6 | Indicates whether VCO autoselection was successful.<br>0 = Indicates the autoselect function is disabled or unsuccessful VCO selection.<br>1 = Indicates successful VCO autoselection. |
| VASE | 5 | Status indicator for the autoselect function.<br>0 = Indicates the autoselect function is active.<br>1 = Indicates the autoselect process is inactive. |
| LD | 4 | PLL lock detector. TURBO bit must be programmed to 1 for valid LD reading.<br>0 = Unlocked.<br>1 = Locked. |
| X | 3:0 | Don't care. |

表15. 状态字节2寄存器

| BIT NAME | BIT LOCATION (0 = LSB) | FUNCTION |
|---|---|---|
| VCOSBR[4:0] | 7-3 | VCO band readback. |
| ADC[2:0] | 2-0 | VAS ADC output readback.<br>000 = Out of lock.<br>001 = Locked.<br>010 = VAS locked.<br>101 = VAS locked.<br>110 = Locked.<br>111 = Out of lock. |

# 完备的直接变频调谐器，用于DVB-S2系统

### 2线串行接口

MAX2112采用2线I²C兼容串行接口，由串行数据线(SDA)和串行时钟线(SCL)组成。SDA和SCL能够以高达400kHz的时钟频率方便地实现MAX2112与主控制器之间的双向通信。主控制器启动总线数据的传输，产生SCL信号进行数据传输。MAX2112只能作为从器件，能够将数据发送到主控制器并接收来自主控制器的数据。为了进行正常的总线通信，SDA和SCL必须通过外部电阻(1kΩ或更大的)拉高。上拉电阻应当以MAX2112的$V_{CC}$为参考。

每个SCL时钟周期传输1位数据，MAX2112输入或输出1个字节至少需要9个时钟周期(8位数据和1位ACK/NACK)。SCL时钟脉冲为高电平期间SDA数据必须保持稳定。当SCL为高并保持稳定时，SDA的变化被认为是控制信号(请参考*START和STOP条件*部分)。总线不忙时，SDA和SCL都保持高电平。

### START和STOP条件

主控制器通过START条件(S)启动一次传输，SCL为高电平时SDA从高电平跳变为低电平即产生一个START条件。主控制器以STOP条件(P)终止传输，SCL为高电平时SDA从低电平跳变为高电平即产生一个STOP条件。

### 应答和非应答条件

数据传输帧中带有一个应答位(ACK)或一个非应答位(NACK)。主控制器和MAX2112 (从器件)都会产生应答位，为了产生应答信号，接收器件必须在对应的应答脉冲(第9个脉冲)的上升沿之前将SDA拉低，并使其在时钟的高电平期间保持低电平。

为了产生非应答信号，接收器件在对应的应答脉冲的上升沿之前将SDA拉高，并且在时钟脉冲的高电平期间保持SDA为高电平。监测应答位可以检测到失败的数据传输。在接收器件忙或系统发生故障时可能导致数据传输失败。数据传输失败时，总线主控制器必须在稍后重新尝试通信。

### 从地址

MAX2112具有7位从地址，该地址在START条件后发送以启动通信。从地址由内部设置为1100000。7位地址之后的第8位(R/$\overline{W}$)决定进行读操作还是写操作。

MAX2112连续等待START条件，从地址紧随START条件之后。当器件识别到其从地址后，会将SDA拉低一个时钟周期进行应答；然后根据R/$\overline{W}$位的状态准备接收或发送数据(图1)。

ADDR引脚接地，则写/读地址为C0/C1；ADDR引脚接$V_{CC}$，则写/读地址为C2/C3。

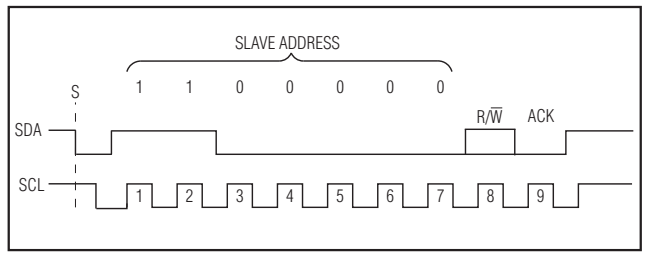



*图1. ADDR引脚接地时的MAX2112从地址字节*

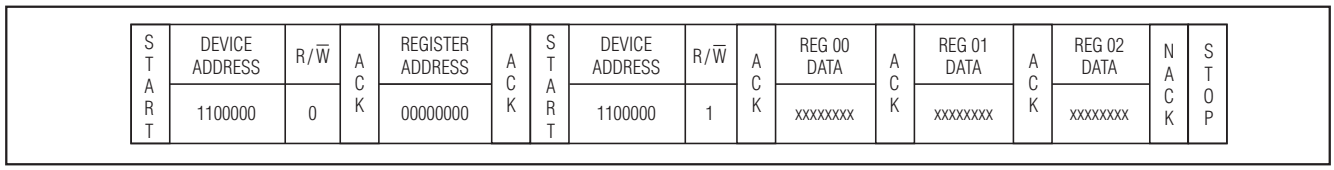
### 写周期

接收到写命令后，MAX2112允许主控制器对一个寄存器进行写操作或对多个连续的寄存器进行写操作。

总线主控制器发出START条件，并随后发送7位从地址和写控制位(R/$\overline{W}$ = 0)，开始一次写操作。MAX2112在成功接收到从地址字节后发出ACK。然后，总线主控器必须将所要写入的第一个寄存器的地址发送给从器件(参考表1的寄存器地址)。如果从器件应答了该地址，主控制器可以将一个字节写入到该地址指定的寄存器。数据从最高有效位开始写入。如果数据被成功写入寄存器，MAX2112会再次发出ACK。主控制器可以在MAX2112每次应答成功的传输后连续地将数据写入到内部寄存器，也可以产生STOP条件终止传输。在主控制器产生STOP条件后终止写操作。

| START | WRITE DEVICE ADDRESS | R/$\overline{W}$ | ACK | WRITE REGISTER ADDRESS | ACK | WRITE DATA TO REGISTER 0x00 | ACK | WRITE DATA TO REGISTER 0x01 | ACK | WRITE DATA TO REGISTER 0x02 | ACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1100000 | 0 | — | 0x00 | — | 0x0E | — | 0xD8 | — | 0xE1 | — | |

*图2. 例子：将0x0E、0xD8和0xE1分别写入寄存器0–2*



| START | DEVICE ADDRESS | R/W | ACK | REGISTER ADDRESS | ACK | START | DEVICE ADDRESS | R/W | ACK | REG 00 DATA | ACK | REG 01 DATA | ACK | REG 02 DATA | NACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1100000 | 0 | | 00000000 | | | 1100000 | 1 | | xxxxxxxx | | xxxxxxxx | | xxxxxxxx | | |

*图3. 例子：从读寄存器接收数据*

### *读周期*

接收到读命令后，MAX2112允许主控制器对一个或多个连续的寄存器进行读操作。

总线主控制器发出START条件，并随后传输7位从地址和1位写控制位(R/$\overline{W}$ = 0)，开启一次读操作。MAX2112在成功接收到从地址字节后发出ACK。然后总线主控制器须发送需要读取的第一个寄存器的地址(寄存器地址参见表1)，从机对该地址进行应答。接着总线主控制器发出START条件，并随后传输7位从地址和1位读控制位(R/$\overline{W}$ = 1)。MAX2112在成功接收到从地址字节后发出ACK。接下来MAX2112开始在每个SCL时钟周期发送数据，MSB在前。在第9个时钟周期，主控制器可以发出ACK以继续读取连续的寄存器，或者可以发出NACK以终止传输。读周期只有在主控制器发出STOP条件后才会结束。

图3给出了从寄存器0至2读取数据的示例。

## *应用信息*

MAX2112能够将925MHz至2175MHz范围的RF信号直接下变频到基带I/Q信号。该器件可理想用于数字DBS调谐器。

### *RF输入*

MAX2112的RF输入由内部匹配到75Ω，外部只需要一个隔直流电容，请参考*典型应用电路*。

### *RF增益控制*

MAX2112具有一个可变增益低噪声放大器，提供73dB的RF增益调节范围。电压控制(VGC)信号的范围是0.5V (最小衰减)到2.7V (最大衰减)。

### *基带可变增益放大器*

接收机基带可变增益放大器能够提供15dB的可编程增益范围，步长1dB。该VGA增益可通过SPI接口设置控制寄存器的BBG[3:0]位进行配置。

**表16. 晶体ESR的最大值要求**

| $ESR_{MAX}$ (Ω) | XTAL FREQUENCY (MHz) |
|---|---|
| 80 | $12 < f_{XTAL} \le 14$ |
| 60 | $14 < f_{XTAL} \le 30$ |

### *基带低通滤波器*

MAX2112内置一个可编程7阶巴特沃斯滤波器，滤波器的-3dB角频率通过低通滤波器寄存器的LPF[7:0]位进行配置，范围为4MHz到40MHz。LPF[7:0]的数值是由以下公式确定：

$$LPF[7:0]_{dec} = (f_{-3dB} - 4MHz)/0.29MHz + 12,$$

其中$f_{-3dB}$的单位为MHz。

器件的总电源电流与滤波器的带宽设置有关，请参考*典型工作特性*中的Supply Current vs. Baseband Filter Cutoff Frequency曲线。

### *直流失调抑制*

为了保证I/Q输出的动态范围需要消除直流失调电压。在IDC+和IDC-之间连接一个外部电容，构成I通道的高通滤波器；在QDC+和QDC-之间连接一个电容，构成Q通道的高通滤波器。选择小于47nF的外部电容，组成一个角频率为250Hz的典型高通滤波器。

### *XTAL振荡器*

MAX2112包含内部参考时钟振荡器，作为输出分频器和输出缓冲器的参考时钟。外部只需要一个1nF电容与晶体的串联电路。将晶体与串联电容尽可能靠近引脚14 (XTAL引脚)放置，以最大程度地减小寄生效应。关于晶体(XTAL)的ESR (等效串联电阻)要求，请参见表16。

### *VCO自动选择(VAS)*

MAX2112包括24个VCO，本振频率可通过配置VCO寄存器的VCO[4:0]位手动选择。VCO选择可以从状态字节2寄存器读取(参考表15)。

# 完备的直接变频调谐器，用于DVB-S2系统

MAX2112也可以通过将VCO寄存器的VAS位置位自动选择VCO。一旦写入F分频器LSB寄存器字(REG 5)，VAS流程将自动开启。

**如果只改变N分频器寄存器或F分频器的MSB字，那么F分频器的LSB字也必须在最后装载，以启动VCO自动选择功能**。在寄存器的VCO[4:0]中写入VCO值，将其作为VCO自动选择的起点。

选择过程中，状态字节1寄存器的VASE位清零，表明自动选择功能已经生效。成功完成操作后，VASE和VASA位被置位，所选择的VCO可以从状态字节2寄存器读取(参考表15)。如果搜索失败，VASA将被清零，而VASE被置位。这表明搜索已经结束但没有发现合适的VCO，这种情况通常发生在试图将频率调谐到VCO指定频率范围以外的条件下。

详细信息请参考关于MAX2112/MAX2120 VCO自动选择(VAS)的应用笔记。

### 3位ADC

MAX2112内部带有一个3位ADC，连接到VCO的调谐引脚(VTUNE)。这个ADC可用来检查VCO的锁定状态。

表17概括了ADC的跳变点和VCO锁定指示。VCO自动选择程序在“VAS锁定”范围内选择一个VCO，从而为VCO留出了一定的温漂余量，并保持一个有效的“锁定”范围。

ADC必须首先通过设置VCO寄存器的ADE位使能，通过对ADC锁定位编程(ADL = 1)锁存ADC读数。ADC数值可以从状态字节2寄存器读取(参考表15)。

### 待机模式

MAX2112可通过$I^2C$接口设置正常工作模式和待机模式。将控制寄存器的STBY置位，使器件进入待机模式。这种模式下只有2线总线、晶体振荡器、XTAL缓冲器和XTAL缓冲分频器处于工作状态。

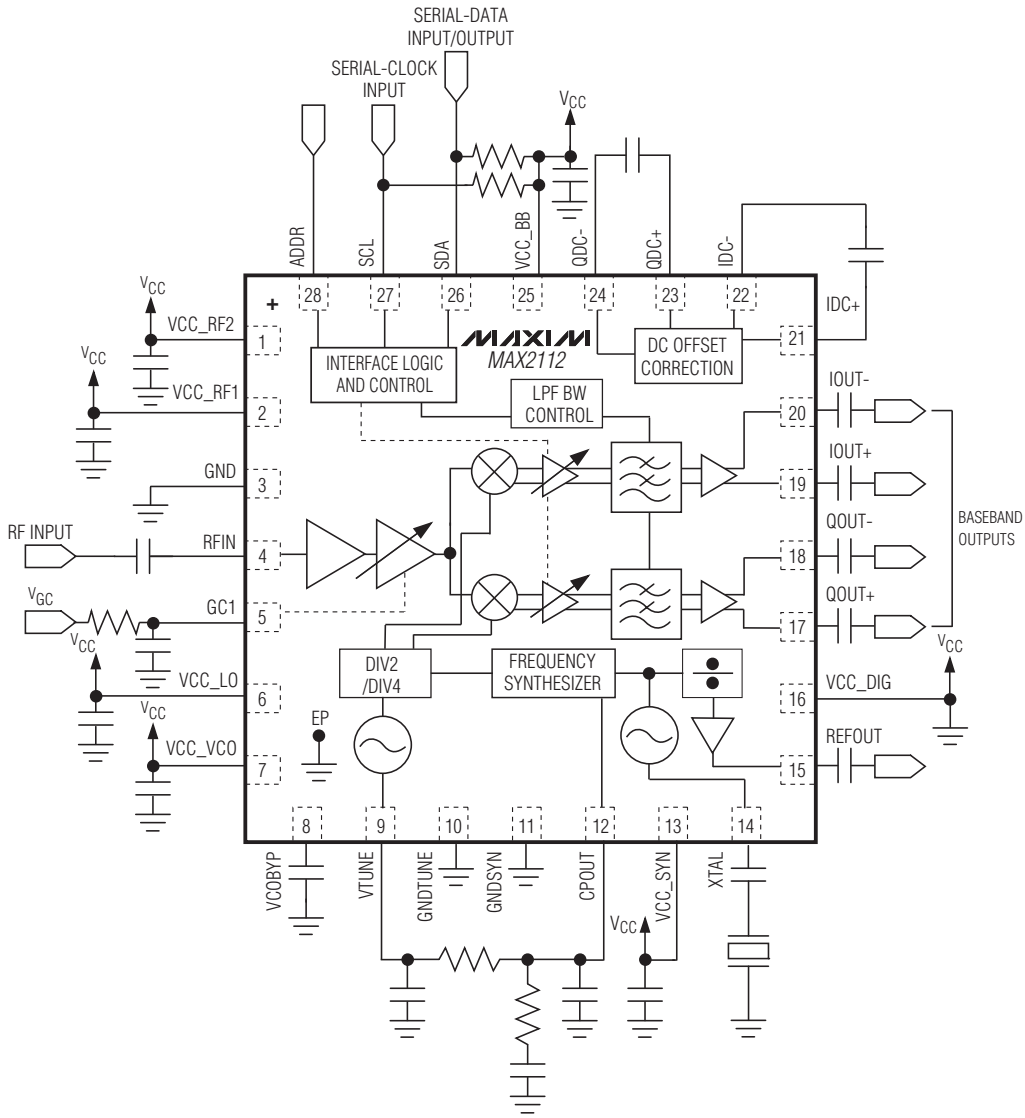
任何情况下，器件在进入关断模式之前都需要保存寄存器设置，以便在器件恢复后进入有效模式。所提供的寄存器缺省设置只是为了方便用户的使用，用户在器件上电100µs后可以配置所有寄存器。

### 布板考虑

MAX2112评估板提供了一个PCB布局参考。RF信号线要尽可能短，以减小损耗和辐射。所有高频引线须使用受控阻抗。为了保证正常工作，裸焊盘必须均匀地焊接到电路板的地层。裸焊盘下方使用大量过孔可以达到最佳的散热效果。在RF引线之间采用多个接地过孔，可以降低干扰信号的耦合。每个$V_{CC}$引脚都需要在尽可能靠近引脚的位置安装一个1nF的旁路电容。

## 表17. ADC跳变点和锁定状态

| ADC[2:0] | LOCK STATUS |
|---|---|
| 000 | Out of lock |
| 001 | Locked |
| 010 | VAS locked |
| 101 | VAS locked |
| 110 | Locked |
| 111 | Out of lock |


SERIAL-DATA
INPUT/OUTPUT
SERIAL-CLOCK
INPUT
VCC
ADDR
SCL
SDA
VCC_BB
QDC-
QDC+
IDC-
IDC+
28
27
26
25
24
23
22
21
MAXIM
MAX2112
INTERFACE LOGIC
AND CONTROL
DC OFFSET
CORRECTION
LPF BW
CONTROL
VCC_RF2
VCC_RF1
GND
RF INPUT
RFIN
VGC
GC1
VCC_LO
VCC_VCO
1
2
3
4
5
6
7
IOUT-
IOUT+
QOUT-
QOUT+
BASEBAND
OUTPUTS
20
19
18
17
DIV2
/DIV4
FREQUENCY
SYNTHESIZER
VCC_DIG
REFOUT
16
15
EP
8
9
10
11
12
13
14
VCOBYP
VTUNE
GNDTUNE
GNDSYN
CPOUT
VCC_SYN
XTAL

# 完备的直接变频调谐器，用于DVB-S2系统

## 芯片信息

PROCESS: BiCMOS

## 封装信息

如需最近的封装外形信息和焊盘布局，请查询 **china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

| 封装类型 | 封装编码 | 外形编号 | 焊盘布局编号 |
|---|---|---|---|
| 28 TQFN-EP | T2855+3 | **21-0140** | **90-0023** |

## 修订历史

| 修订号 | 修订日期 | 说明 | 修改页 |
|---|---|---|---|
| 0 | 8/07 | 最初版本。 | — |
| 1 | 12/07 | 修正了数据资料中的错误。 | 1–7, 9–16 |
| 2 | 5/10 | 更正了表8和表10的FUNCTION栏中的错误，更正了*基带低通滤波器*部分中的公式。 | 11, 15 |