19-4570; Rev 1; 10/09

MAXIM

8通道超声前端，提供CW多普勒混频器

概述

MAX2078八通道超声前端是完全集成的双极型、高密度、八通道超声接收器，优化用于低成本、多通道、高性能便携及车载超声系统。这款易于使用的IC允许用户以较小的空间和功耗实现高端2D、PW以及CW多普勒(CWD)成像。结构紧凑的成像接收机包括低噪声放大器(LNA)、可变增益放大器(VGA)和抗混叠滤波器(AAF)，$R_S = R_{IN}$ = 200Ω时具有2.4dB超低噪声系数，每通道功耗仅为64.8mW。完备的超声成像接收通道针对二次谐波成像进行优化，输出信号为$1V_{P-P}$ 5MHz时，二次谐波失真为-64dBFS。双极型超声前端经过优化，可以获得优异的低速PW和流体多普勒彩超检测灵敏度，并在5MHz $1V_{P-P}$杂波输出、1kHz频偏下，具有140dBc/Hz的近载波SNR。

器件完全集成了高性能、可编程CWD波束成形器。在强杂波环境下，每个通道独立的I/Q混频器可以对CWD灵敏度进行优化，在1.25MHz $200mV_{P-P}$输入杂波信号、1kHz频偏时，具有154dBc/Hz的近载波SNR。

MAX2078八通道超声前端采用带有裸焊盘的小尺寸10mm x 10mm、68引脚薄型QFN封装，工作温度范围为0°C至+70°C。

特性

- 小尺寸10mm x 10mm TQFN封装内集成了8通道LNA、VGA、AAF以及CWD混频器
- 与带有LNA、VGA和AAF、采用10mm x 10mm TQFN封装的MAX2077引脚兼容
- $R_{IN} = R_S$ = 200Ω时具有2.4dB超低通道噪声系数
- 5MHz、20dB增益下具有23nV/√Hz低输出参考噪声，68dB**宽带SNR，提供极佳的二次谐波成像
- 5MHz、$1V_{P-P}$输出信号、1kHz频偏，增益为20dB时，具有140dBc/Hz的近载波SNR，强杂波环境下能够提供出色的低速PW和流体多普勒彩超灵敏度
- 常规成像模式下，每通道(LNA、VGA以及AAF)具有64.8mW超低功耗(CWD模式下每通道功耗为234mW)
- 可选择有源输入阻抗匹配：50Ω、100Ω、200Ω和1kΩ
- 较宽的输入电压范围：高LNA增益模式下为$330mV_{P-P}$、低LNA增益模式下为$550mV_{P-P}$
- 集成可选择的3极点9MHz、10MHz、15MHz及18MHz巴特沃斯AAF
- 快速恢复、低功耗模式(< 2µs)
- 集成了高动态范围的CWD波束成形器，在1.25MHz、200mV$_{P-P}$输入杂波信号、1kHz频偏时，具有154dBc/Hz的近载波SNR

***配合MAX1437B ADC使用。*

应用

医疗超声成像

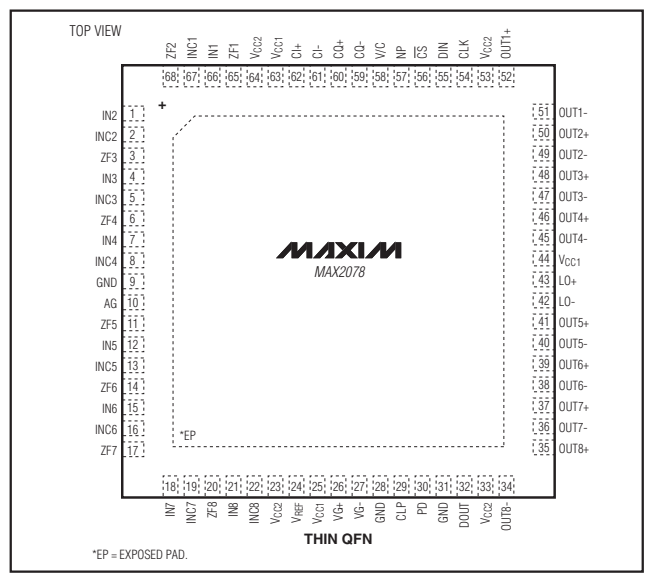
声纳系统

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX2078CTK+	0°C to +70°C	68 Thin QFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*

引脚配置



8通道超声前端，提供CW多普勒混频器

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to GND .....-0.3V to +5.5V
V_{CC2} - V_{CC1} .....> -0.3V
CI_, CQ_ to GND .....-0.3V to +13V
ZF_, IN_, AG to GND .....-0.3V to ($V_{CC\_}$ + 0.3V)
INC_ .....20mA DC
V_{REF} to GND .....-0.3V to +3V
IN_ to AG .....-0.6V to +0.6V
OUT_, LO_, DIN, DOUT, VG_, NP, $\overline{CS}$, CLK, PD, CLP, V/C to GND .....-0.3V to V_{CC1} + 0.3V
CI_, CQ_, $V_{CC\_}$, V_{REF} analog and digital control signals must be applied in this order
Input Differential Voltage .....2.0V_{P-P} differential
Continuous Power Dissipation (T_A = +70°C)
68-Pin TQFN (derated 40mW/°C above +70°C) 4W
Operating Temperature Range (Note 1) .....0°C to +70°C
Junction Temperature .....+150°C
θ_{JC} (Notes 2, 3) .....+0.3°C/W
θ_{JA} (Notes 2, 4) .....+20°C/W
Storage Temperature Range .....-40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Note 2: Junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can only be used if the component is soldered down to a printed circuit board pad containing multiple ground vias to remove the heat. The junction temperature must not exceed 150°C.

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maxim-ic.com/thermal-tutorial**.

Note 4: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$, assuming there is no heat removal from the exposed pad. The junction temperature must not exceed 150°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, CLP = 0, PD = 0, no RF signals applied. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage	V_{CC1}		3.13	3.3	3.47	V
4.75V/5V Supply Voltage	V_{CC2}		4.5	4.75	5.25	V
External Reference Voltage Range	V_{REF}	(Note 6)	2.475		2.525	V
CMOS Input High Voltage	V_{IH}	Applies to CMOS control inputs	2.5			V
CMOS Input Low Voltage	V_{IL}	Applies to CMOS control inputs			0.8	V
CMOS Input Leakage Current	I_{IN}	T_A = +25°C, applies to CMOS control inputs; 0 to 3.47V			10	µA
DATA Output High Voltage	DOUT_HI	10MΩ load		V_{CC1}		V
DATA Output Low Voltage	DOUT_LO	10MΩ load		0		V

DC ELECTRICAL CHARACTERISTICS—VGA MODE

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, V/C = 1, CLP = 0, PD = 0, no RF signals applied. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
4.75V/5V Supply Standby Current	I_NP_5V_TOT	NP = 1, all channels		3.9	6	mA
3V Supply Standby Current	I_NP_3V_TOT	NP = 1, all channels		1.7	3	mA
4.75V/5V Power-Down Current	I_PD_5V_TOT	PD = 1, all channels		0.4	10	µA
3V Power-Down Current	I_PD_3V_TOT	PD = V_{CC1}, all channels		0.3	10	µA
3V Supply Current per Channel	I_3V_NM	Total I divided by 8, VG+ - VG- = -2V		11	16	mA
4.75V/5V Supply Current per Channel	I_5V_NM	Total I divided by 8		6.0	8.3	mA
DC Power per Channel	P_NM			64.8	92.3	mW

DC ELECTRICAL CHARACTERISTICS—VGA MODE (continued)

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, V/C = 1, CLP = 0, PD = 0, no RF signals applied. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Analog Control Voltage Range	VGAIN_RANG	VG+ - VG-		±3		V
Common-Mode Voltage for Difference Analog Control	VGAIN_COMM	(VG+ + VG-)/2		1.65 ±5%		V
Source/Sink Current for Gain Control Pins	I_ACONTROL	Per pin		±1.6	±2.3	µA
Reference Voltage Input	V_{REF}		2.475		2.525	V
Reference Current	I_{REF}	All channels		9.7	13	µA
Output Common-Mode Level	V_{CMO}			1.73		V

DC ELECTRICAL CHARACTERISTICS—CW MODE

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, CLP = 0, V/C = 0, no RF signals applied. CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Current	I_{REF}			82.7		µA
Mixer LVDS LO Input Common-Mode Voltage	V_LVDS_CM	LO+ and LO-		1.25 ±0.2		V
LVDS LO Differential Input Voltage	V_LVDS_DM	Common-mode input voltage = 1.25V (Note 7)	200	700		mV_{P-P}
LVDS LO Input Common-Mode Current	I_LVDS_CM	Current out of each pin, V_LVDS_CM = 1.25V		130		µA
LVDS LO Differential Input Resistance	R_DM_LVDS	(Note 8)	4			kΩ
POWER-DOWN MODE						
4.75V/5V Supply Current per Channel	I_C_5V_P	PD = 1		0.6	10	µA
3.3V Supply Current per Channel	I_C_3_3V_P	PD = 1		0.1	10	µA
LOW-POWER MODE						
4.75V/5V Supply Current per Channel	I_C_5V_L	CLP = 1		27	30	mA
3.3V Supply Current per Channel	I_C_3_3V_L	CLP = 1		0.4	0.95	mA
11V Supply Current per Channel	I_C_11V_L	CLP = 1		6.8	8.4	mA
On-Chip Power Dissipation (All 8 Channels)	PDIS_FP_TOT_L	CLP = 1		1.44	1.7	W
NORMAL POWER MODE						
4.75V/5V Supply Current per Channel	I_C_5V_N			31	34	mA
3.3V Supply Current per Channel	I_C_3_3V_N			0.4	0.95	mA
11V Supply Current per Channel	I_C_11V_N			11.3	13	mA
On-Chip Power Dissipation (All 8 Channels)	PDIS_FP_TOT_N	(Note 9)		1.87	2.2	W

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB, D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Mode Select Response Time (Note 7)	V/C stepped from 0 to 1, DC stable within 10%		1		µs
	V/C stepped from 1 to 0, DC stable within 10%		1		
High Gain Maximum Input-Voltage Range	High LNA gain D43/D42/D41/D40 = 1/0/1/0		0.33		V_{P-P} differential
Low Gain Maximum Input-Voltage Range	Low LNA gain D43/D42/D41/D40 = 0/0/0/1		0.6		V_{P-P} differential

AC ELECTRICAL CHARACTERISTICS—VGA MODE

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, V/C = 1, NP = 0, PD = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	D42/D41/D40 = 0/0/0, R_{IN} = 50Ω	47.5	50	60	Ω
	D42/D41/D40 = 0/0/1, R_{IN} = 100Ω	90	100	110	
	D42/D41/D40 = 0/1/0, R_{IN} = 200Ω	185	200	210	
	D42/D41/D40 = 0/1/1, R_{IN} = 1000Ω, f_{RF} = 2MHz	700	830	1000	
Noise Figure	R_S = R_{IN} = 50Ω, VG+ - VG- = +3V		4.5		dB
	R_S = R_{IN} =100Ω, VG+ - VG- = +3V		3.4		
	R_S = R_{IN} = 200Ω, VG+ - VG- = +3V		2.4		
	R_S = R_{IN} = 1000Ω, VG+ - VG- = +3V		2.1		
Low-Gain Noise Figure	D43/D42/D41/D40 = 0/0/0/1, LNA gain = 12.5dB, R_S = R_{IN} = 200Ω, VG+ - VG- = +3V		3.9		dB
Input-Referred Noise Voltage	D43/D42/D41/D40 = 1/1/1/0		0.9		nV/√Hz
Input-Referred Noise Current	D43/D42/D41/D40 = 1/1/1/0		2.1		pA/√Hz
Maximum Gain, High Gain Setting	VG+ - VG- = +3V	41	42.8	45	dB
Minimum Gain, High Gain Setting	VG+ - VG- = -3V	8.5	10	11	dB
Maximum Gain, Low Gain Setting	D43/D42/D41/D40 = 0/0/0/1, VG+ - VG- = +3V	35	36.8	38	dB
Minimum Gain, Low Gain Setting	D43/D42/D41/D40 = 0/0/0/1, VG+ - VG- = -3V	2.5	4	6	dB
Anti-Aliasing Filter 3dB Corner Frequency	D45/D44 = 0/0, f_C = 9MHz		9		MHz
	D45/D44 = 0/1, f_C = 10MHz		10		
	D45/D44 = 1/0, f_C = 15MHz		15		
	D45/D44 = 1/1, f_C = 18MHz		18		
Gain Range	VG+ - VG- = -3V to +3V		33		dB

AC ELECTRICAL CHARACTERISTICS—VGA MODE (continued)

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, V/C = 1, NP = 0, PD = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Gain Error	Measured at T_A = +25°C, VG+ - VG- = -2V		±0.4		dB
	Measured at T_A = +25°C, VG+ - VG- = 0V		±0.4		
	Measured at T_A = +25°C, VG+ - VG- = +2V		±0.4		
Input Gain Compression	VG+ - VG- = -3V (VGA minimum gain), gain ratio with 330mV_{P-P}/50mV_{P-P} input tones		1.4		dB
	LNA low gain = 12.5dB, VG+ - VG- = -3V (VGA minimum gain), gain ratio with 600mV_{P-P}/50mV_{P-P}		0.8		
VGA Gain Response Time	Gain step up (V_{IN} = 5mV_{P-P}, gain changed from 10dB to 44dB, settling time is measured within 1dB final value)		1.4		µs
	Gain step down (V_{IN} = 5mV_{P-P}, gain changed from 44dB to 10dB, settling time is measured within 1dB final value)		1.6		
VGA Output Offset Under Pulsed Overload	Overdrive is ±10mA in clamping diodes, gain at 30dB, 16 pulses at 5MHz, repetition rate 20kHz; offset is measured at output when RF duty cycle is off		180		mV
Small-Signal Output Noise	20dB of gain, VG+ - VG- = -0.85V, no input signal		23		nV/√Hz
Large-Signal Output Noise	20dB of gain, VG+ - VG- = -0.85V, f_{RF} = 5MHz, f_{NOISE} = f_{RF} + 1kHz, V_{OUT} = 1V_{P-P} differential		35		nV/√Hz
Second Harmonic (HD2)	V_{IN} = 50mV_{P-P}, f_{RF} = 2MHz, V_{OUT} = 1V_{P-P}		-67		dBc
	V_{IN} = 50mV_{P-P}, f_{RF} = 5MHz, V_{OUT} = 1V_{P-P}		-64.2		
High-Gain IM3 Distortion	V_{IN} = 50mV_{P-P}, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, V_{OUT} = 1V_{P-P} (Note 11)	-52	-61		dBc
Low-Gain IM3 Distortion	D43/D42/D41/D40 = 0/0/0/1 (R_{IN} = 200Ω, LNA gain = 12.5dB),V_{IN} = 100mV_{P-P}, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, V_{OUT} = 1V_{P-P} (Note 11)	-50	-60		dBc
Standby Mode Power-Up Response Time	Gain set for 26dB, f_{RF} = 5MHz, V_{OUT} = 1V_{P-P}, settled with in 1dB from transition on NP pin		2.1		µs
Standby Mode Power-Down Response Time	To reach DC current target ±10%		2.0		µs
Power-Up Response Time	Gain set for 28dB, f_{RF} = 5MHz, V_{OUT} = 1V_{P-P}, settled within 1dB from transition on PD		2.7		ms
Power-Down Response Time	Gain set for 28dB, f_{RF} = 5MHz, DC power reaches 6mW/channel, from transition on PD		5		ns
Adjacent Channel Crosstalk	V_{OUT} = 1V_{P-P} differential, f_{RF} = 10MHz, 28dB of gain		-58		dBc
Nonadjacent Channel Crosstalk	V_{OUT} = 1V_{P-P} differential, f_{RF} = 10MHz, 28dB of gain		-71		dBc
Phase Matching Between Channels	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = 1V_{P-P}, f_{RF} = 10MHz		±1.2		Degrees

AC ELECTRICAL CHARACTERISTICS—VGA MODE (continued)

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, V/C = 1, NP = 0, PD = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3V Supply Modulation Ratio	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = 1V_{P-P}, f_{RF} = 5MHz, f_{MOD} = 1kHz, V_{MOD} = 50mV_{P-P}, ratio of output sideband at 5.001MHz, 1V_{P-P}		-73		dBc
4.75V/5V Supply Modulation Ratio	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = 1V_{P-P}, f_{RF} = 5MHz, f_{MOD} = 1kHz, V_{MOD} = 50mV_{P-P}, ratio of output sideband at 5.001MHz, 1V_{P-P}		-82		dBc
Gain Control Lines Common-Mode Rejection Ratio	Gain = 28dB, VG+ - VG- = 0.4V, f_{MOD} = 5MHz, V_{MOD} = 50mV_{P-P}, V_{OUT} = 1.0V_{P-P}		-74		dBc
Overdrive Phase Delay	VG+ - VG- = -3V, delay between V_{IN} = 300mV_{P-P} and V_{IN} = 30mV_{P-P} differential		5		ns
Output Impedance	Differential		100		Ω

AC ELECTRICAL CHARACTERISTICS—CW MODE

(*Typical Application Circuit*, V/C = 0, PD = 0, NP = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), f_{RF} = f_{LO}/16 = 5MHz, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz (Note 12). Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CW DOPPLER MIXER					
Mixer RF Frequency Range		0.9		7.6	MHz
LO Frequency Range	LO+ and LO-	16		120	MHz
Mixer Output Frequency Range		DC		100	kHz
FULL-POWER MODE					
Noise Figure	No carrier		3.4		dB
Noise Figure at 100mV_{P-P} Input	100mV_{P-P} at input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset		3.6		dB
Noise Figure at 200mV_{P-P} Input	200mV_{P-P} at input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset		4.1		dB
SNR at 100mV_{P-P} Input	100mV_{P-P} at input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset		-148.3		dBc/Hz
SNR at 200mV_{P-P} Input	200mV_{P-P} at input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset		-153.8		dBc/Hz

AC ELECTRICAL CHARACTERISTICS—CW MODE (continued)

(*Typical Application Circuit*, V/C = 0, PD = 0, NP = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), f_{RF} = f_{LO}/16 = 5MHz, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz (Note 12). Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Two-Tone Intermodulation IMD3 at 100mV	f_{RF1} = 5MHz, 0.1V_{P-P}, f_{RF2} = 5.01MHz at -25dBc, f_{LO} = 80MHz (Note 11)		-50	-55		dBc
Two-Tone Intermodulation IMD3 at 200mV	f_{RF1} = 5MHz, 0.2V_{P-P}, f_{RF2} = 5.01MHz at -25dBc, f_{LO} = 80MHz (Note 11)			-48.5		dBc
Mixer Output-Voltage Compliance	Valid voltage range (AC + DC) on summed mixer output pins		4.5		12	V
Channel-to-Channel Phase Matching	Measured under zero beat conditions, V_{RF} = 100mV_{P-P}, f_{RF} = 5MHz, f_{LO} = 80MHz (Note 13)			±0.4		Degrees
Channel-to-Channel Gain Matching	Measured under zero beat conditions, V_{RF} = 100mV_{P-P}, f_{RF} = 5MHz, f_{LO} = 80MHz (Notes 13, 14)			±0.2		dB
Transconductance	Calculated from LNA input voltage and twice the I or Q current	f_{RF} = 0.9MHz, f_{LO}/16 = 1MHz	19	23	26	mS
		f_{RF} = 7.6MHz, f_{LO}/16 = 7.5MHz	19	22.5	26	
LOW-POWER MODE (CLP = 1)						
Noise Figure	No carrier			3.2		dB
Noise Figure at 100mV_{P-P} Input	100mV_{P-P} on input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			3.5		dB
Noise Figure at 200mV_{P-P} Input	200mV_{P-P} on input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			4.3		dB
SNR at 100mV_{P-P} Input	100mV_{P-P} on input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			-148.2		dBc/Hz
SNR at 200mV_{P-P} Input	200mV_{P-P} on input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			-153.6		dBc/Hz
Two-Tone Intermodulation IMD3	f_{RF1} = 5MHz, 0.1V_{P-P}, f_{RF2} = 5.01MHz at -25dBc, f_{LO} = 80MHz (Note 11)			-44		dBc
Mixer Output-Voltage Compliance	Valid voltage range on summed mixer output pins (Note 12)		4.5		12	V
Transconductance (Note 16)	Calculated from LNA input voltage and twice the I or Q current	f_{RF} = 1.1MHz, f_{LO}/16 = 1MHz	19	21.5	26	mS
		f_{RF} = 7.6MHz, f_{LO}/16 = 7.5MHz	19	21.5	26	

AC ELECTRICAL CHARACTERISTICS—SERIAL PERIPHERAL INTERFACE

(DOUT loaded with 60pF and 10MΩ, 2ns rise and fall edges on CLK.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Speed					10	MHz
Mininimum Data-to-Clock Setup Time	t_{CS}			5		ns
Mininimum Data-to-Clock Hold Time	t_{CH}			0		ns
Mininimum Clock-to-$\overline{CS}$ Setup Time	t_{ES}			5		ns
$\overline{CS}$ Positive Mininimum Pulse Width	t_{EW}			1		ns
Mininimum Clock Pulse Width	t_{CW}			2		ns
Mininimum $\overline{CS}$ High to Mixer Clock on	$t_{MIX\overline{CS}}$			2		ns

Note 5: Minimum and maximum limits at T_A = +25°C and +70°C are guaranteed by design, characterization, and/or production test.

Note 6: Noise performance of the device is dependent on the noise contribution from V_{REF}. Use a low-noise supply for V_{REF}.

Note 7: Note that the LVDS CWD LO clocks are DC-coupled. This is to ensure immediate synchronization when the clock is first turned on. An AC-coupled LO is problematic in that the RC time constant associated with the coupling capacitors and the input impedance of the pin causes a period of time (related to the RC time constant) when the DC level on the chip side of the capacitor is outside the acceptable common-mode range and the LO swing does not excede both of the logic thresholds required for proper operation. This problem associated with AC-coupling causes an inability to ensure synchronization among beamforming channels. The LVDS signal is terminated differentially with an external 100Ω resistor on the board.

Note 8: An external 100Ω resistor terminates the LVDS differential signal path.

Note 9: Total on-chip power dissipation is calculated as $P_{DISS} = V_{CC1} \times I_{CC1} + V_{CC2} \times I_{CC2} + V_{REF} \times I_{REF} + [11V - (I_{11V}/4) \times 162] \times I_{11V}$.

Note 10: This response time does not include the CW output highpass filter. When switching to VGA mode, the CW outputs stop drawing current and the output voltage goes to the rail. If a highpass filter is used, the recovery time may be excessive and a switching network is recommended, as shown in the *Applications Information* section.

Note 11: See the *Ultrasound-Specific IMD3 Specification* section.

Note 12: The reference input noise is given for 8 channels, knowing that the reference-noise contributions are correlated in all 8 channels. If more channels are used, the reference noise must be reduced to get the best noise performance.

Note 13: Channel-to-channel gain and phase matching measured on 30 pieces during engineering characterization at room temperature. Each mixer is used as a phase detector and produces a DC voltage in the IQ plane. The phase is given by the angle of the vector drawn on that plane. Multiple channels from multiple parts are compared to each other to produce the phase variation.

Note 14: Voltage gain is measured by subtracting the output-voltage signal from the input-voltage signal. The output-voltage signal is obtained by taking the differential CW I output and summing it in quadrature with the differential CW Q output. The input voltage is defined as the differential voltage applied to the CW input pins.

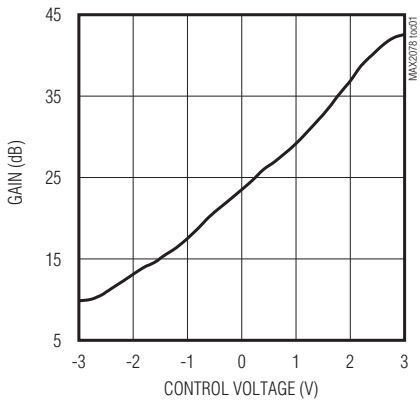
Note 15: Mixer output-voltage compliance is the range of acceptable voltages allowed on the CW mixer outputs.

Note 16: Transconductance is defined as the quadrature-combined CW differential output current at baseband divided by the mixer's input voltage.

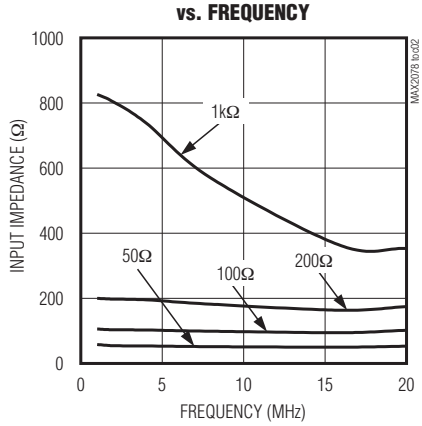
典型工作特性

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

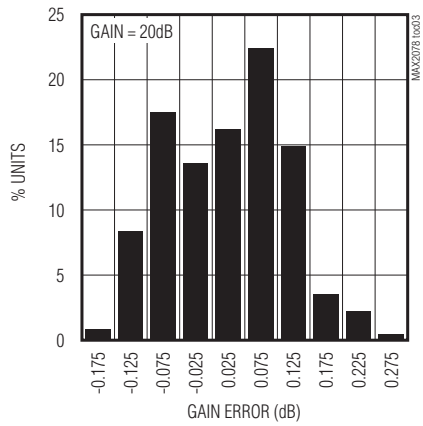
GAIN vs. DIFFERENTIAL ANALOG CONTROL VOLTAGE



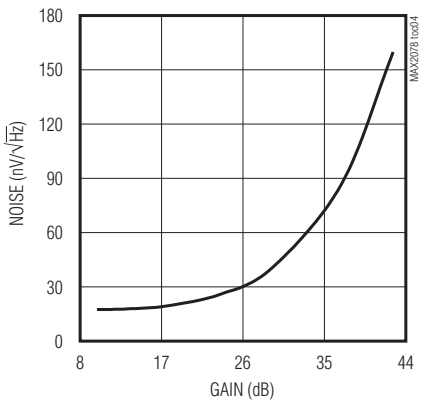
COMPLEX INPUT IMPEDANCE MAGNITUDE vs. FREQUENCY



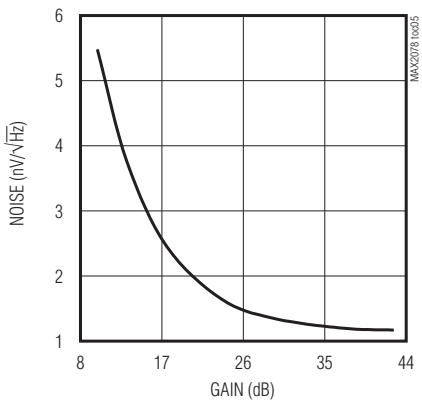
GAIN ERROR HISTOGRAM



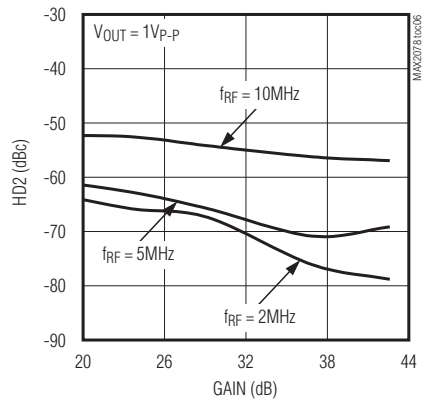
OUTPUT-REFERRED NOISE vs. GAIN



INPUT-REFERRED NOISE vs. GAIN



SECOND-HARMONIC DISTORTION vs. GAIN



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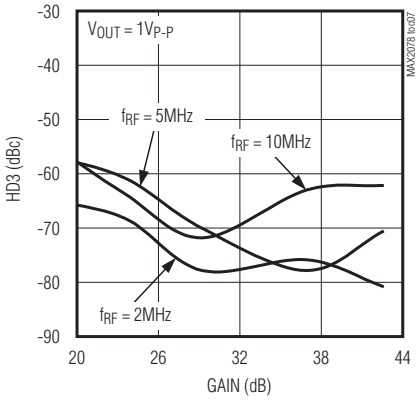
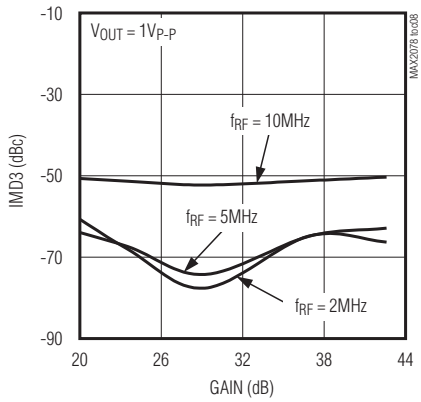
典型工作特性(续)

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), $f_{RF} = f_{LO}/16$ = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

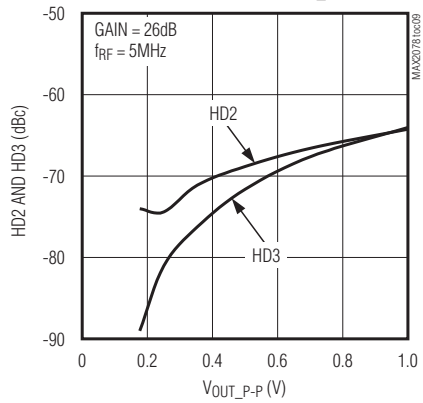
THIRD-HARMONIC DISTORTION vs. GAIN



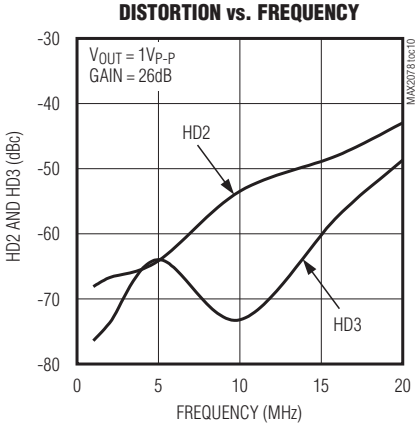
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. GAIN



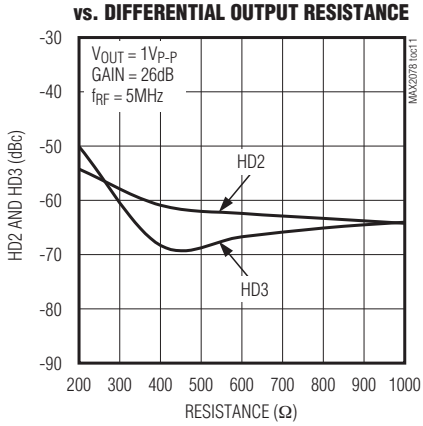
SECOND- AND THIRD-HARMONIC DISTORTION vs. V_{OUT_P-P}



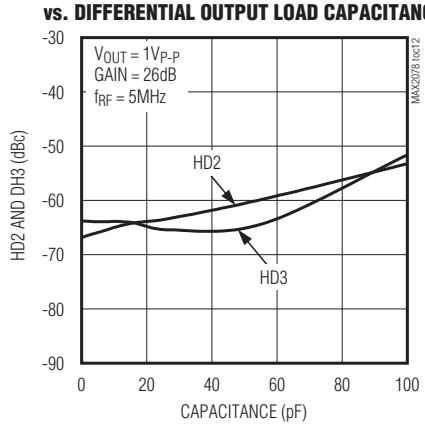
SECOND- AND THIRD-HARMONIC DISTORTION vs. FREQUENCY



SECOND- AND THIRD-HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT RESISTANCE



SECOND- AND THIRD-HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT LOAD CAPACITANCE



典型工作特性(续)

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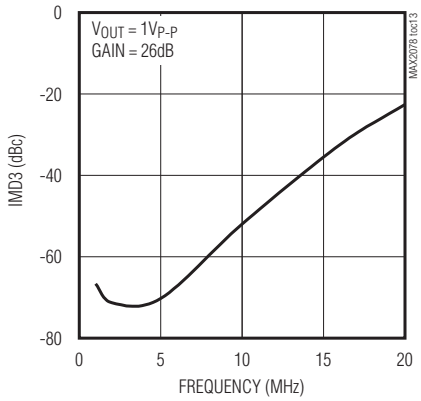
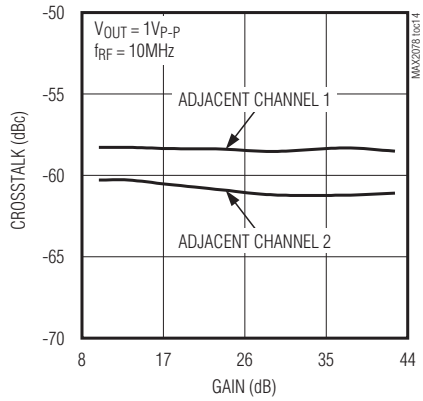
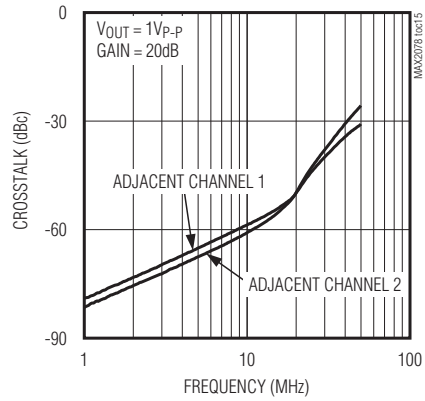
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. FREQUENCY



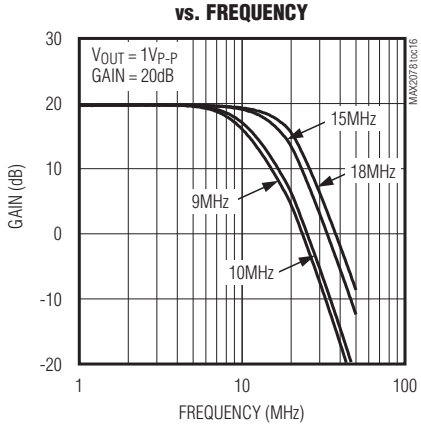
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN



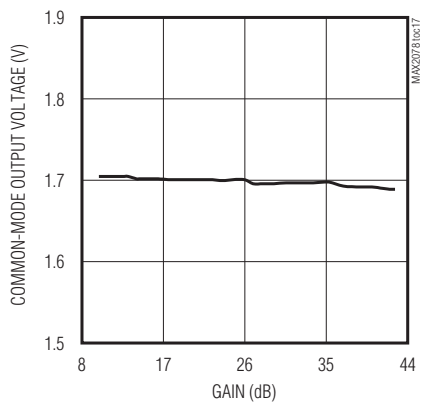
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



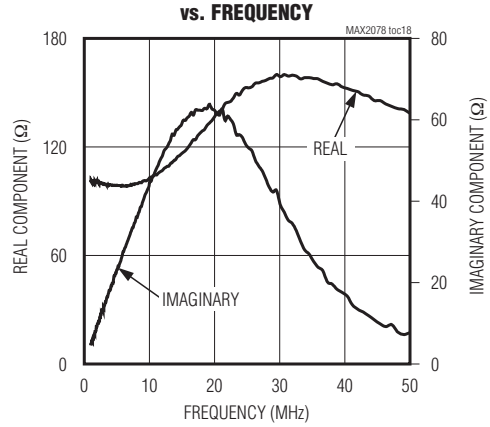
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



COMMON-MODE OUTPUT VOLTAGE vs. GAIN



DIFFERENTIAL OUTPUT IMPEDANCE vs. FREQUENCY



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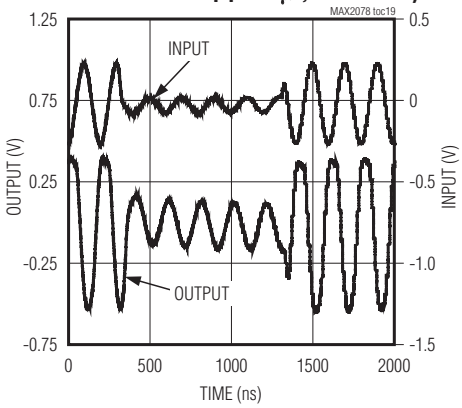
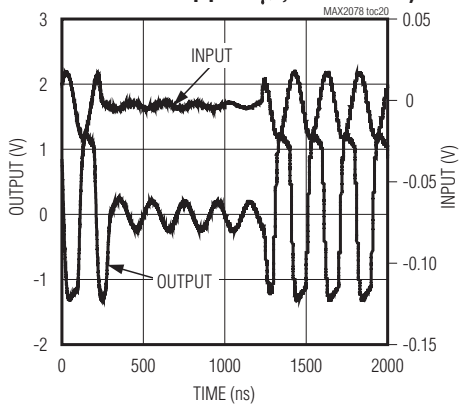
典型工作特性(续)

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

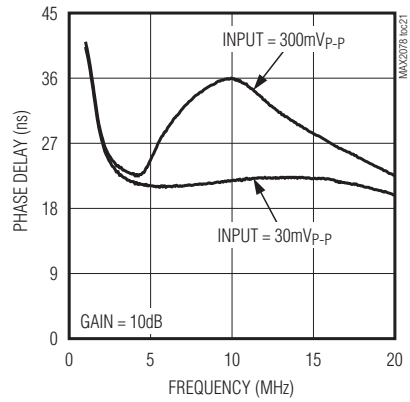
LNA OVERLOAD RECOVERY TIME
(V_{IN} = 500mV$_{P-P}$ for 1µs TO 100mV$_{P-P}$ for 1µs AND BACK TO 500mV$_{P-P}$ for 1µs, GAIN = 10dB)



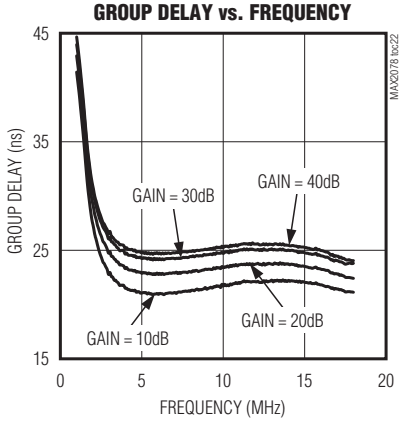
VGA OVERLOAD RECOVERY TIME
(V_{IN} = 40mV$_{P-P}$ for 1µs TO 4mV$_{P-P}$ for 1µs AND BACK TO 40mV$_{P-P}$ for 1µs, GAIN = 42.5dB)



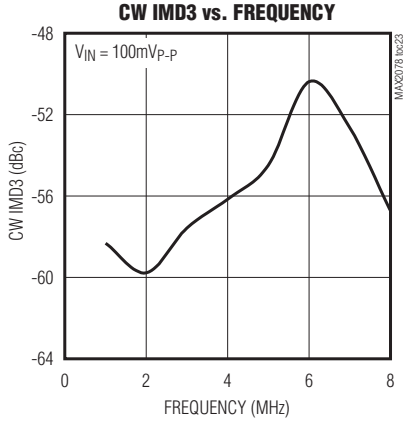
OVERDRIVE PHASE DELAY vs. FREQUENCY



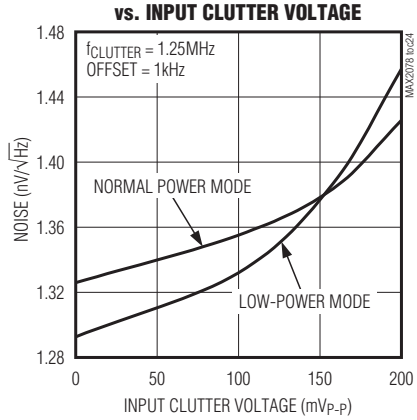
GROUP DELAY vs. FREQUENCY



CW IMD3 vs. FREQUENCY



INPUT-REFERRED NOISE vs. INPUT CLUTTER VOLTAGE



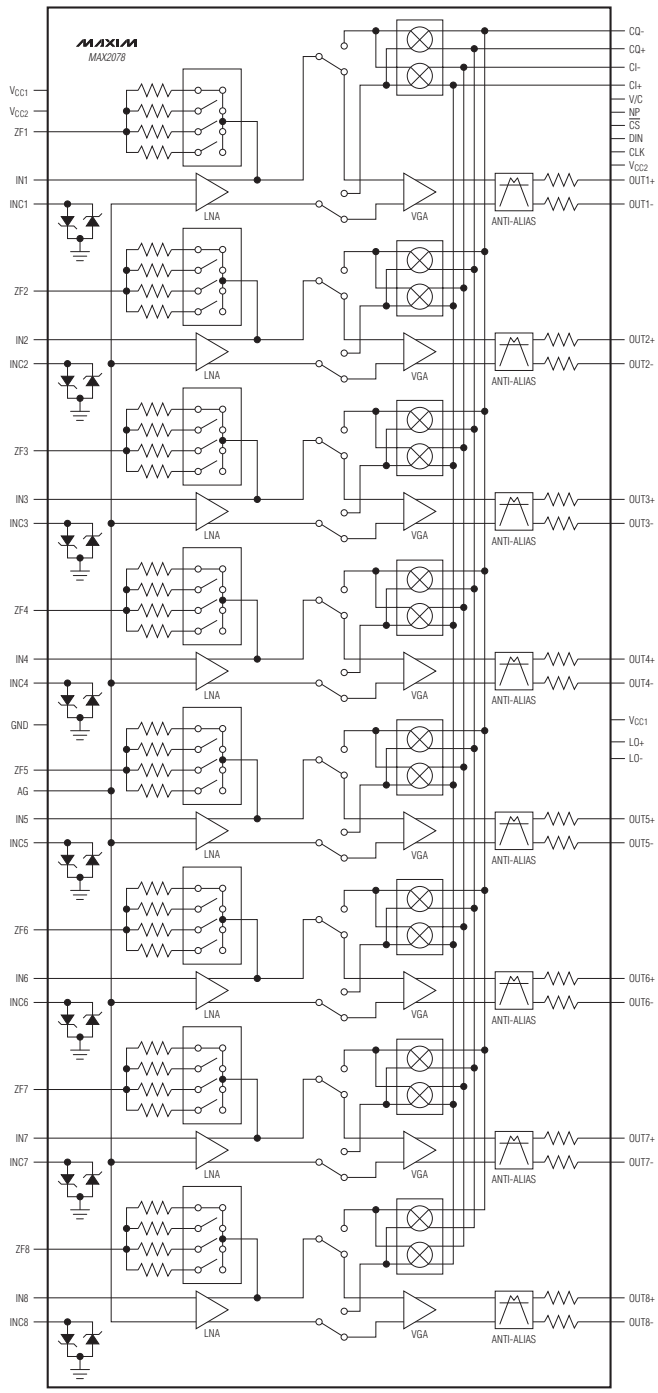
引脚说明

引脚	名称	功能
1	IN2	通道2输入。
2	INC2	通道2箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
3	ZF3	通道3有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
4	IN3	通道3输入。
5	INC3	通道3箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
6	ZF4	通道4有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
7	IN4	通道4输入。
8	INC4	通道4箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
9, 28, 31	GND	地。
10	AG	交流地，连接一个低ESR的1µF电容至地。
11	ZF5	通道5有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
12	IN5	通道5输入。
13	INC5	通道5箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
14	ZF6	通道6有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
15	IN6	通道6输入。
16	INC6	通道6箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
17	ZF7	通道7有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
18	IN7	通道7输入。
19	INC7	通道7箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
20	ZF8	通道8有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
21	IN8	通道8输入。
22	INC8	通道8箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
23, 33, 53, 64	V_{CC2}	4.75V电源，连接至外部4.75V电源。在外部将所有4.75V电源引脚连接在一起，并尽量靠近引脚放置100nF旁路电容。
24	V_{REF}	外部2.5V基准电源，连接至低噪声电源。通过0.1µF电容旁路至GND，电容须靠近引脚放置。注意，器件噪声性能取决于V_{REF}端引入的噪声，V_{REF}须使用低噪声电源。
25, 44, 63	V_{CC1}	3.3V电源，连接至外部3.3V电源。在外部将所有3.3V电源引脚连接在一起，并尽量靠近引脚放置100nF旁路电容。
26	VG+	VGA模拟增益控制差分输入。差分电压为-3V时对应于最小增益设置，+3V时对应于最大增益设置。
27	VG-	
29	CLP	CW低功耗模式选择输入，将CLP驱动至高电平使CW混频器进入低功耗模式。
30	PD	关断模式选择输入。PD置于V_{CC1}时，整个器件进入关断模式；PD置于低电平时正常工作。该模式的设置权限高于待机模式。
32	DOUT	串口数据输出。数据输出简化了菊链配置，电平为3.3V CMOS。
34	OUT8-	通道8差分输出负端。
35	OUT8+	通道8差分输出正端。
36	OUT7-	通道7差分输出负端。

引脚说明(续)

引脚	名称	功能
37	OUT7+	通道7差分输出正端。
38	OUT6-	通道6差分输出负端。
39	OUT6+	通道6差分输出正端。
40	OUT5-	通道5差分输出负端。
41	OUT5+	通道5差分输出正端。
42	LO-	本地振荡器差分输入，LO在波束成形器中分频。
43	LO+	
45	OUT4-	通道4差分输出负端。
46	OUT4+	通道4差分输出正端。
47	OUT3-	通道3差分输出负端。
48	OUT3+	通道3差分输出正端。
49	OUT2-	通道2差分输出负端。
50	OUT2+	通道2差分输出正端。
51	OUT1-	通道1差分输出负端。
52	OUT1+	通道1差分输出正端。
54	CLK	串口时钟输入(上升沿触发)，3.3V CMOS。时钟输入用于编程串行移位寄存器。
55	DIN	串口数据输入，3.3V CMOS。数据输入用于编程串行移位寄存器。
56	$\overline{CS}$	串口片选输入，3.3V CMOS。用于存储寄存器的设置位，并在CW模式下同步所有通道的相位(上升沿)。
57	NP	VGA待机模式选择输入。NP置于1时，整个器件进入待机模式。该模式设置权限高于串行移位寄存器中的通道软关断设置，但优先级低于通用断电(PD)模式设置。
58	V/C	VGA/CW模式选择输入。将V/C置于逻辑高电平使能VGA，关闭CW模式；将V/C置于逻辑低电平，使能CW混频器，关闭VGA模式。
59	CQ-	8通道CW正交输出负端，通过162Ω外部上拉电阻连接至外部11V电源。
60	CQ+	8通道CW正交输出正端，通过162Ω外部上拉电阻连接至外部11V电源。
61	CI-	8通道CW同相输出负端，通过162Ω外部上拉电阻连接至外部11V电源。
62	CI+	8通道CW同相输出正端，通过162Ω外部上拉电阻连接至外部11V电源。
65	ZF1	通道1有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
66	IN1	通道1输入。
67	INC1	通道1箝位输入，连接至输入耦合电容，详细说明请参考*典型应用电路*。
68	ZF2	通道2有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
—	EP	裸焊盘，内部连接至地。通过多个过孔连接至大面积地平面，以改善散热和电气特性。不要将其作为电气连接点。

方框图


MAXIM
MAX2078
VCC1
VCC2
ZF1
IN1
INC1
ZF2
IN2
INC2
ZF3
IN3
INC3
ZF4
IN4
INC4
GND
ZF5
AG
IN5
INC5
ZF6
IN6
INC6
ZF7
IN7
INC7
ZF8
IN8
INC8
LNA
VGA
ANTI-ALIAS
CQ-
CQ+
CI-
CI+
V/C
NP
CS
DIN
CLK
VCC2
OUT1+
OUT1-
OUT2+
OUT2-
OUT3+
OUT3-
OUT4+
OUT4-
VCC1
LO+
LO-
OUT5+
OUT5-
OUT6+
OUT6-
OUT7+
OUT7-
OUT8+
OUT8-

8通道超声前端，提供CW多普勒混频器

详细说明

MAX2078是高密度、8通道超声接收器，优化用于低成本、多通道、高性能便携式和车载超声应用。集成8通道LNA、VGA、AAF和可编程CWD波束成形器提供完整的多功能超声接收方案。

成像通道动态范围经过优化，具有优异的二次谐波性能。整个成像接收通道在5MHz时具有出色的68dBFS** SNR。双极型超声前端经过优化，其极低的近载波调制噪声在高杂波环境中可以提供优异的低速PW和流体多普勒彩超检测灵敏度，并在V_{OUT} = $1V_{P-P}$、5MHz杂波输出、1kHz频偏下，具有140dBc/Hz的近载波SNR。

MAX2078还集成了8通道正交混频器阵列和可编程LO相位发生器，构建完备的连续波多普勒(CWD)波束成形方案。每个通道独立的混频器可优化CWD灵敏度，在$200mV_{P-P}$、1.25MHz输入信号、1kHz频偏下达到154dBc/Hz的SNR。通过数字串行接口和一个高频时钟编程选择每个通道的LO相位。串口设计支持多个器件方便菊链，占用最少的编程接口。混频器输出叠加在每个I、Q差分电流输出。

工作模式

MAX2078需要在使用之前进行编程。工作模式由47个设置位进行控制，表1和表2给出了这些设置位的功能。

***配合MAX1437B ADC使用。*

表1. 设置位总结

BIT NAME	DESCRIPTION
D40, D41, D42	Input impedance programming
D43	LNA gain (D43 = 0 is low gain)
D44, D45	Anti-alias filter f_C programming
D46	Don't care
D0–D39	Beamformer programming, from channel 1 to 8

表2. 设置位的逻辑功能

D46	D45	D44	D43	D42	D41	D40	MODE
X	X	X	1	0	0	0	R_{IN} = 50Ω, LNA gain = 18.5dB
X	X	X	1	0	0	1	R_{IN} = 100Ω
X	X	X	1	0	1	0	R_{IN} = 200Ω
X	X	X	1	0	1	1	R_{IN} = 1000Ω
X	X	X	0	0	0	0	R_{IN} = 100Ω, LNA gain = 12.5dB
X	X	X	0	0	0	1	R_{IN} = 200Ω
X	X	X	0	0	1	0	R_{IN} = 400Ω
X	X	X	0	0	1	1	R_{IN} = 2000Ω
X	X	X	1	1	X	X	Open feedback
X	0	0	X	X	X	X	f_C = 9MHz
X	0	1	X	X	X	X	f_C = 10MHz
X	1	0	X	X	X	X	f_C = 15MHz
X	1	1	X	X	X	X	f_C = 18MHz

X = 无关。

8通道超声前端，提供CW多普勒混频器

低噪声放大器(LNA)

MAX2078的LNA经过优化，具有优异的动态范围和线性指标，可理想用于超声成像应用。当LNA工作在低增益模式，输入阻抗(R_{IN})为增益A的函数($R_{IN} = R_F/(1 + A)$)，增大至原来的2倍。因此，控制反馈电阻(R_F)的开关必须改变。例如，高增益模式下100Ω的电阻在低增益模式下将变为200Ω (参见表2)。

可变增益放大器(VGA)

MAX2078的VGA优化于高线性度、高动态范围和低输出噪声，这些性能都是超声成像应用的关键参数。每个VGA通路包含模拟增益调节电路，以及带差分输出端口(OUT_+、OUT_-)的输出缓冲器，用于驱动ADC，详细内容请参考*高级CW混频器和可编程波束成形器功能框图*。

VGA增益可以通过差分增益控制输入VG+和VG-调节。差分增益控制输入电压为-3V时对应于最小增益，+3V时对应于最大增益。差分模拟控制共模电压为1.65V (典型值)。

过载恢复

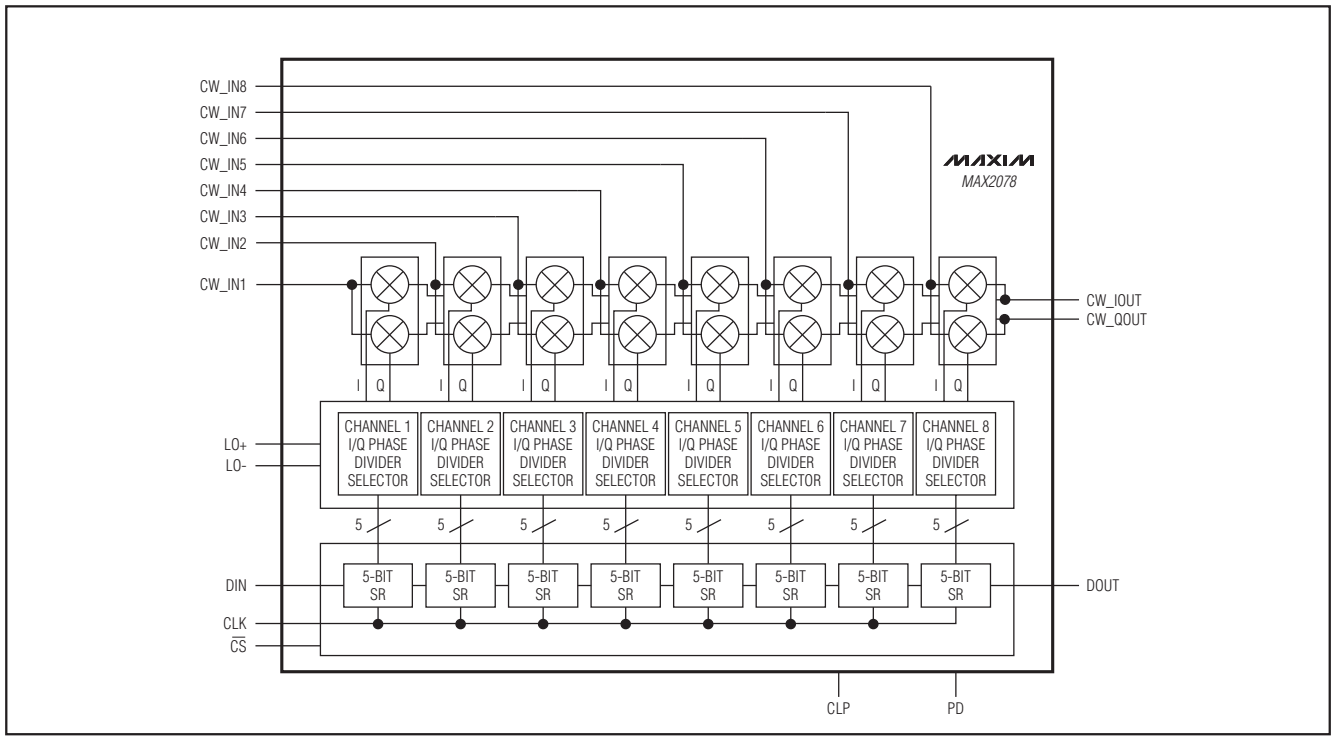
器件经过优化设计具有快速过载恢复功能，非常适合典型的成像系统，这些系统的超声输入缓冲器通常具有较大的输入信号，请参考*典型工作特性*中关于瞬态过载的快速恢复时间示意图。

8通道连续波(CW)混频器

MAX2078 CW混频器采用有源双平衡架构，混频器具有高动态范围、高线性度特性和极低的热噪声、抖动噪声，可理想用于超声CWD信号接收。8路正交混频器阵列在1.25MHz、200mV_{P-P}输入杂波信号、1kHz频偏下具有154dBc/Hz的噪声指标、-48.5dBc (典型值)的双音3阶互调超声指标，请参考*超声规范定义的IMD3*部分。

8通道阵列提供正交、同相差分电流输出(CQ+、CQ-、CI+、CI-)，以产生总的CWD波束成形信号。最大差分电流输出为3mA_{P-P}，混频器输出电压范围为4.5V至12V。

高级CW混频器和可编程波束成形器功能框图



8通道超声前端，提供CW多普勒混频器

每个混频器可以设置在16种相位之一，因此每个通道需要4个设置位。每个CW通道通过将Di置为1，使其进入关闭状态。关断模式(PD)引脚的设置权限高于软关断设置。

串行移位寄存器编程后，将$\overline{CS}$信号拉高，则按照每通道5位的格式装载相位信息，设置I/Q相位分频器/选择器。这一过程将预先设置分频器，选择适当的混频器相位，混频器相位配置参见表3。

CW混频器输出合成

八路混频器阵列的输出在内部合成，以产生总的CWD合成波束成形信号。八路阵列产生八路正交(Q)的差分输出和八路同相(I)的差分输出。所有正交、同相输出相加至单路I、Q差分电流输出(CQ+、CQ-、CI+、CI-)。

LO相位选择

LO分相器可通过移位寄存器设置，可设置16个正交相位，构成完整的CW波束成形方案。

同步

图1给出了通过串行数据端口对8个独立通道串行编程的流程。注意，串行数据能够以菊链方式连接，通过一条数据线实现系统的多芯片编程。

表3. 混频器相位配置

PER CHANNEL	MSB				LSB	SHUTDOWN
PHASE (DEGREE)	Di + 4	Di + 3	Di + 2	Di + 1		Di
0	0	0	0	0		0/1
22.5	1	0	0	0		0/1
45	0	1	0	0		0/1
67.5	1	1	0	0		0/1
90	0	0	1	0		0/1
112.5	1	0	1	0		0/1
135	0	1	1	0		0/1
157.5	1	1	1	0		0/1
180	0	0	0	1		0/1
202.5	1	0	0	1		0/1
225	0	1	0	1		0/1
247.5	1	1	0	1		0/1
270	0	0	1	1		0/1
292.5	1	0	1	1		0/1
315	0	1	1	1		0/1
337.5	1	1	1	1		0/1

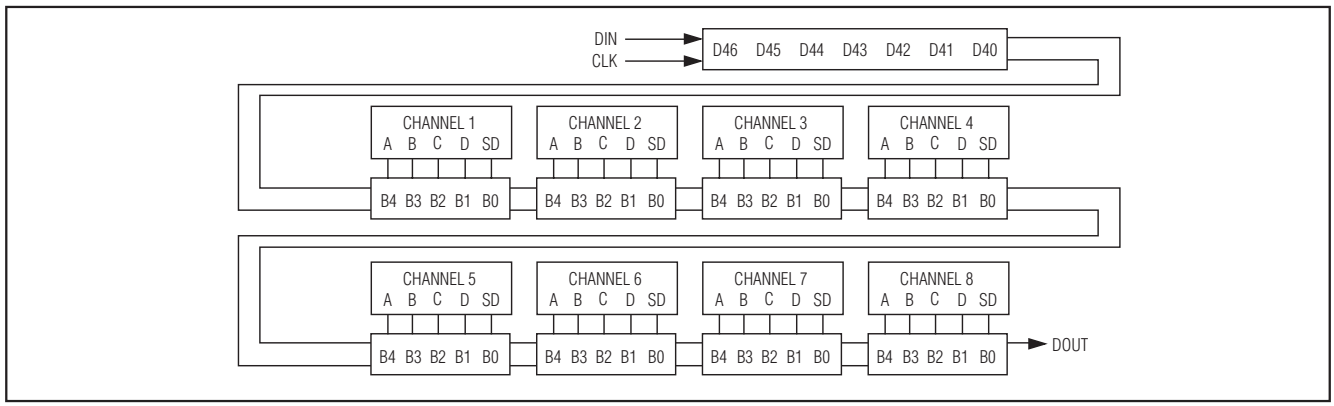


图1. 串行移位寄存器的数据流

VGA和CW混频器工作原理

标准工作模式下，MAX2078配置为VGA通道使能而混频器阵列关断(VGA模式)，或者配置为正交混频器阵列使能而VGA通道关断(CW模式)。对于VGA模式，将V/C置为逻辑高电平；对于CW模式，将V/C置于逻辑低电平。

关断和低功耗模式

MAX2078还可以通过PD控制关断，PD为V_{CC1}时进入关断模式。关断模式下，器件仅消耗1µA以内的总电源电流。PD置为逻辑低电平时，进入正常工作模式。

器件提供低功耗模式，以降低CWD模式的功耗。选择低功耗模式时，复合混频器工作在更低的静态电流，每通道总电流降至34.2mA。注意，工作在此模式时，器件的动态性能略有降低。表4给出了标准工作模式的逻辑功能。

应用信息

模式选择响应时间

模式选择响应时间表示器件在CW和VGA模式间切换时需要的时间。图2给出了CW输出与仪表放大器连接，用于驱动ADC的一种方案。该方案中，每个CQ+、CQ-、CI+、CI-输出与其驱动电路之间有四个大电容(介于470nF至1µF之间)。CW混频器输出通常用于驱动仪表放大器的输入，这些仪表放大器由运算放大器组成，其输入阻抗由共模电压设置电阻决定。

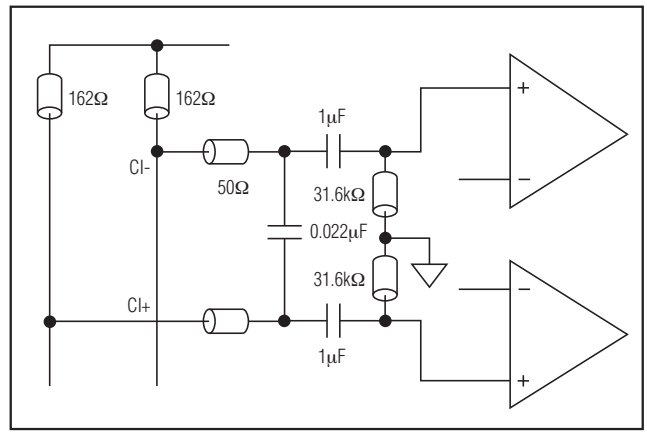


图2. CW混频器输出电路的典型范例

很明显，这一输出网络既有高通滤波器，也有低通滤波器。低通滤波器主要由162Ω混频器上拉电阻、50Ω串联电阻以及0.022µF并联电容组成。低通滤波器用于滤除LO泄漏和上边带的组合噪声。高通滤波器主要由1µF隔直流电容和31.6kΩ并联电阻组成，需要谨慎考虑。

表4. 标准工作模式的逻辑功能

PD INPUT	V/C	CLP	VGA	CW MIXER	INTERNAL SWITCH TO VGA	INTERNAL SWITCH TO CW MIXER	3.3V V_{CC} CURRENT CONSUMPTION	5V V_{CC} CURRENT CONSUMPTION	11V V_{MIX} CURRENT CONSUMPTION
1	1	N/A	Off	Off	Off	Off	0.3µA	0.4µA	0
1	0	N/A	Off	Off	Off	Off	0.1µA	0.6µA	0
0	0	0	Off	On	Off	On	3.2mA	248mA	90.4mA
0	0	1	Off	On	Off	On	3.2mA	216mA	54.4mA
0	1	N/A	On	Off	On	Off	88mA	48mA	0

N/A = 不适用。

8通道超声前端，提供CW多普勒混频器

简化后的高通滤波器如图3所示。

这里的高通滤波器极点为$f_P = 1/(2 \times \pi \times RC)$，大约为5Hz。注意，较低的高通滤波器角频率用于滤除下变频器的杂散频率，它出现在直流附近，但不会干扰低至400Hz的CWD成像信号。例如，如果需要采用低至400Hz的CWD，高通滤波器极点的最佳选择应该至少为该频率的十分之一(< 40Hz)，保证该极点不会对有用信号产生衰减。注意，如果高通滤波器极点设置为400Hz，角频率处的频响将会下降3dB。上例中高通滤波器的极点采用5Hz，满足上述讨论的直流至40Hz限制。

问题在于，混频器输出与仪表放大器之间任何大小合适的隔直流电容都会引入明显的时间常数，从而降低模式选择的切换速度。

图4给出了一个图2的替代方案，能够实现快速的模式选择响应时间。

图4中，CWD混频器的输出与仪表放大器的输入直流耦合。因此运算放大器必须能够支持混频器输出的全部范围，当混频器禁止时最大为11V，当混频器使能时低至5V的MAX2078电源电压。运算放大器可由高压11V以及低压5V供电，因此需要6V运算放大器。

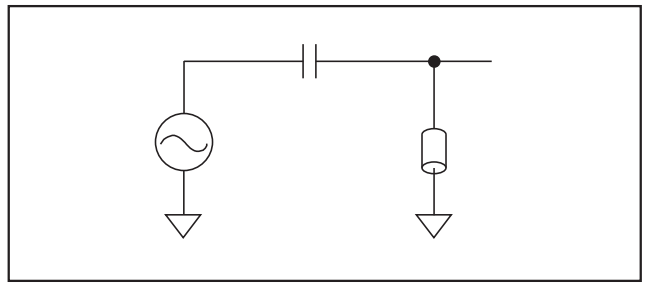


图3. 确定高通滤波器极点的简化电路

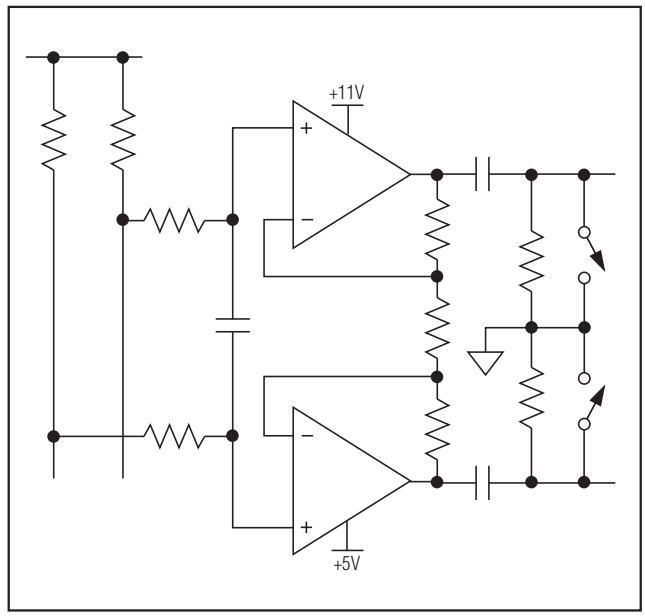


图4. 直流耦合输入至仪表放大器，以改善模式选择的响应时间

串口

MAX2078通过串行移位寄存器进行编程设置。这种方式大大简化了编程电路的复杂度，减少了编程所需的IC引脚，并降低了PCB布局的复杂度。设置位的顺序请参考表5。数据输入(DIN)和数据输出(DOUT)可以构建逐个器件的菊链，所有前端工作在同一编程时钟下。

$\overline{CS}$拉至低电平时装载数据，整个字装载完毕后，需要将$\overline{CS}$拉至高电平。器件编程时，LSB在前、MSB在后。

设置波束成形器

标准CWD工作模式下，混频器时钟(LO+、LO-)开启，编程信号(DIN、CLK、$\overline{CS}$)关闭($\overline{CS}$ = 高电平、CLK = 低电平、DIN = 无关，但固定为高电平或低电平)。开始编程时，关闭混频器时钟。数据按照推荐的10MHz编程速率或100ns最小数据时钟周期/时间移入移位寄存器。对于一个64通道CWD接收器，每通道5位，则需花费30ms，时序详细信息参见图5。设置移位寄存器后，拉高$\overline{CS}$将适当的内部计数器数值装载到I/Q分相器/选择器。这时，混频器时钟应当关闭，否则装载引脚时序和混频器时钟时序之间可能会发生时序问题。用户开启混频器时钟启动波束成形，时钟必须打开才能在混频器时钟周期开始时启动工作。混频器时钟不能存在较窄的干扰脉冲，否则会在I/Q分相器产生亚稳态。

表5. 设置位顺序

47 REGISTER BITS																	
MSB																	LSB
								CHANNEL 1 (i = 1)				…	CHANNEL 8 (i = 8)				
D46	D45	D44	D43	D42	D41	D40	D39	D38	D37	D36	D35	…	D4	D3	D2	D1	D0
D46	D45	D44	D43	D42	D41	D40	Di + 4	Di + 3	Di + 2	Di + 1	Di	…	Di + 4	Di + 3	Di + 2	Di + 1	Di

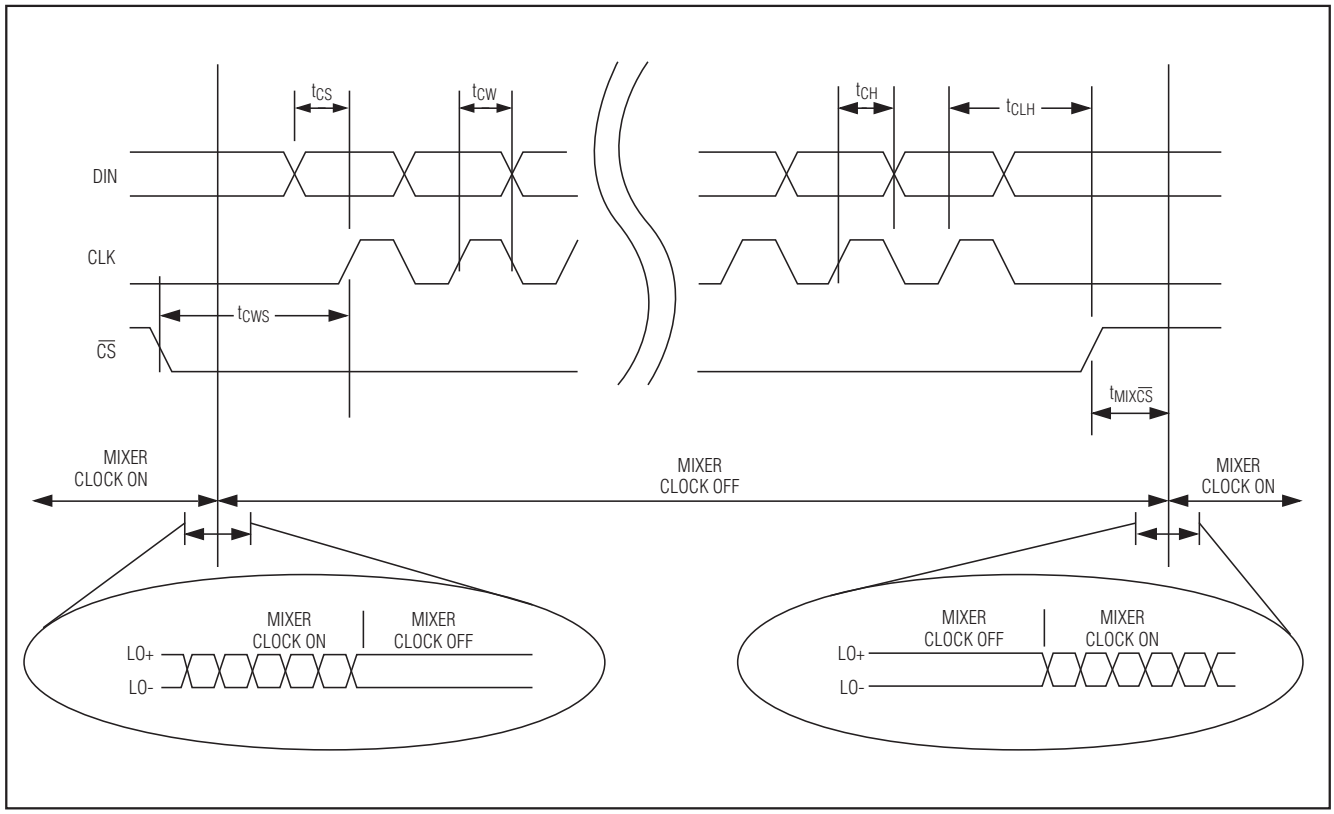


图5. 移位寄存器时序图

8通道超声前端，提供CW多普勒混频器

超声前端CWD波束成形器

用户提供一路16MHz至120MHz的LO时钟，较高的时钟频率需要差分LVDS输入。注意，LVDS CWD LO时钟采用直流耦合，以保证时钟首次开启后迅速同步。交流耦合LO存在一定的问题，因为耦合电容和引脚输入电阻所形成的RC时间常数会产生一定的时间延迟(与RC时间常数有关)，当电容芯片侧的直流电平超出可接受的共模范围时，LO摆幅无法满足正常工作要求的高、低电平逻辑门限。这个由交流耦合引发的问题将会造成波束成形通道无法同步。

LVDS信号在电路板上以100Ω外部差分电阻端接。LO输入在内部进行16分频，产生1MHz至7.5MHz频率范围的16个相位。每个通道具有一个分频器，每通道对应于5位移位寄存器(4位设置相位，1位用于通道使能)，设置16分频电路的输出相位。移位寄存器的前4位用于设置16个相位，第5位通过串行总线用于独立开启/关闭每个通道。

CW混频器输出合成

最大差分电流输出通常为3mA$_{P-P}$，而每个混频器通道的混频输出电压范围为4.5V至12V。每个差分混频器输出的混频器共模电流通常为2.83mA。在每个162Ω负载电阻下，总电流输出等于N x 2.83mA (其中N = 通道数)。本例中，+V_{SUM}和-V_{SUM}的静态输出电压为11V - (N x 2.83mA x 162Ω) = 11V - (8 x 2.83mA x 162Ω) = 7.34V。当一个通道由最大输出电流(差分2.8mA$_{P-P}$)驱动，而其它通道没有驱动时，每个输出的电压摆幅为1.4mA$_{P-P}$ x 162Ω，或226mV$_{P-P}$，而差分电压为452mV$_{P-P}$。本例中，电压范围为+V_{SUM}和-V_{SUM}的有效范围。

有源阻抗匹配

为提供优异的噪声系数指标，每个放大器的输入阻抗均采用反馈拓扑，实现有源阻抗匹配。在放大器的反相输入与输出之间增加阻值为(1 + (A/2)) x R_S的反馈电阻。输入阻抗为反馈电阻(Z_F)除以1 + (A/2)。系数2源于定义差分输出的放大器增益(A)。对于共模输入阻抗，可以使用内部数字编程阻抗(参见表1和表2)。对于其它输入阻抗，设置配合外部电阻使用的阻抗，然后根据上述公式利用外部电阻设置输入阻抗。

表6. 噪声系数与源阻抗和输入阻抗

R_S (Ω)	R_{IN} (Ω)	NF (dB)
50	50	4.5
100	100	3.4
200	200	2.4
1000	1000	2.1

噪声系数

MAX2078设计用于提供最高输入灵敏度和优异的低噪声系数。选择输入有源器件保持极低的等效输入噪声电压和电流，针对50Ω至1000Ω源阻抗优化。另外，匹配电阻引入的噪声将被衰减1 + (A/2)倍。采用这种结构，放大器的典型噪声系数在R_{IN} = R_S = 200Ω时可以达到大约2.4dB，表6给出了其它输入阻抗下的噪声系数。

输入箝位

MAX2078集成了可配置的输入箝位二极管，二极管箝位至地电位的±0.8V。输入箝位二极管可以避免大的瞬态信号过驱动放大器输入。输入过驱动可能对输入耦合电容充电，造成较长的过载恢复时间。输入信号交流耦合至单端输入IN1至IN8，但INC1至INC8输入具有箝位，参见*典型应用电路*。如果选择外部箝位器件，可以将INC1至INC8浮空。

模拟输出耦合

每路VGA的差分输出可驱动25pF的连接至GND的差分负载电容，而VGA输出差分电容为15pF，R_L = 1kΩ。差分输出具有大约1.73V的共模偏置。如果下一级具有不同的共模输入范围，则对这些差分输出采用交流耦合。

超声规范定义的IMD3

与典型的通信规范不同，超声规范定义的双音IMD3指标对应的两个输入音具有不同的幅度。测试中，f_1代表肌肉等组织的反射波，f_2代表血液的反射波。后者一般比前者的幅度低25dB，所以这种测量方式中，双音输入的其中一个比另一个低25dB。在超声应用中，IMD3指标(f_1 - (f_2 - f_1))表现为不希望出现的多普勒误差信号(见图6)。

PCB布局

MAX2078的引脚配置经过优化后，能够很方便地与相关分立元件连接，实现紧凑的物理布局。通常，该器件与几个器件一起构成多通道信号处理系统。

MAX2078采用TQFN-EP封装，其裸焊盘(EP)提供了一个与管芯之间的低热阻通道。设计PCB时，借助MAX2078的裸焊盘散热非常重要。此外，将裸焊盘通过一个低电感路径连接至电气地。裸焊盘**必须**直接或通过一系列电镀过孔焊接至PCB的地层。

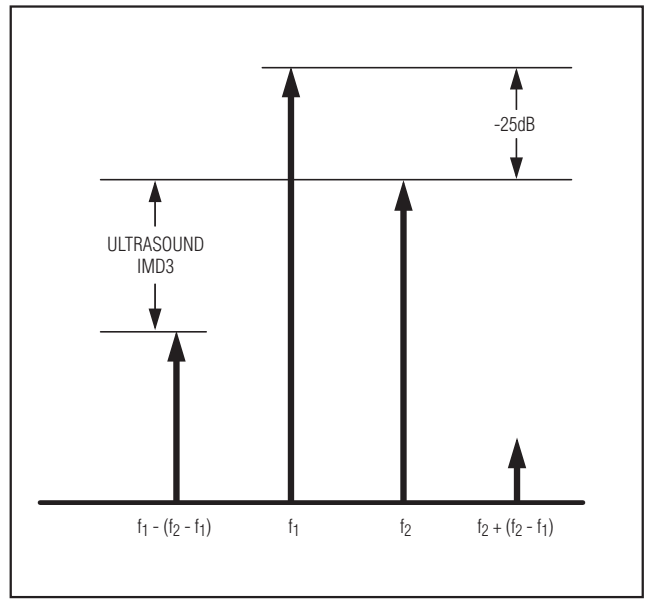


图6. 超声IMD3测量方法

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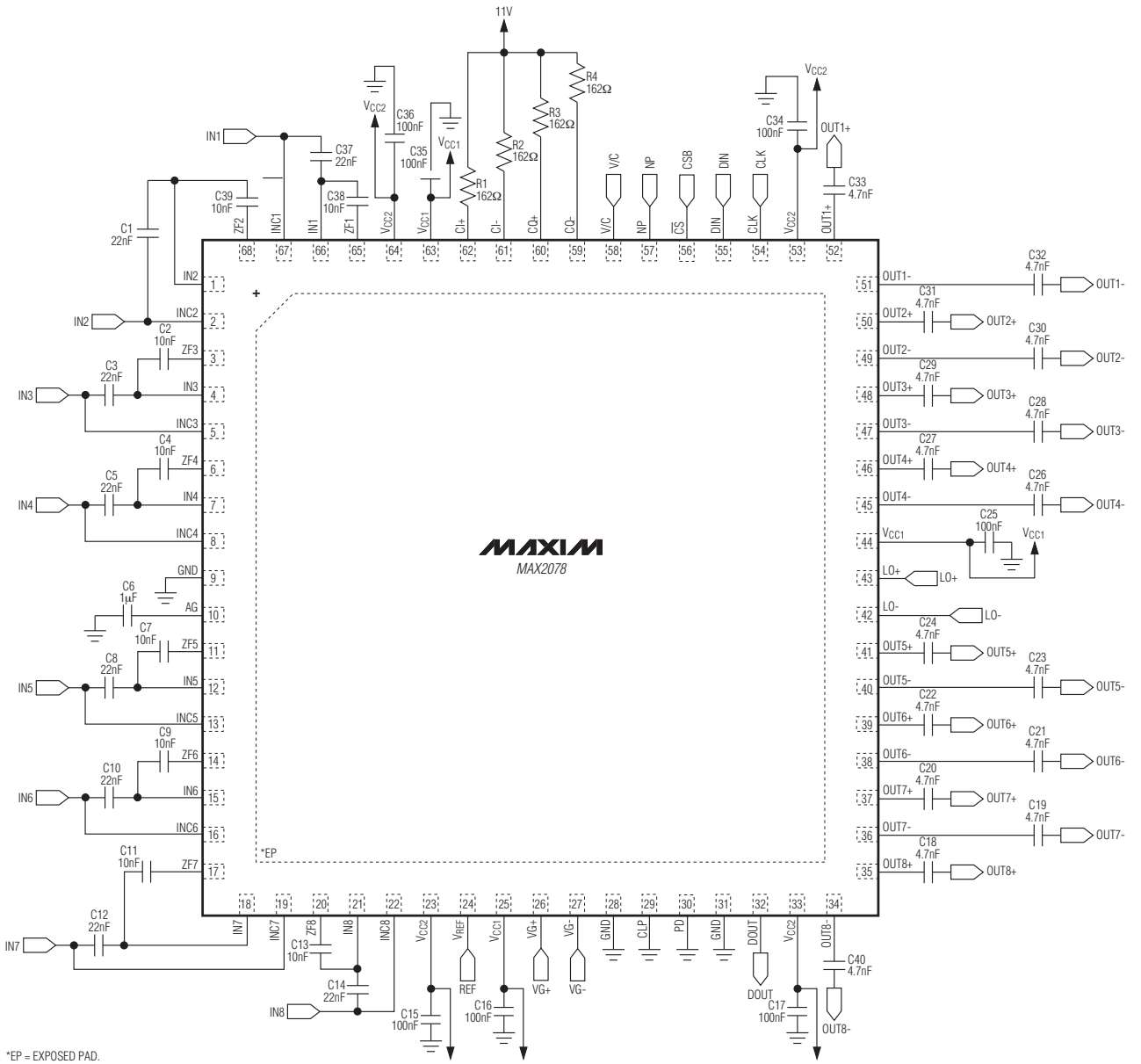
典型应用电路



芯片信息

PROCESS: Complementary BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局，请查询 **china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	文档编号
68引脚薄型QFN-EP	T6800+4	**21-0142**

8通道超声前端，提供CW多普勒混频器

修订历史

修订号	修订日期	说明	修改页
0	6/09	最初版本。	—
1	10/09	修正了两处小错误。	16, 24

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