19-4696; Rev 1; 9/09

MAXIM

八通道超声前端

概述

MAX2077八通道超声前端是完全集成的双极型、高密度、八通道超声接收器，优化用于低成本、多通道、高性能便携及车载超声系统。这款易于使用的IC允许用户以较小的空间和功耗实现高端2D和PW成像。结构紧凑的成像接收机包括低噪声放大器(LNA)、可变增益放大器(VGA)和抗混叠滤波器(AAF)，在$R_S = R_{IN} = 200\Omega$时具有2.4dB超低噪声系数，每通道功耗仅为64.8mW。完备的超声成像接收通道针对二次谐波成像进行优化，二次谐波失真仅为-64dBFS，可输出$1V_{P-P}$、5MHz信号，20dB增益下宽带SNR > 68dB*。双极型超声前端经过优化，可以获得优异的低速PW和流体多普勒彩超检测灵敏度，并在5MHz $1V_{P-P}$杂波输出、1kHz频偏下，具有140dBc/Hz的近载波SNR。

MAX2077八通道超声前端采用带有裸焊盘的小尺寸8mm x 8mm、56引脚薄型QFN封装或10mm x 10mm、68引脚薄型QFN封装，工作温度范围为0°C至+70°C。如需添加CW多普勒性能，可以用MAX2078替代MAX2077。

应用

医疗超声成像

声纳系统

引脚配置和典型应用电路在数据资料的最后给出。

特性

- 小尺寸8mm x 8mm、56引脚或10mm x 10mm、68引脚TQFN封装内集成了8通道LNA、VGA和AAF
- $R_{IN} = R_S = 200\Omega$时具有2.4dB超低通道噪声系数
- 5MHz、20dB增益下具有23nV/√Hz低输出参考噪声，68dB*宽带SNR，提供极佳的二次谐波成像
- 5MHz、$1V_{P-P}$输出信号、1kHz频偏，增益为20dB时，具有140dBc/Hz的近载波SNR，强杂波环境下能够提供出色的低速PW和流体多普勒彩超检测灵敏度
- 常规成像模式下，每通道(LNA、VGA以及AAF)具有64.8mW超低功耗
- 可选择有源输入阻抗匹配：50Ω、100Ω、200Ω和1kΩ
- 较宽的输入电压范围：高LNA增益模式下为$330mV_{P-P}$、低LNA增益模式下为$550mV_{P-P}$
- 集成可选择的3极点9MHz、10MHz、15MHz以及18MHz巴特沃斯AAF
- 快速恢复、低功耗模式(< 2µs)
- 与带CW多普勒混频器的MAX2078超声前端引脚兼容(MAX2077 68引脚封装器件)

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX2077CTN+	0°C to +70°C	56 Thin QFN-EP**
MAX2077CTK+	0°C to +70°C	68 Thin QFN-EP**

+表示无铅(Pb)/符合RoHS标准的封装。

***EP = 裸焊盘。*

**配合MAX1437B ADC使用。*

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to GND .....-0.3V to +5.5V
V_{CC2} - V_{CC1} .....> -0.3V
ZF_, IN_, AG to GND .....-0.3V to ($V_{CC\_}$ + 0.3V)
INC_ .....20mA DC
V_{REF} to GND .....-0.3V to +3V
IN_ to AG .....-0.6V to +0.6V
OUT_, DIN, DOUT, VG_, NP, $\overline{CS}$, CLK,
PD to GND .....-0.3V to (V_{CC1} + 0.3V)
$V_{CC\_}$, V_{REF} analog and digital control signals must be applied in this order
Input Differential Voltage .....2.0V_{P-P} differential

Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 47.6mW/°C above +70°C) 3.8W
68-Pin TQFN (derate 40.0mW/°C above +70°C) 4.0W
Operating Temperature Range (Note 1) .....0°C to +70°C
Junction Temperature .....+150°C
θ_{JC} (Notes 2, 3) (56-Pin TQFN) .....1°C/W
θ_{JC} (Notes 2, 3) (68-Pin TQFN) .....0.3°C/W
θ_{JA} (Notes 3, 4) (56-Pin TQFN) .....21°C/W
θ_{JA} (Notes 3, 4) (68-Pin TQFN) .....20°C/W
Storage Temperature Range .....-40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.
Note 2: Junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can only be used if the component is soldered down to a printed circuit board pad containing multiple ground vias to remove the heat. The junction temperature must not exceed 150°C.
Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maxim-ic.com/thermal-tutorial**.
Note 4: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$, assuming there is no heat removal from the exposed pad. The junction temperature must not exceed 150°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, no RF signals applied. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage	V_{CC1}		3.13	3.3	3.47	V
4.75V/5V Supply Voltage	V_{CC2}		4.5	4.75	5.25	V
External Reference Voltage Range	V_{REF}	(Note 6)	2.475		2.525	V
CMOS Input High Voltage	V_{IH}	Applies to CMOS control inputs	2.5			V
CMOS Input Low Voltage	V_{IL}	Applies to CMOS control inputs			0.8	V
CMOS Input Leakage Current	I_{IN}	0V to 3.3V			10	µA
Data Output High Voltage	DOUT_HI	10MΩ load		V_{CC1}		V
Data Output Low Voltage	DOUT_LO	10MΩ load		0		V
4.75V/5V Supply Standby Current	I_NP_5V_TOT	NP = 1, all channels		3.9	6	mA
3V Supply Standby Current	I_NP_3V_TOT	NP = 1, all channels		1.7	3	mA
4.75V/5V Power-Down Current	I_PD_5V_TOT	PD = 1, all channels (Note 7)		0.4	10	µA
3V Power-Down Current	I_PD_3V_TOT	PD = 1, all channels (Note 7)		0.3	10	µA
3V Supply Current per Channel	I_3V_NM	Total I divided by 8, VG+ - VG- = -2V		11	18	mA
4.75V/5V Supply Current per Channel	I_5V_NM	Total I divided by 8		6.0	8.3	mA
DC Power per Channel	P_NM			64.8	105	mW
Differential Analog Control Voltage Range	VGAIN_RANG	VG+ - VG-		±3		V

DC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, no RF signals applied. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Voltage for Difference Analog Control	VGAIN_COMM	(VG+ + VG-)/2		1.65 ±5%		V
Source/Sink Current for Gain Control Pins	I_ACONTROL	Per pin		±1.6	±4	µA
Reference Current	I_{REF}	All channels		9.7	13	µA
Output Common-Mode Level	V_{CMO}			1.73		V

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	D1/D0 = 0/0, R_{IN} = 50Ω, f_{RF} = 2MHz	47.5	50	60	Ω
	D1/D0 = 0/1, R_{IN} = 100Ω, f_{RF} = 2MHz	90	100	115	
	D1/D0 = 1/0, R_{IN} = 200Ω, f_{RF} = 2MHz	185	200	220	
	D1/D0 = 1/1, R_{IN} = 1000Ω, f_{RF} = 2MHz	600	830	1000	
Noise Figure	R_S = R_{IN} = 50Ω, LNA gain = 18.5dB, VG+ - VG- = +3V		4.5		dB
	R_S = R_{IN} =100Ω, LNA gain = 18.5dB, VG+ - VG- = +3V		3.4		
	R_S = R_{IN} = 200Ω, LNA gain = 18.5dB, VG+ - VG- = +3V		2.4		
	R_S = R_{IN} = 1000Ω, LNA gain = 18.5dB, VG+ - VG- = +3V		2.2		
Low-Gain Noise Figure	D3/D2/D1/D0 = 0/0/0/1, LNA gain = 12.5dB, R_S = R_{IN} = 200Ω, VG+ - VG- = +3V		3.9		dB
Input-Referred Noise Voltage	D3/D2/D1/D0 = 1/1/1/0		0.9		nV/√Hz
Input-Referred Noise Current	D3/D2/D1/D0 = 1/1/1/0		2.1		pA/√Hz
Maximum Gain, High Gain Setting	VG+ - VG- = +3V	41	42.4	45	dB
Minimum Gain, High Gain Setting	VG+ - VG- = -3V	9	10.1	12	dB
Maximum Gain, Low Gain Setting	D3/D2/D1/D0 = 0/0/0/1, R_{IN} = 200Ω, LNA gain = 12.5dB, VG+ - VG- = +3V	35	37.6	39	dB
Minimum Gain, Low Gain Setting	D3/D2/D1/D0 = 0/0/0/1, R_{IN} = 200Ω, LNA gain = 12.5dB, VG+ - VG- = -3V	3	5.4	8	dB
Anti-Aliasing Filter 3dB Corner Frequency	D5/D4 = 0/0, f_C = 9MHz		9		MHz
	D5/D4 = 0/1, f_C = 10MHz		10		
	D5/D4 = 1/0, f_C = 15MHz		15		
	D5/D4 = 1/1, f_C = 18MHz		18		
Gain Range	VG+ - VG- = -3V to +3V		33		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Gain Error	VG+ - VG- = -2V		±0.4		dB
	VG+ - VG- = 0V		±0.4		
	VG+ - VG- = +2V		±0.4		
Input Gain Compression	VG+ - VG- = -3V (VGA minimum gain), gain ratio with 330mV$_{P-P}$/50mV$_{P-P}$ input tones		1.4		dB
	LNA low gain = 12.5dB, VG+ - VG- = -3V (VGA minimum gain), gain ratio with 600mV$_{P-P}$/50mV$_{P-P}$		0.8		
VGA Gain Response Time	Gain step up (V_{IN} = 5mV$_{P-P}$, gain changed from 10dB to 44dB, settling time is measured within 1dB final value)		1.4		µs
	Gain step down (V_{IN} = 5mV$_{P-P}$, gain changed from 44dB to 10dB, settling time is measured within 1dB final value)		1.6		
VGA Output Offset Under Pulsed Overload	Overdrive is ±10mA in clamping diodes, gain at 30dB, 16 pulses at 5MHz, repetition rate 20kHz; offset is measured at output when RF duty cycle is off		180		mV
Small-Signal Output Noise	20dB of gain, VG+ - VG- = -0.85V, no input signal		23		nV/√Hz
Large-Signal Output Noise	20dB of gain, VG+ - VG- = -0.85V, f_{RF} = 5MHz, f_{NOISE} = f_{RF} + 1kHz, V_{OUT} = 1V$_{P-P}$ differential		35		nV/√Hz
Second Harmonic (HD2)	V_{IN} = 50mV$_{P-P}$, f_{RF} = 2MHz, V_{OUT} = 1V$_{P-P}$		-67		dBc
	V_{IN} = 50mV$_{P-P}$, f_{RF} = 5MHz, V_{OUT} = 1V$_{P-P}$		-64.2		
High-Gain IM3 Distortion	D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), V_{IN} = 50mV$_{P-P}$, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, V_{OUT} = 1V$_{P-P}$ (Note 8)	-52	-61		dBc
Low-Gain IM3 Distortion	D3/D2/D1/D0 = 0/0/0/1 (R_{IN} = 200Ω, LNA gain = 12.5dB), V_{IN} = 100mV$_{P-P}$, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, V_{OUT} = 1V$_{P-P}$ (Note 8)	-50	-60		dBc
Standby Mode Power-Up Response Time	Gain set for 26dB, f_{RF} = 5MHz, V_{OUT} = 1V$_{P-P}$, settled within 1dB from transition on NP pin		2.1		µs
Standby Mode Power-Down Response Time	To reach DC current target ±10%		2.0		µs
Power-Up Response Time	Gain set for 28dB, f_{RF} = 5MHz, V_{OUT} = 1V$_{P-P}$, settled within 1dB from transition on PD		2.7		ms
Power-Down Response Time	Gain set for 28dB, f_{RF} = 5MHz, DC power reaches 6mW/channel, from transition on PD		5		ns
Adjacent Channel Crosstalk	V_{OUT} = 1V$_{P-P}$ differential, f_{RF} = 10MHz, 28dB of gain		-58		dBc
Nonadjacent Channel Crosstalk	V_{OUT} = 1V$_{P-P}$ differential, f_{RF} = 10MHz, 28dB of gain		-71		dBc
Phase Matching Between Channels	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = 1V$_{P-P}$, f_{RF} = 10MHz		±1.2		Degrees

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3V Supply Modulation Ratio	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = 1V_{P-P}, f_{RF} = 5MHz, f_{MOD} = 1kHz, V_{MOD} = 50mV_{P-P}, ratio of output sideband at 5.001MHz, 1V_{P-P}		-73		dBc
4.75V/5V Supply Modulation Ratio	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = 1V_{P-P}, f_{RF} = 5MHz, f_{MOD} = 1kHz, V_{MOD} = 50mV_{P-P}, ratio of output sideband at 5.001MHz, 1V_{P-P}		-82		dBc
Gain Control Lines Common-Mode Rejection Ratio	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = 1V_{P-P}, f_{RF} = 5MHz, $f_{MOD(CM)}$ = 1kHz, $V_{MOD(CM)}$ = 50mV_{P-P}, ratio of output sideband at 5.001MHz to 1V_{P-P}		-74		dBc
Overdrive Phase Delay	VG+ - VG- = -3V, delay between V_{IN} = 300mV_{P-P} and V_{IN} = 30mV_{P-P} differential		5		ns
Output Impedance	Differential		100		Ω

AC ELECTRICAL CHARACTERISTICS—SERIAL PERIPHERAL INTERFACE

(DOUT loaded with 60pF and 10MΩ, 2ns rise and fall edges on CLK.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Speed					10	MHz
Mininimum Data-to-Clock Setup Time	t_{CS}			5		ns
Mininimum Data-to-Clock Hold Time	t_{CH}			0		ns
Mininimum Clock-to-$\overline{CS}$ Setup Time	t_{ES}			5		ns
$\overline{CS}$ Positive Mininimum Pulse Width	t_{EW}			1		ns
Mininimum Clock Pulse Width	t_{CW}			2		ns

Note 5: Minimum and maximum limits at T_A = +25°C and +70°C are guaranteed by design, characterization, and/or production test.

Note 6: Noise performance of the device is dependent on the noise contribution from V_{REF}. Use a low-noise supply for V_{REF}. The reference input noise is given for 8 channels, knowing that the reference-noise contributions are correlated in all 8 channels. If more channels are used, the reference noise must be reduced to get the best noise performance.

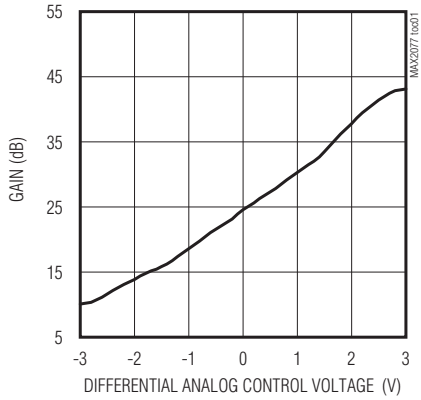
Note 7: Not applicable to the MAX2077CTK+.

Note 8: See the *Ultrasound-Specific IMD3 Specification* section.

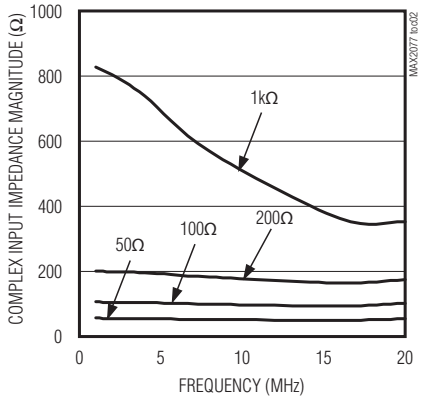
典型工作特性

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF, unless otherwise noted. All typical operating curves have been taken with the MAX2077CTN+ package variant.)

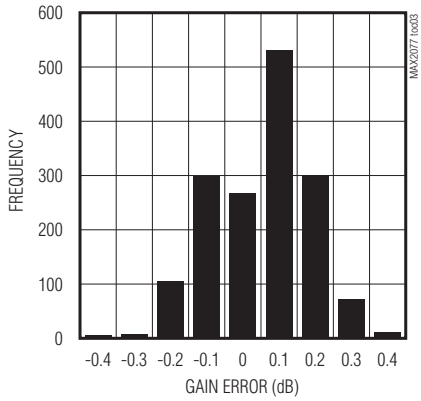
GAIN vs. DIFFERENTIAL ANALOG CONTROL VOLTAGE



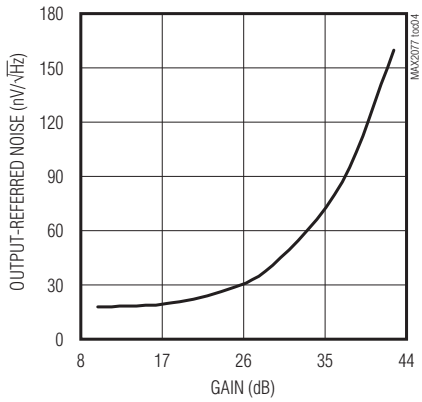
COMPLEX INPUT IMPEDANCE MAGNITUDE vs. FREQUENCY



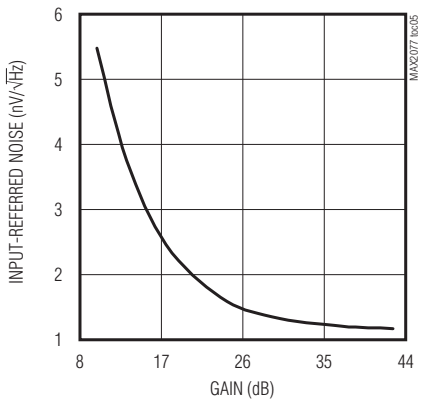
GAIN ERROR HISTOGRAM



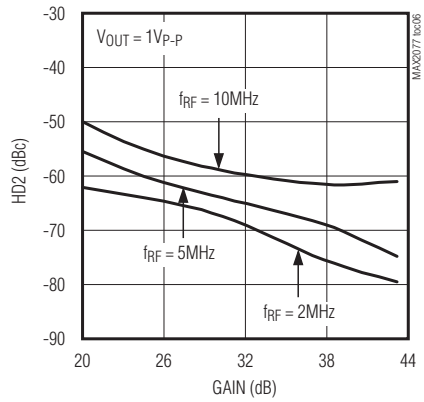
OUTPUT-REFERRED NOISE vs. GAIN



INPUT-REFERRED NOISE vs. GAIN



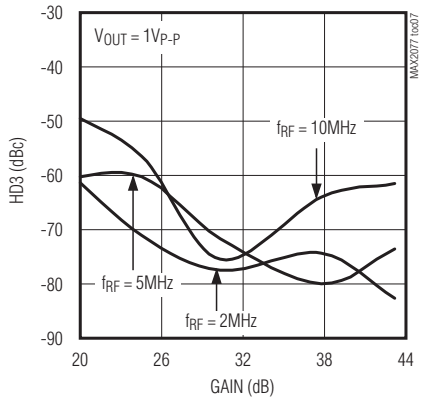
SECOND-HARMONIC DISTORTION vs. GAIN



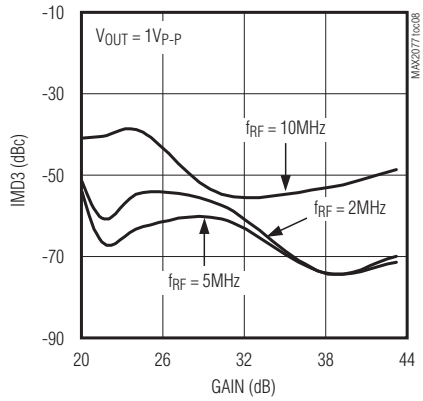
典型工作特性(续)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF, unless otherwise noted. All typical operating curves have been taken with the MAX2077CTN+ package variant.)

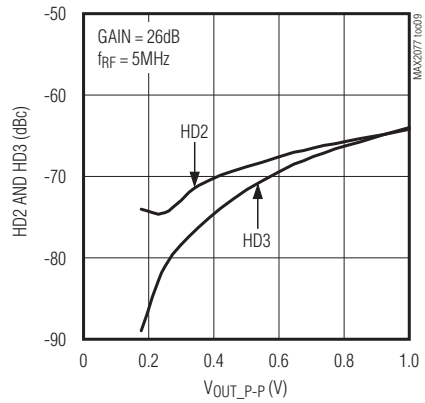
THIRD-HARMONIC DISTORTION vs. GAIN



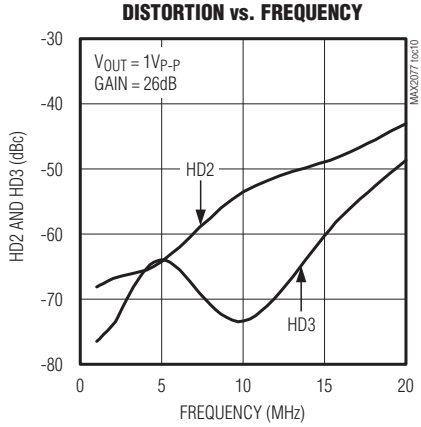
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. GAIN



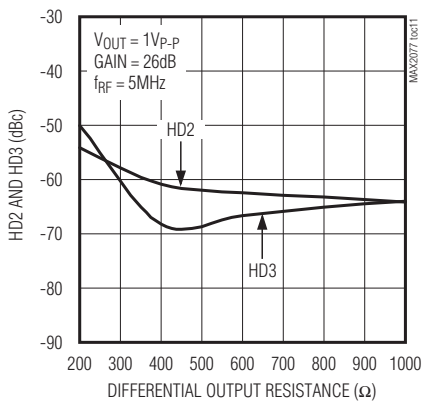
SECOND- AND THIRD-HARMONIC DISTORTION vs. V_{OUT_P-P}



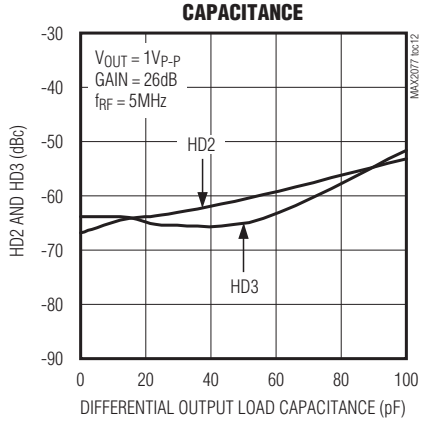
SECOND- AND THIRD-HARMONIC DISTORTION vs. FREQUENCY



SECOND- AND THIRD-HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT RESISTANCE



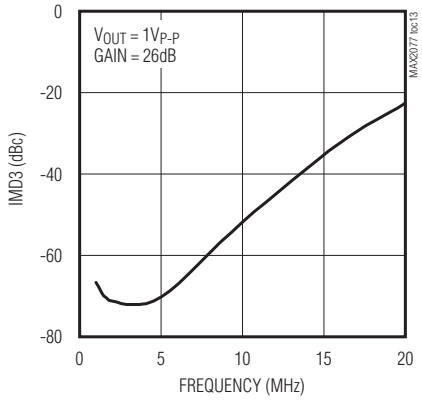
SECOND- AND THIRD-HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT LOAD CAPACITANCE



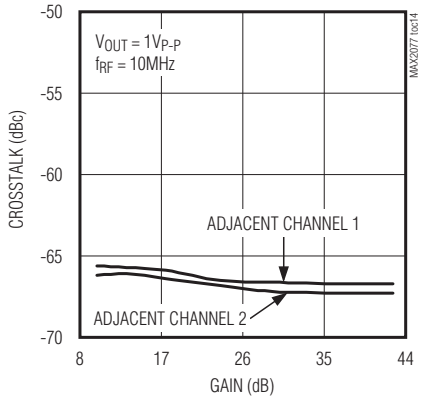
典型工作特性(续)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF, unless otherwise noted. All typical operating curves have been taken with the MAX2077CTN+ package variant.)

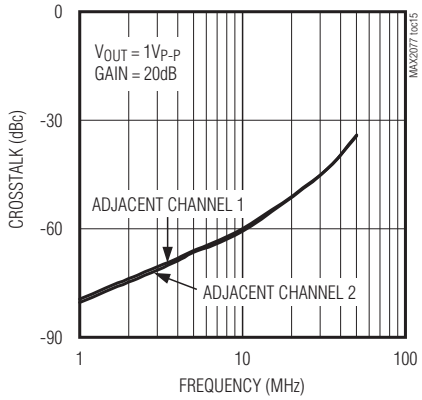
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. FREQUENCY



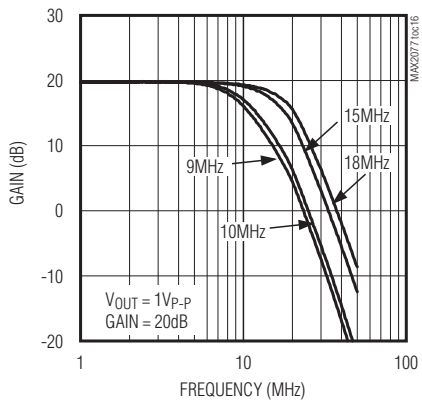
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN



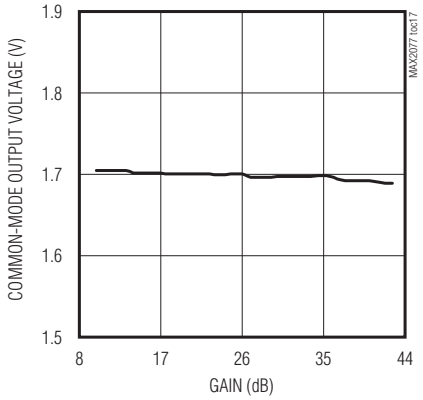
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



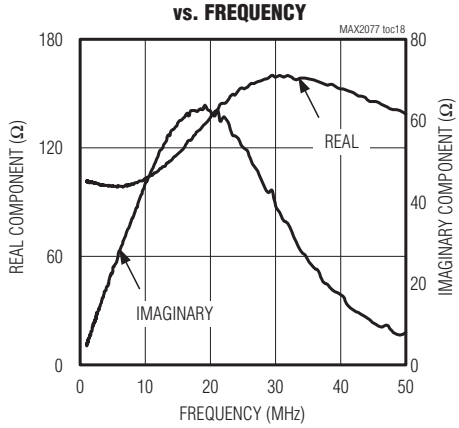
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY (GAIN = 20dB, V_{OUT} = 1V_{P-P})



COMMON-MODE OUTPUT VOLTAGE vs. GAIN



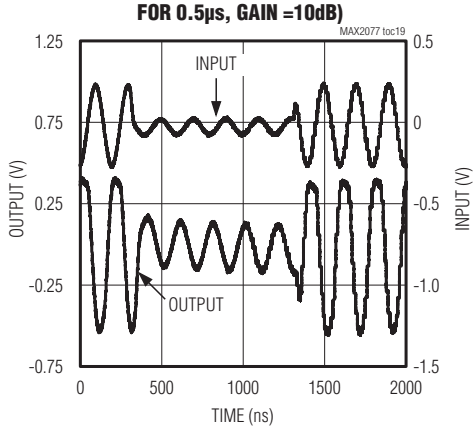
DIFFERENTIAL OUTPUT IMPEDANCE vs. FREQUENCY



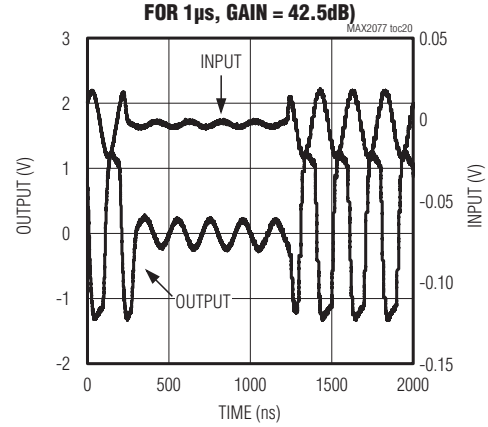
典型工作特性(续)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF, unless otherwise noted. All typical operating curves have been taken with the MAX2077CTN+ package variant.)

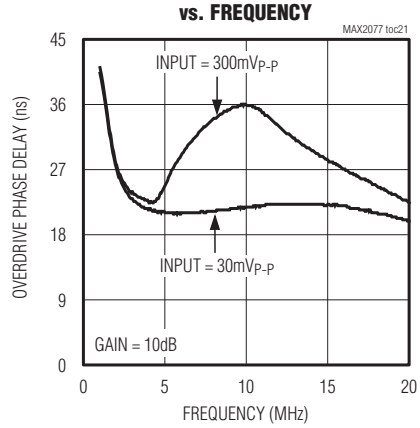
LNA OVERLOAD RECOVERY TIME (V_{IN} = 500mV$_{P-P}$ FOR 0.5µs TO 100mV$_{P-P}$ FOR 1µs AND BACK TO 500mV$_{P-P}$ FOR 0.5µs, GAIN =10dB)



VGA OVERLOAD RECOVERY TIME (V_{IN} = 40mV$_{P-P}$ FOR 1µs TO 4mV$_{P-P}$ FOR 1µs AND BACK TO 40mV$_{P-P}$ FOR 1µs, GAIN = 42.5dB)



OVERDRIVE PHASE DELAY vs. FREQUENCY



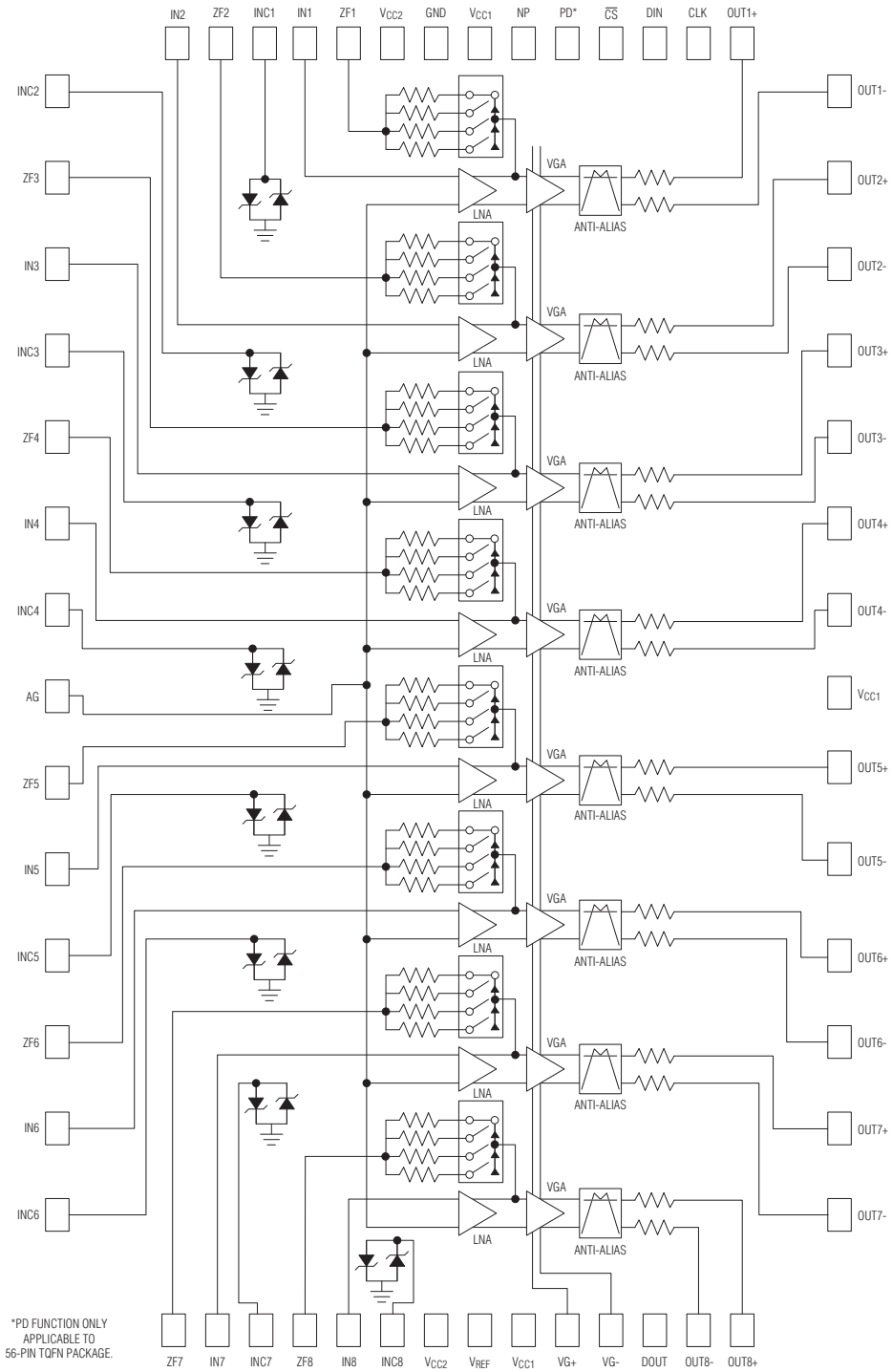
引脚说明

引脚		名称	功能
56 TQFN	68 TQFN		
1	2	INC2	通道2箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
2	3	ZF3	通道3有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
3	4	IN3	通道3输入。
4	5	INC3	通道3箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
5	6	ZF4	通道4有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
6	7	IN4	通道4输入。
7	8	INC4	通道4箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
8	10	AG	交流地，连接一个低ESR的1µF电容至地。
9	11	ZF5	通道5有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
10	12	IN5	通道5输入。
11	13	INC5	通道5箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
12	14	ZF6	通道6有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
13	15	IN6	通道6输入。
14	16	INC6	通道6箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
15	17	ZF7	通道7有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
16	18	IN7	通道7输入。
17	19	INC7	通道7箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
18	20	ZF8	通道8有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
19	21	IN8	通道8输入。
20	22	INC8	通道8箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
21, 51	23, 64	V_{CC2}	4.75V电源，连接至外部4.75V电源。在外部将所有4.75V电源引脚连接在一起，并尽量靠近引脚放置100nF旁路电容。
22	24	V_{REF}	外部2.5V基准电源，连接至低噪声电源。通过0.1µF电容旁路至GND，电容须靠近引脚放置。注意，器件噪声性能取决于V_{REF}端引入的噪声，使用在1kHz至20MHz范围内噪声低于5nV/√Hz电源。
23, 35, 49	25, 44, 63	V_{CC1}	3.3V电源，连接至外部3.3V电源。在外部将所有3.3V电源引脚连接在一起，并尽量靠近引脚放置100nF旁路电容。
24	26	VG+	VGA模拟增益控制差分输入。差分电压为-3V时对应于最小增益设置，+3V时对应于最大增益设置。
25	27	VG-	
26	32	DOUT	串口数据输出。数据输出简化了菊链配置，电平为3.3V CMOS。

引脚说明(续)

引脚		名称	功能
56 TQFN	68 TQFN		
27	34	OUT8-	通道8差分输出负端。
28	35	OUT8+	通道8差分输出正端。
29	36	OUT7-	通道7差分输出负端。
30	37	OUT7+	通道7差分输出正端。
31	38	OUT6-	通道6差分输出负端。
32	39	OUT6+	通道6差分输出正端。
33	40	OUT5-	通道5差分输出负端。
34	41	OUT5+	通道5差分输出正端。
36	45	OUT4-	通道4差分输出负端。
37	46	OUT4+	通道4差分输出正端。
38	47	OUT3-	通道3差分输出负端。
39	48	OUT3+	通道3差分输出正端。
40	49	OUT2-	通道2差分输出负端。
41	50	OUT2+	通道2差分输出正端。
42	51	OUT1-	通道1差分输出负端。
43	52	OUT1+	通道1差分输出正端。
44	54	CLK	串口时钟输入(上升沿触发)，3.3V CMOS。时钟输入用于编程串行移位寄存器。
45	55	DIN	串口数据输入，3.3V CMOS。数据输入用于编程串行移位寄存器。
46	56	$\overline{CS}$	低电平有效的串口片选输入，3.3V CMOS。用于存储寄存器的设置位，并在CW模式下同步所有通道的相位(上升沿)。
47	—	PD	关断模式选择输入(56引脚TQFN)。PD置于高电平时，整个器件进入关断模式；PD置于低电平时正常工作。该模式的设置权限高于待机模式。
48	57	NP	VGA待机模式选择输入。NP置于1时，整个器件进入待机模式。该模式设置权限高于串行移位寄存器中的通道软关断设置，但优先级低于通用断电(PD)模式设置。
50	9, 28, 31	GND	地。
52	65	ZF1	通道1有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
53	66	IN1	通道1输入。
54	67	INC1	通道1箝位输入，连接至耦合电容，详细说明请参考*典型应用电路*。
55	68	ZF2	通道2有源阻抗匹配引脚，通过10nF电容交流耦合至源端。
56	1	IN2	通道2输入。
—	29, 30, 33, 42, 43, 53, 58–62	N.C.	无连接，内部没有连接。
—	—	EP	裸焊盘，内部连接至地。通过多个过孔连接至大面积地平面，以改善散热和电气特性。不要将其作为电气连接点。

功能框图


IN2
ZF2
INC1
IN1
ZF1
VCC2
GND
VCC1
NP
PD*
CS
DIN
CLK
OUT1+
INC2
ZF3
IN3
INC3
ZF4
IN4
INC4
AG
ZF5
IN5
INC5
ZF6
IN6
INC6
VGA
LNA
ANTI-ALIAS
OUT1-
OUT2+
OUT2-
OUT3+
OUT3-
OUT4+
OUT4-
VCC1
OUT5+
OUT5-
OUT6+
OUT6-
OUT7+
OUT7-
*PD FUNCTION ONLY APPLICABLE TO 56-PIN TQFN PACKAGE.
ZF7
IN7
INC7
ZF8
IN8
INC8
VCC2
VREF
VCC1
VG+
VG-
DOUT
OUT8-
OUT8+

详细说明

MAX2077是高密度、8通道超声接收器，优化用于低成本、多通道、高性能便携式和车载超声应用。集成8通道LNA、VGA、AAF提供完整的超声成像接收方案。

成像通道动态范围经过优化，具有优异的二次谐波性能。整个成像接收通道在5MHz具有出色的68dBFS* SNR。双极型超声前端经过优化，其极低的近载波调制噪声在高杂波环境中可以提供优异的低速PW和流体多普勒彩超检测灵敏度，并在V_{OUT} = $1V_{P-P}$、5MHz杂波输出、1kHz频偏下，具有140dBc/Hz的近载波SNR。如需添加CW多普勒功能，请选择MAX2078替代MAX2077。

*配合MAX1437B ADC使用。

工作模式

MAX2077需要在使用之前进行编程。工作模式由D0至D6设置位进行控制，表1和表2给出了这些设置位的功能。

低噪声放大器(LNA)

MAX2077的LNA经过优化，具有优异的动态范围和线性指标，可理想用于超声成像应用。当LNA工作在低增益模式，输入电阻(R_{IN})为增益A的函数(R_{IN} = R_F/(1+A))，增大至原来的2倍。因此，控制反馈电阻(R_F)的开关必须改变。例如，高增益模式下100Ω的电阻在低增益模式下将变为200Ω (参见表2)。

表1. 设置位总结

BIT NAME	DESCRIPTION
D0, D1, D2	Input-impedance programming
D3	LNA gain (D3 = 0 is low gain)
D4, D5	Anti-alias filter f_C programming
D6	Don't care

表2. 设置位的逻辑功能

D6	D5	D4	D3	D2	D1	D0	MODE
X	X	X	1	0	0	0	R_{IN} = 50Ω, LNA gain = 18.5dB
X	X	X	1	0	0	1	R_{IN} = 100Ω
X	X	X	1	0	1	0	R_{IN} = 200Ω
X	X	X	1	0	1	1	R_{IN} = 1000Ω
X	X	X	0	0	0	0	R_{IN} = 100Ω, LNA gain = 12.5dB
X	X	X	0	0	0	1	R_{IN} = 200Ω
X	X	X	0	0	1	0	R_{IN} = 400Ω
X	X	X	0	0	1	1	R_{IN} = 2000Ω
X	X	X	1	1	X	X	Open feedback, LNA gain = 18.5dB
X	0	0	X	X	X	X	f_C = 9MHz
X	0	1	X	X	X	X	f_C = 10MHz
X	1	0	X	X	X	X	f_C = 15MHz
X	1	1	X	X	X	X	f_C = 18MHz

X = 无关。

可变增益放大器(VGA)

MAX2077的VGA优化于高线性度、高动态范围和低输出噪声，这些性能都是超声成像应用的关键参数。每个VGA通路包含模拟增益调节电路，以及带差分输出端口(OUT_+、OUT_-)的输出缓冲器，用于驱动ADC。

VGA增益可以通过差分增益控制输入VG+和VG-调节。差分增益控制输入电压为-3V时对应于最小增益，+3V时对应于最大增益。差分模拟控制共模电压为1.65V (典型值)。

过载恢复

器件经过优化设计具有快速过载恢复功能，非常适合具有较大输入信号的典型成像系统，请参考*典型工作特性*中关于瞬态过载的快速恢复时间示意图。

关断模式

MAX2077CTN+也可以通过PD引脚控制置于关断模式(MAX2077CTK+不具备类似功能)，PD置为逻辑高电平时器件进入关断模式，关断模式下器件仅消耗3.0µW (典型值)功率。PD置为逻辑低电平时，器件正常工作。

将NP置于逻辑高电平，使MAX2077进入待机模式。待机模式下，器件消耗较低功率(5.6mW，典型值)，输入/输出端保持其偏置电压，以便快速响应上电。MAX2077CTN+和MAX2077CTK+产品均具有待机模式。

应用信息

串口

MAX2077通过串行移位寄存器进行编程设置。这种方式大大简化了编程电路的复杂度，减少了编程所需的IC引脚，并降低了PCB布局的复杂度。数据输入(DIN)和数据输出(DOUT)可以构建逐个器件的菊链，所有前端工作在同一编程时钟下。

$\overline{CS}$拉至低电平时装载数据，整个字装载完毕后，需要将$\overline{CS}$拉至高电平。器件编程时，LSB在前、MSB在后。片选信号($\overline{CS}$)可同时装载多片MAX2077的设置信息。开始编程前，将片选信号拉低，完成所有器件的编程后将其拉高。在片选信号的上升沿将设置信息储存到内部寄存器。

有源阻抗匹配

为提供优异的噪声系数指标，每个放大器的输入阻抗均采用反馈拓扑，实现有源阻抗匹配。在放大器的反相输入与输出之间增加阻值为(1 + (A/2)) x R_S的反馈电阻。输入阻抗为反馈电阻(Z_F)除以1 + (A/2)。系数2源于定义差分输出的放大器增益(A)。对于共模输入阻抗，可以使用内部数字编程阻抗(参见表2)。对于其它输入阻抗，设置与当前可编程反馈电阻串联的外部电阻，按照上述公式设置输入阻抗。

噪声系数

MAX2077设计用于提供最高输入灵敏度和优异的低噪声系数。选择输入有源器件保持极低的等效输入噪声电压和电流，针对50Ω至1000Ω源阻抗优化。另外，匹配电阻引入的噪声将被衰减1 + (A/2)倍。采用这种结构，放大器的典型噪声系数在$R_{IN} = R_S = 200Ω$时可以达到大约2.4dB，表3给出了其它输入阻抗下的噪声系数。

输入箝位

MAX2077集成了可配置的输入箝位二极管，二极管箝位至地电位的±0.8V。输入箝位二极管可以避免大的瞬态信号过驱动放大器输入。输入过驱动可能对输入耦合电容充电，造成较长的过载恢复时间。输入信号交流耦合至单端输入IN1至IN8，但INC1至INC8输入具有箝位，参见*典型应用电路*。如果选择外部箝位器件，可以将INC1至INC8浮空。

表3. 噪声系数与源阻抗和输入阻抗

R_S (Ω)	R_{IN} (Ω)	NF (dB)
50	50	4.5
100	100	3.4
200	200	2.4
1000	1000	2.2

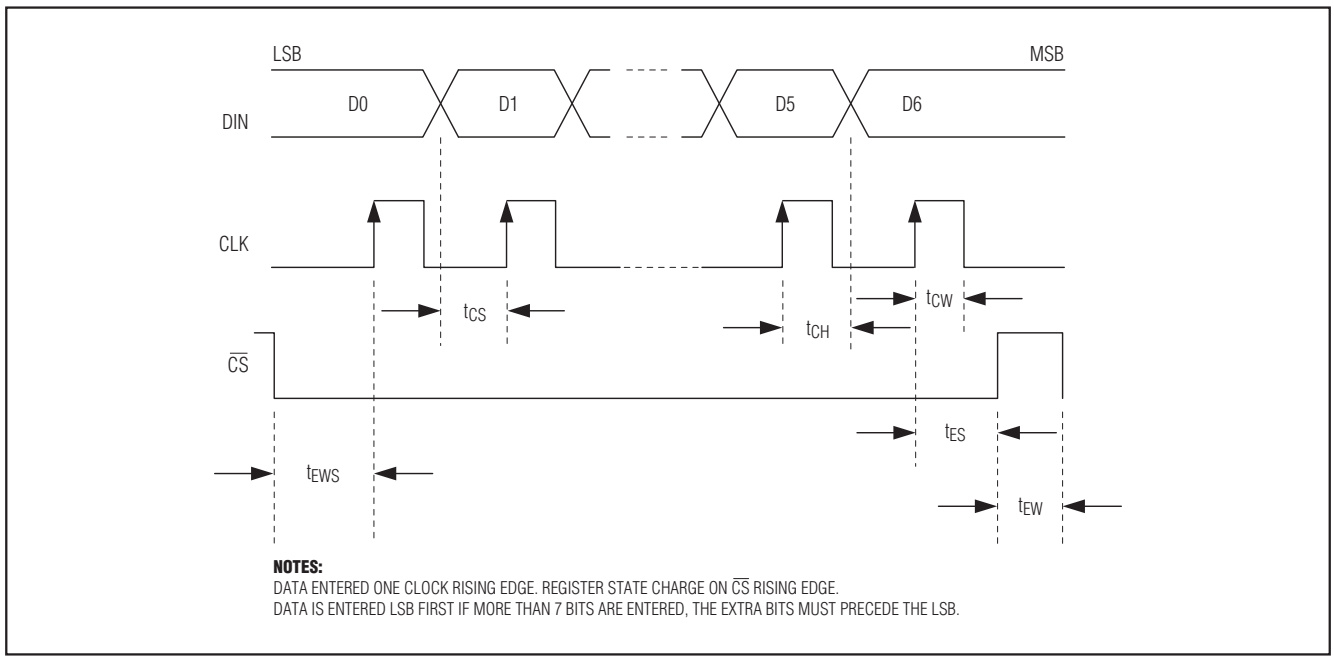


图1. 移位寄存器时序图

模拟输出耦合

每组VGA差分输出引脚可以驱动连接在各个输出端至GND之间的25pF负载以及15pF ‖ 1kΩ的差分负载(连接在引脚之间)。差分输出具有大约1.73V的共模偏置，如果下一级电路具有不同的共模输入范围，则对这些差分输出采用交流耦合。

电源排序

按照以下顺序上电：

1) 4.75V电源

2) 3.3V电源

3) 2.5V基准电压

4) 控制信号

信号接通之前应处于0V或开路状态。

超声规范定义的IMD3

与典型的通信规范不同，超声规范定义的双音IMD3指标对应的两个输入音具有不同的幅度。测试中，f_1代表肌肉等组织的反射波，f_2代表血液的反射波。后者一般比前者的幅度低25dB，所以这种测量方式中，双音输入的其中一个比另一个低25dB。在超声应用中，IMD3指标(f_1 - (f_2 - f_1))表现为不希望出现的多普勒误差信号(见图2)。

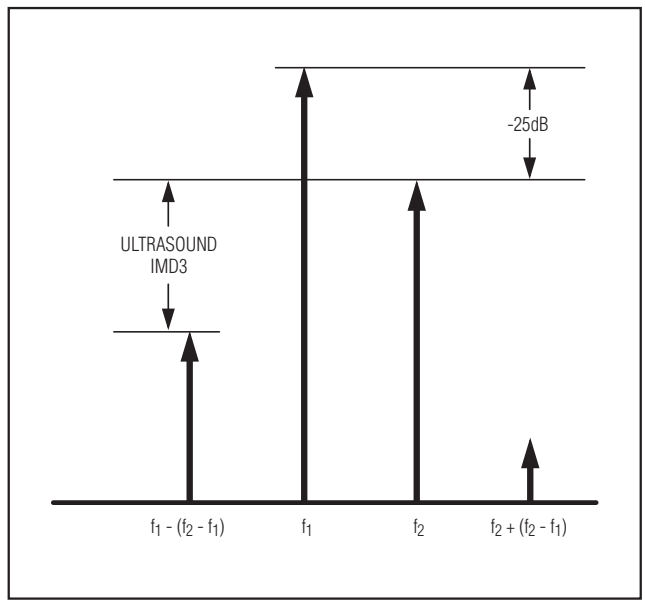


图2. 超声IMD3测量方法

八通道超声前端

PCB布局

MAX2077的引脚配置经过优化后，能够很方便地与相关分立元件连接，实现紧凑的物理布局。通常，该器件与几个器件一起构成多通道信号处理系统。

MAX2077采用TQFN-EP封装，其裸焊盘(EP)提供了一个与管芯之间的低热阻通道。设计PCB时，借助MAX2077的裸焊盘散热非常重要。此外，将裸焊盘通过一个低电感路径连接至电气地。裸焊盘**必须**直接或通过一系列电镀过孔焊接至PCB的地层。

芯片信息

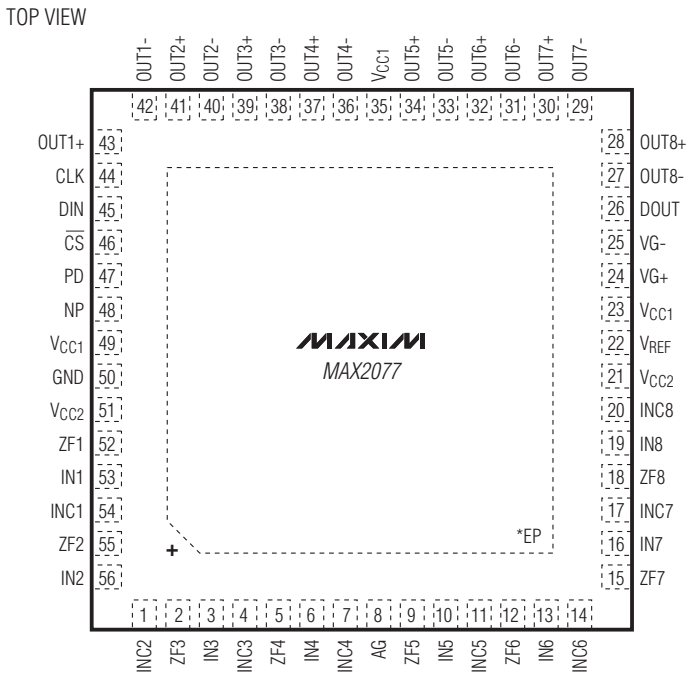
PROCESS: Complementary BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局，请查询 **china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

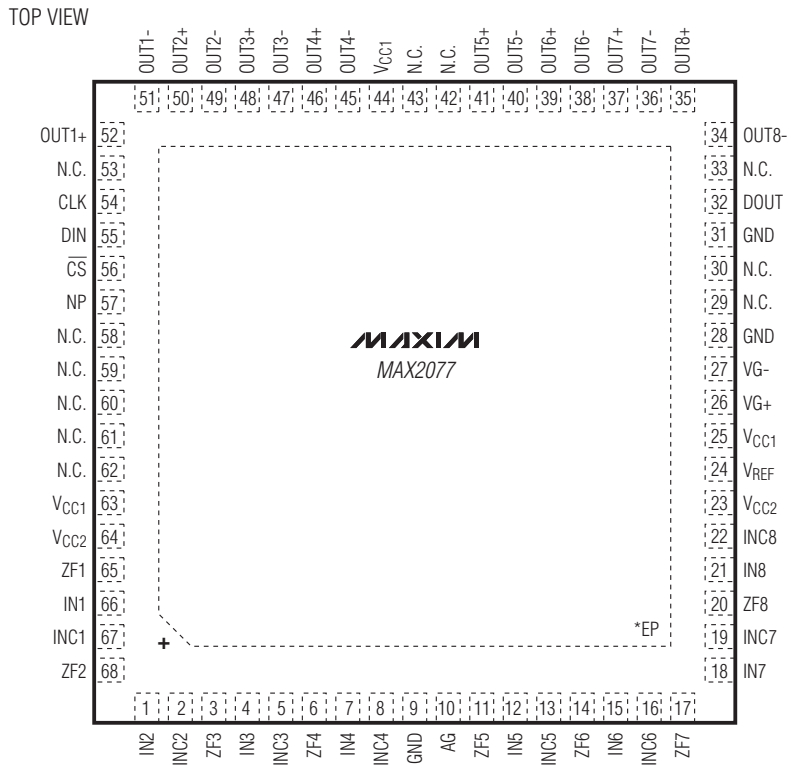
封装类型	封装编码	文档编号
56 TQFN-EP	T5688+2	21-0135
68 TQFN-EP	T6800+2	21-0142

引脚配置



TQFN
(8mm × 8mm)

*EP = EXPOSED PAD.

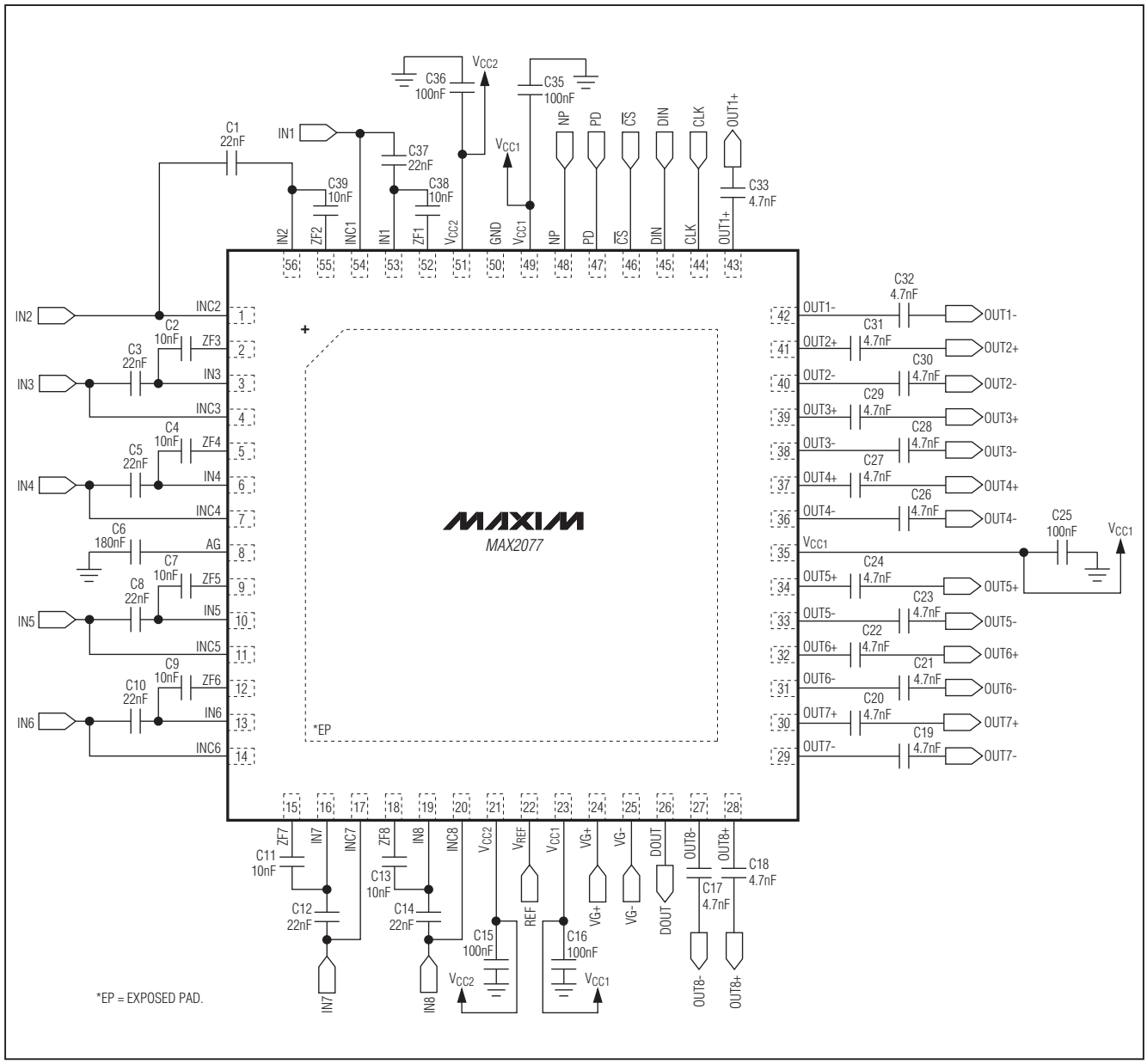


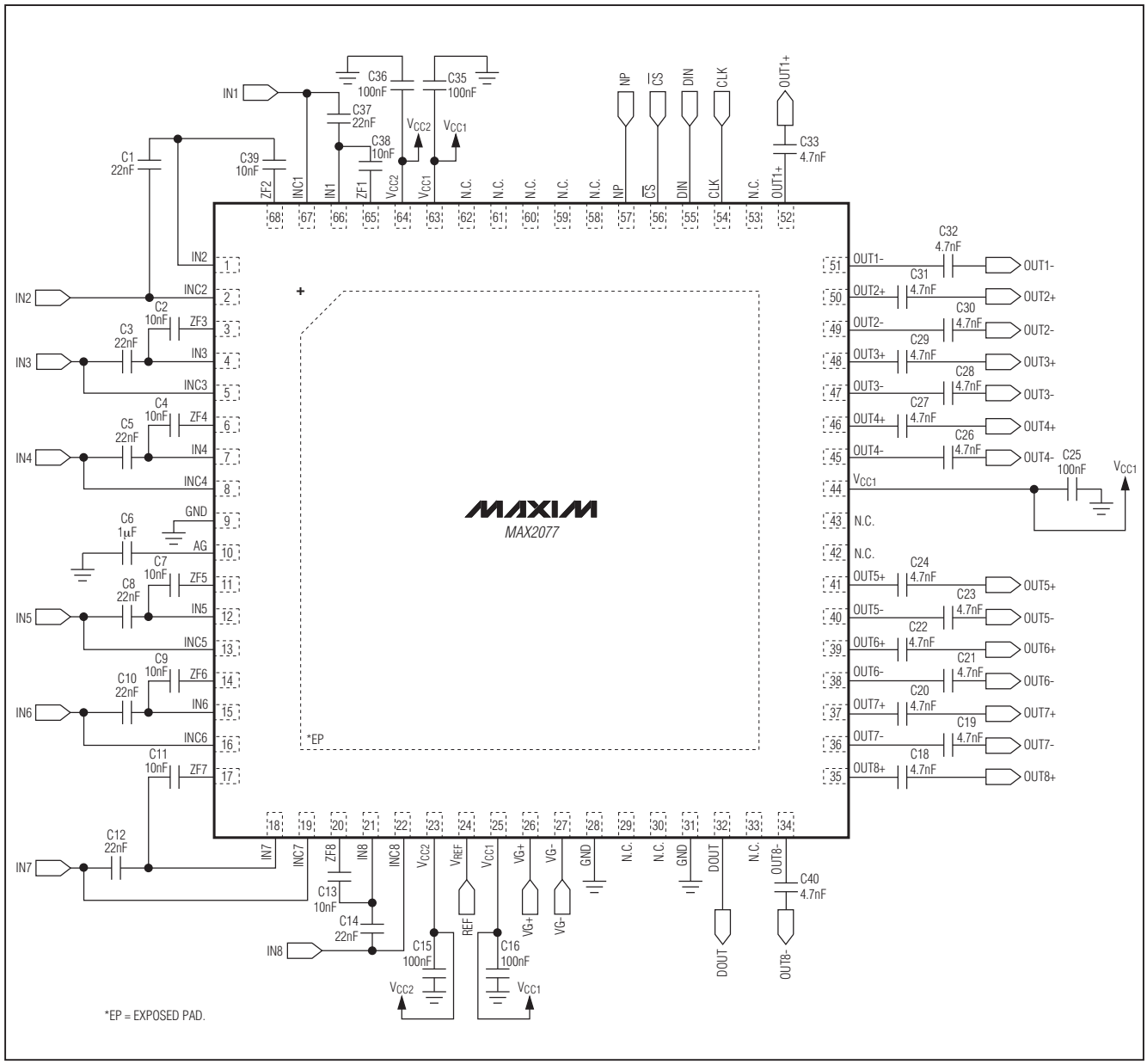
TQFN
(10mm × 10mm)

*EP = EXPOSED PAD.

八通道超声前端

典型应用电路




MAX2077
*EP
*EP = EXPOSED PAD.
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
C1 22nF
C2 10nF
C3 22nF
C4 10nF
C5 22nF
C6 1µF
C7 10nF
C8 22nF
C9 10nF
C10 22nF
C11 10nF
C12 22nF
C13 10nF
C14 22nF
C15 100nF
C16 100nF
C25 100nF
C32 4.7nF
C31 4.7nF
C30 4.7nF
C29 4.7nF
C28 4.7nF
C27 4.7nF
C26 4.7nF
C24 4.7nF
C23 4.7nF
C22 4.7nF
C21 4.7nF
C20 4.7nF
C19 4.7nF
C18 4.7nF
C33 4.7nF
C40 4.7nF
C35 100nF
C36 100nF
C37 22nF
C38 10nF
C39 10nF
VCC1
VCC2
GND
AG
VREF
VG+
VG-
DOUT
NP
CS
DIN
CLK
OUT1+
OUT1-
OUT2+
OUT2-
OUT3+
OUT3-
OUT4+
OUT4-
OUT5+
OUT5-
OUT6+
OUT6-
OUT7+
OUT7-
OUT8+
OUT8-
N.C.

修订历史

修订号	修订日期	说明	修改页
0	7/09	最初版本。	—
1	9/09	删除了MAX2077CTK+的未来产品说明，并做了一些细微的修改。	1, 6–9, 12

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