19-5618; Rev 0; 12/10

50MHz至1000MHz、高线性度、串行/模拟控制VGA

概述

MAX2064为高线性度、双通道模拟调节可变增益放大器(VGA)，工作在50MHz至1000MHz频率范围。每路模拟衰减器可由外部电压控制，或者通过SPI™兼容接口利用片上8位DAC控制。

因为每一级电路都具有RF输入和RF输出，通过适当配置可以优化噪声系数(放大器第一级)或OIP3（放大器最后一级)。该器件还包含具有24dB增益的放大器(放大器本身)，增益最大时，噪声系数(NF)为4.4dB（包括衰减器的插入损耗)，具有高达+41dBm的OIP3。这些特性使得该器件成为多通道接收器和发射器应用的理想VGA选择。

此外，器件采用+5V单电源供电时具有最佳性能；工作在+3.3V单电源时，将启有先进的省电模式，但性能指标略有降低。器件采用紧凑、带裸焊盘的48引脚、TQFN封装(7mm x 7mm)，在扩展级温度范围(T_C = -40°C至+85°C)内工作时确保电气特性。

应用

IF和RF增益级设计

温度补偿电路

WCDMA、TD-SCDMA和cdma2000®基站

GSM 850/GSM 900 EDGE基站

WiMAX™、LTE和TD-LTE基站及用户端设备

固定宽带无线接入

无线本地环路

军用系统

特性

- 可独立控制两个通道
- 50MHz至1000MHz RF频率范围
- 引脚兼容产品:
  - MAX2062 (模拟/数字VGA)
  - MAX2063 (数字VGA)
- 22dB (典型值)最大增益
- 100MHz带宽内保持0.19dB的增益平坦度
- 33dB增益范围
- 49dB通道隔离(200MHz频率)
- 片内8位DAC用于模拟衰减控制
- 200MHz时具有优异的线性特性(放大器最后一级)
  - +41dBm OIP3
  - +59dBm OIP2
  - 输出1dB压缩点为+19dBm
- 4.4dB典型噪声系数(200MHz频率)
- +5V单电源供电(可选择+3.3V供电)
- 放大器关断模式支持TDD应用

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX2064ETM+	-40°C to +85°C	48 TQFN-EP*
MAX2064ETM+T	-40°C to +85°C	48 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*
T = 卷带包装。

SPI是Motorola, Inc.的商标。
cdma2000是电信工业协会的注册认证标志和注册服务标志。
WiMAX是WiMAX论坛的注册认证标志和注册服务标志。

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有关价格、供货及订购信息，请联络Maxim亚洲销售中心：10800 852 1249 (北中国区)，10800 152 1249 (南中国区)，或访问Maxim的中文网站：china.maxim-ic.com。

50MHz至1000MHz、高线性度、串行/模拟控制VGA

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_AMP\_1}$, $V_{CC\_AMP\_2}$, V_{CC_RG} to GND .....-0.3V to +5.5V
PD_1, PD_2, AMPSET to GND .....-0.3V to +3.6V
A_VCTL_1, A_VCTL_2 to GND.....-0.3V to +3.6V
DAT, $\overline{CS}$, CLK, AA_SP to GND .....-0.3V to +3.6V
AMP_IN_1, AMP_IN_2 to GND.....+0.95V to +1.2V
AMP_OUT_1, AMP_OUT_2 to GND .....-0.3V to +5.5V
A_ATT_IN_1, A_ATT_IN_2, A_ATT_OUT_1, A_ATT_OUT_2 to GND .....0V to +3.6V
REG_OUT to GND.....-0.3V to +3.6V
RF Input Power (A_ATT_IN_1, A_ATT_IN_2)..... +20dBm
RF Input Power (AMP_IN_1, AMP_IN_2)..... +18dBm
θ_{JC} (Notes 1, 2)..... +12.3°C/W
θ_{JA} (Notes 2, 3)..... +38°C/W
Continuous Power Dissipation (Note 1) 5.3W
Operating Case Temperature Range (Note 4) .. -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maxim-ic.com/thermal-tutorial**.

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = +4.75V to +5.25V, AMPSET = 0, PD_1 = PD_2 = 0, T_C = -40°C to +85°C. Typical values are at $V_{CC\_}$ = +5.0V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{DC}			143	210	mA
Power-Down Current	I_{DCPD}	PD_1 = PD_2 = 1, V_{IH} = 3.3V		5.3	8	mA
Input Low Voltage	V_{IL}				0.5	V
Input High Voltage	V_{IH}		1.7		3.465	V
Input Logic Current	I_{IH}, I_{IL}		-1		+1	µA

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = +3.135V to +3.465V, AMPSET = 1, PD_1 = PD_2 = 0, T_C = -40°C to +85°C. Typical values are at $V_{CC\_}$ = +3.3V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.135	3.3	3.465	V
Supply Current	I_{DC}			84.7	145	mA
Power-Down Current	I_{DCPD}	PD_1 = PD_2 = 1, V_{IH} = 3.3V		4.5	8	mA
Input Low Voltage	V_{IL}			0.5		V
Input High Voltage	V_{IH}			1.7		V

RECOMMENDED AC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}	(Note 5)	50		1000	MHz

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (each path, unless otherwise noted)

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +4.75V to +5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, V_{CC} = +5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Gain	G	f_{RF} = 50MHz		22.4		dB
		f_{RF} = 100MHz		22.3		
		f_{RF} = 200MHz		22.2		
		f_{RF} = 350MHz, T_C = +25°C	19.5	21.9	23.5	
		f_{RF} = 450MHz		21.7		
		f_{RF} = 750MHz		21.4		
		f_{RF} = 900MHz		20.6		
Gain vs. Temperature				-0.006		dB/°C
Gain Flatness vs. Frequency		From 100MHz to 200MHz		0.18		dB
		Any 100MHz frequency band from 200MHz to 500MHz		0.19		
Noise Figure	NF	f_{RF} = 50MHz		4.4		dB
		f_{RF} = 100MHz		4.4		
		f_{RF} = 200MHz		4.4		
		f_{RF} = 350MHz		4.6		
		f_{RF} = 450MHz		4.7		
		f_{RF} = 750MHz		5.3		
		f_{RF} = 900MHz		5.7		
Total Attenuation Range		f_{RF} = 350MHz, T_C = +25°C	30	32.9		dB
Output Second-Order Intercept Point	OIP2	P_{OUT} = 0dBm/tone, Δf = 1MHz, $f_1 + f_2$		53.7		dBm
Path Isolation		RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω		48.7		dB
		RF input 2 amplified signal measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω		48.6		
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 50MHz		46.3		dBm
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 100MHz		44.2		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 200MHz		41.1		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 350MHz		37.1		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 450MHz		34.9		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 750MHz		28.2		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 900MHz		24.6		

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (each path, unless otherwise noted) (continued)

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +4.75V to +5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, V_{CC} = +5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output -1dB Compression Point	P_{1dB}	f_{RF} = 350MHz, T_C = +25°C (Note 7)		17	18.7		dBm
Second Harmonic		P_{OUT} = +3dBm			-56.7		dBc
Third Harmonic		P_{OUT} = +3dBm			-72.4		dBc
Group Delay		Includes EV kit PCB delays			0.9		ns
Amplifier Power-Down Time		PD_1 or PD_2 from 0 to 1, amplifier DC supply current settles to within 0.1mA			0.5		µs
Amplifier Power-Up Time		PD_1 or PD_2 from 1 to 0, amplifier DC supply current settles to within 1%			0.5		µs
Input Return Loss	RL_{IN}	50Ω source			16.8		dB
Output Return Loss	RL_{OUT}	50Ω load			30.7		dB
ANALOG ATTENUATOR (each path, unless otherwise noted)							
Insertion Loss	IL				2.2		dB
Input Second-Order Intercept Point	IIP2	P_{IN1} = 0dBm, P_{IN2} = 0dBm (minimum attenuation), Δf = 1MHz, $f_1 + f_2$			61.9		dBm
Input Third-Order Intercept Point	IIP3	P_{IN1} = 0dBm, P_{IN2} = 0dBm (minimum attenuation), Δf = 1MHz			37.0		dBm
Attenuation Range					32.9		dB
Gain Control Slope		Analog control input			-13.3		dB/V
Maximum Gain Control Slope		Over analog control input range			-35.2		dB/V
Insertion Phase Change		Over analog control input range			16.5		Deg/V
Attenuator Response Time		RF settled to within ±0.5dB	31dB to 0dB, AA_SP = 0, from A_VCTL_ step		500		ns
			31dB to 0dB, AA_SP = 1, from $\overline{CS}$ step		500		
			0dB to 31dB, AA_SP = 0, from A_VCTL_ step		500		
			0dB to 31dB, AA_SP = 1, from $\overline{CS}$ step		500		
Group Delay vs. Control Voltage		Over analog control input from 0.25V to 2.75V			-0.26		ns
Analog Control Input Range				0.25		2.75	V
Analog Control Input Impedance					19.2		kΩ
Input Return Loss		50Ω source			16.0		dB
Output Return Loss		50Ω load			15.9		dB

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (each path, unless otherwise noted) (continued)

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +4.75V to +5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, V_{CC} = +5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D/A CONVERTER						
Number of Bits				8		Bits
Output Voltage		DAC code = 00000000			0.35	V
		DAC code = 11111111	2.7			
SERIAL PERIPHERAL INTERFACE (SPI)						
Maximum Clock Speed				20		MHz
Data-to-Clock Setup Time	t_{CS}			2		ns
Data-to-Clock Hold Time	t_{CH}			2.5		ns
Clock-to-$\overline{CS}$ Setup Time	t_{ES}			3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}			7		ns
$\overline{CS}$ Setup Time	t_{EWS}			3.5		ns
Clock Pulse Width	t_{CW}			5		ns

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS (each path, unless otherwise noted)

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +3.135V to +3.465V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, V_{CC} = +3.3V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Gain	G			21.8		dB
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone		29.1		dBm
Noise Figure	NF			4.8		dB
Total Attenuation Range				32.9		dB
Path Isolation		RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω		48.1		dB
		RF input 2 amplified signal measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω		48.2		
Output -1dB Compression Point	P_{1dB}	(Note 7)		13.2		dBm

Note 5: Operation outside this range is possible, but with degraded performance of some parameters. See the *Typical Operating Characteristics*.

Note 6: All limits include external component losses. Output measurements are performed at the RF output port of the *Typical Application Circuit*.

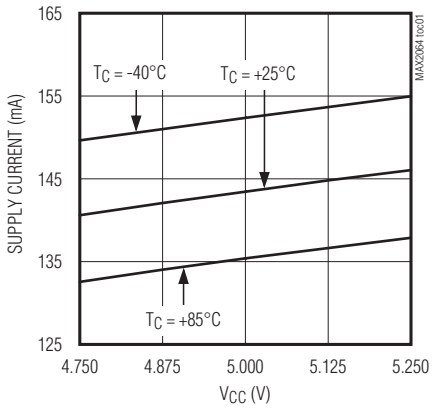
Note 7: It is advisable not to continuously operate the RF input 1 or RF input 2 above +15dBm.

50MHz至1000MHz、高线性度、串行/模拟控制VGA

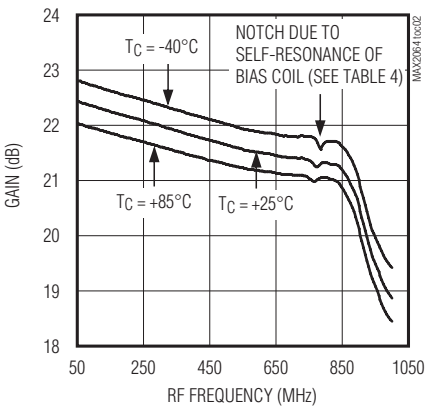
典型工作特性

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +5V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

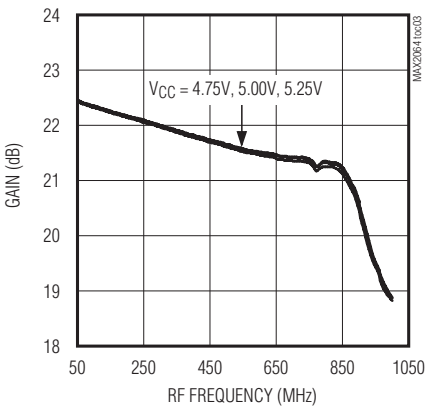
SUPPLY CURRENT vs. SUPPLY VOTAGE



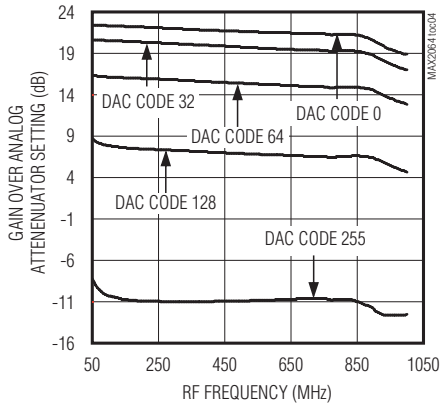
GAIN vs. RF FREQUENCY



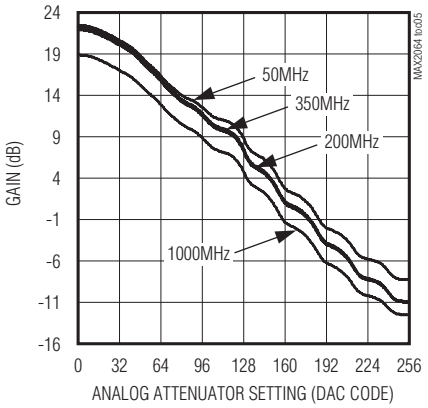
GAIN vs. RF FREQUENCY



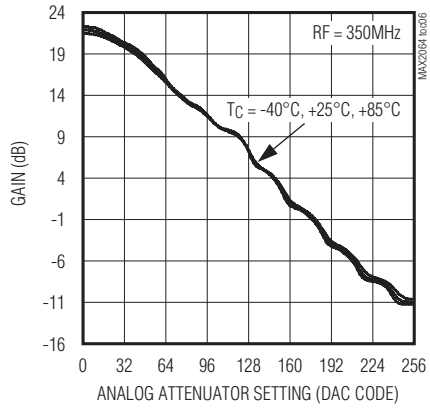
GAIN OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY



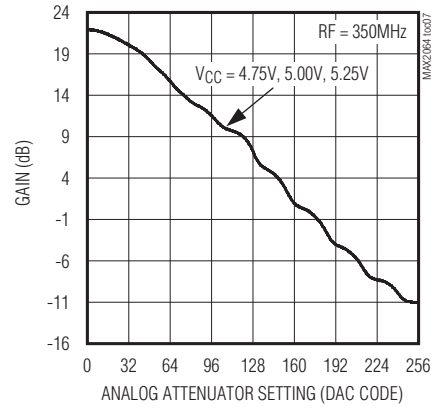
GAIN vs. ANALOG ATTENUATOR SETTING



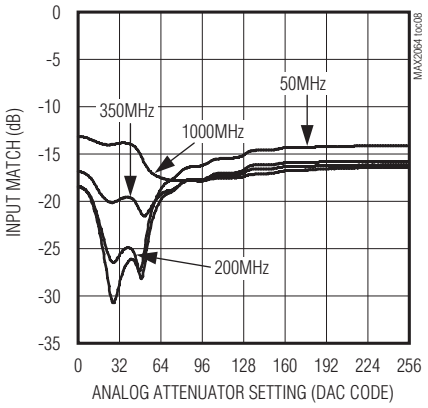
GAIN vs. ANALOG ATTENUATOR SETTING



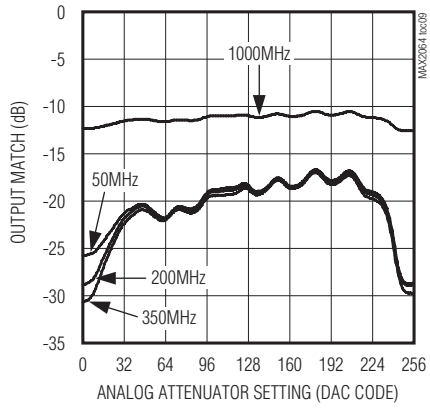
GAIN vs. ANALOG ATTENUATOR SETTING



INPUT MATCH vs. ANALOG ATTENUATOR SETTING



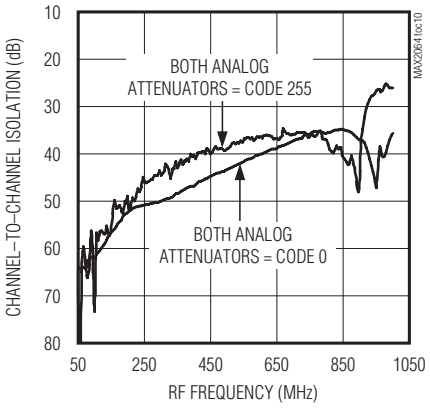
OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING



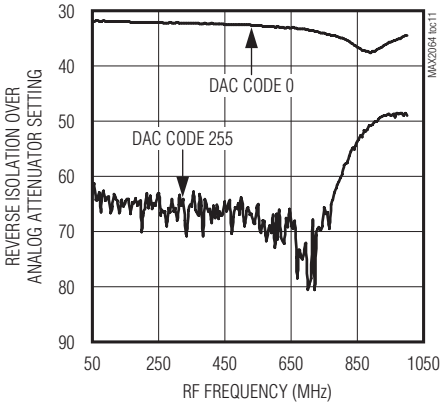
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +5V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

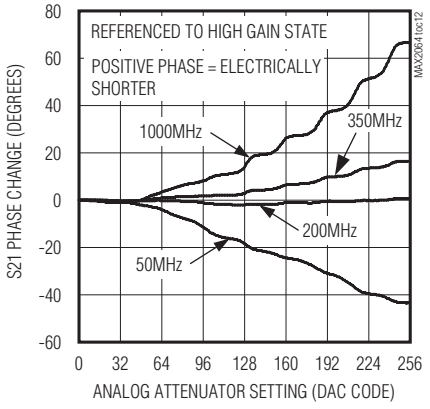
CHANNEL–TO–CHANNEL ISOLATION vs. RF FREQUENCY



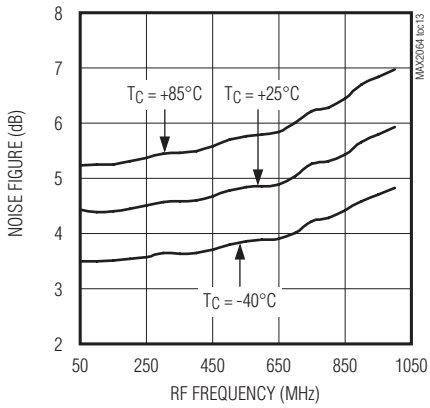
REVERSE ISOLATION OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY



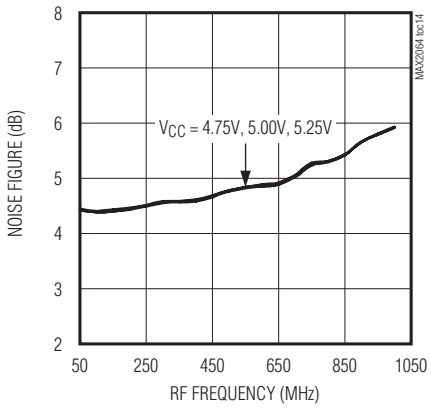
S21 PHASE CHANGE vs. ANALOG ATTENUATOR SETTING



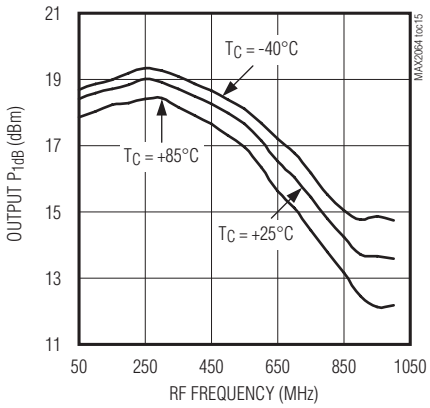
NOISE FIGURE vs. RF FREQUENCY



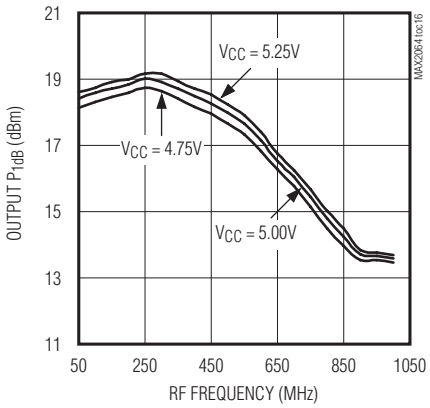
NOISE FIGURE vs. RF FREQUENCY



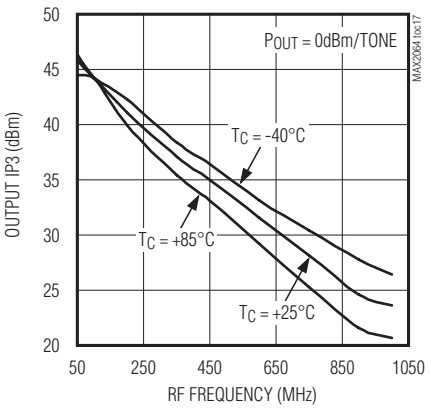
OUTPUT P_{1dB} vs. RF FREQUENCY



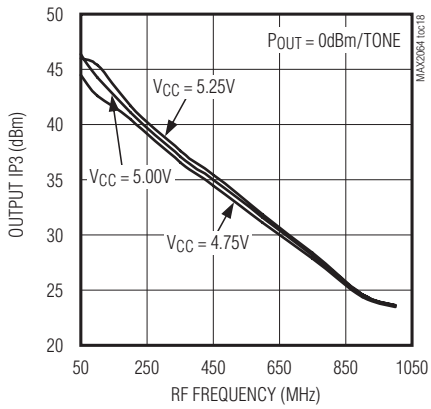
OUTPUT P_{1dB} vs. RF FREQUENCY



OUTPUT IP3 vs. RF FREQUENCY



OUTPUT IP3 vs. RF FREQUENCY

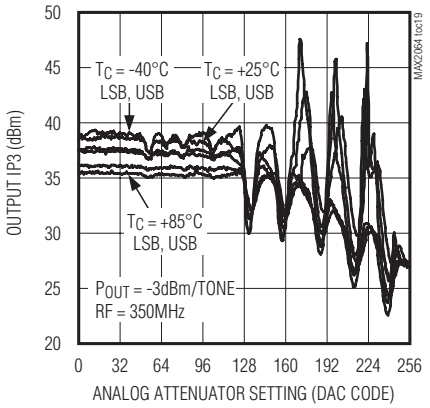


50MHz至1000MHz、高线性度、串行/模拟控制VGA

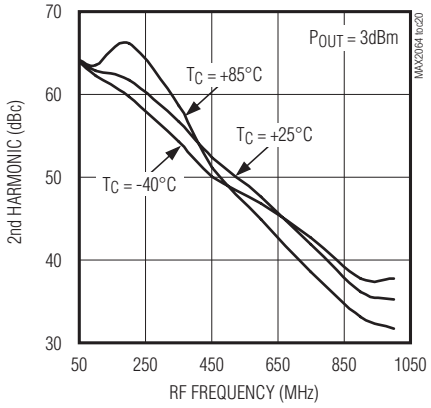
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +5V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

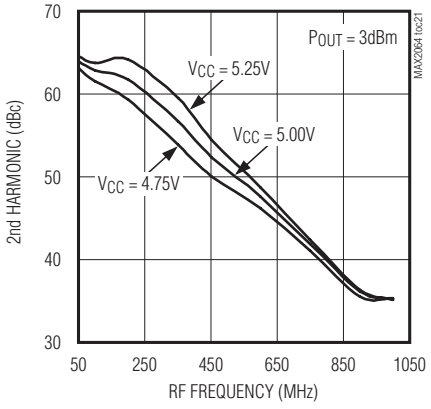
OUTPUT IP3 vs. ANALOG ATTENUATOR SETTING



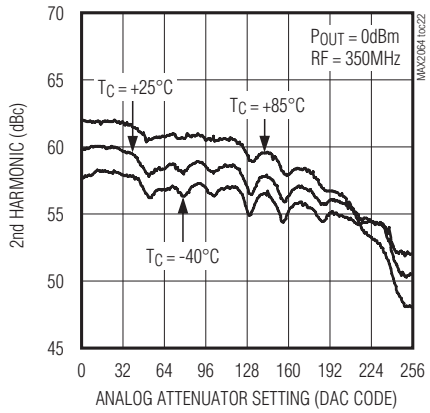
2nd HARMONIC vs. RF FREQUENCY



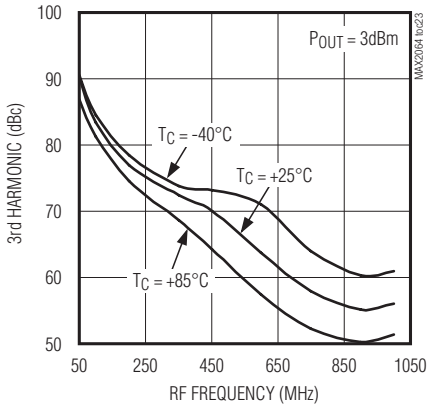
2nd HARMONIC vs. RF FREQUENCY



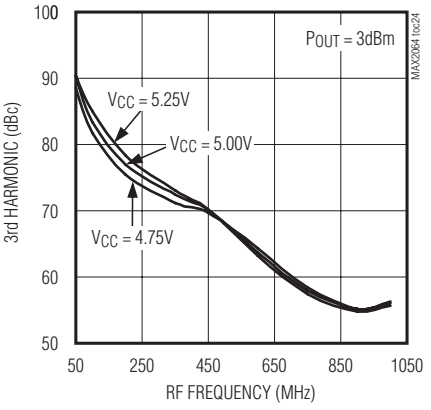
2nd HARMONIC vs. ANALOG ATTENUATOR SETTING



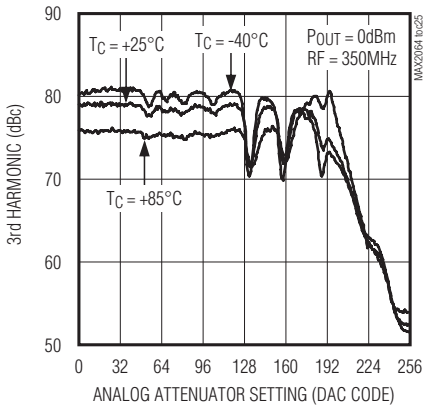
3rd HARMONIC vs. RF FREQUENCY



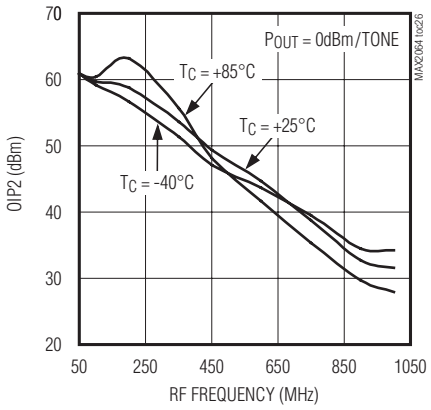
3rd HARMONIC vs. RF FREQUENCY



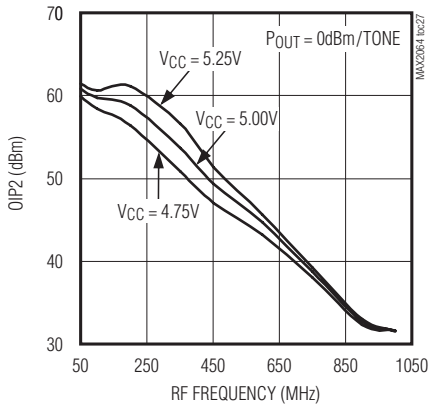
3rd HARMONIC vs. ANALOG ATTENUATOR SETTING



OIP2 vs. RF FREQUENCY



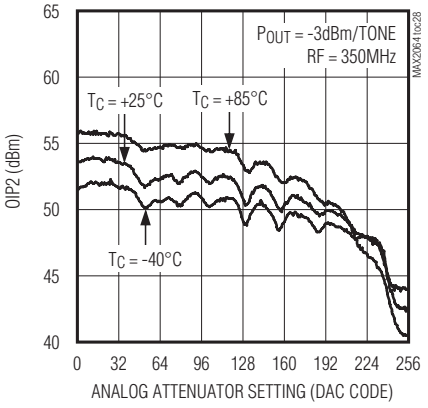
OIP2 vs. RF FREQUENCY



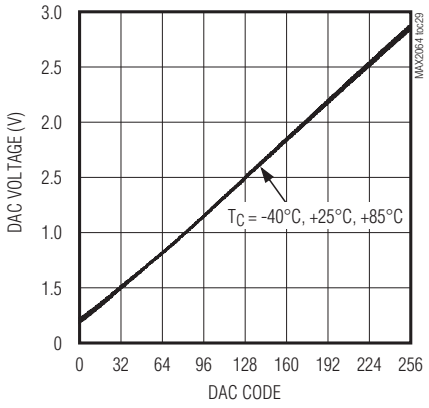
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = +5V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

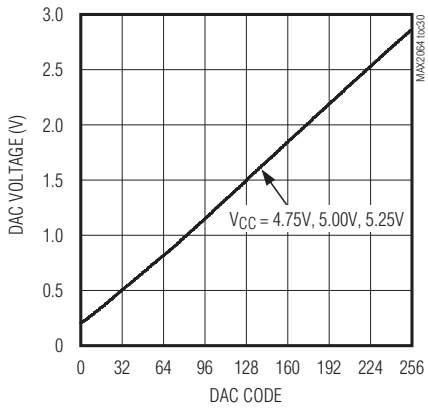
OIP2 vs. ANALOG ATTENUATOR SETTING



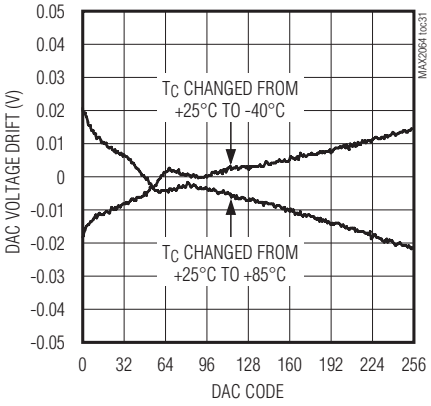
DAC VOLTAGE vs. DAC CODE



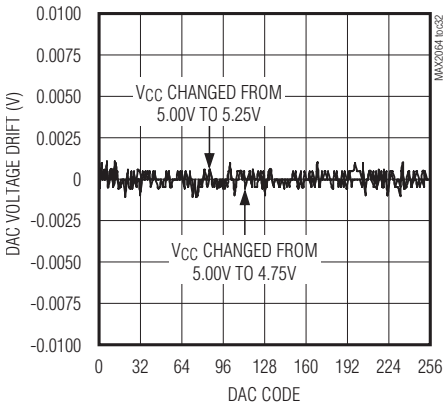
DAC VOLTAGE vs. DAC CODE



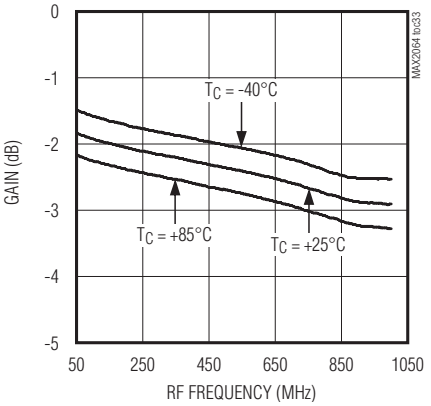
DAC VOLTAGE DRIFT vs. DAC CODE



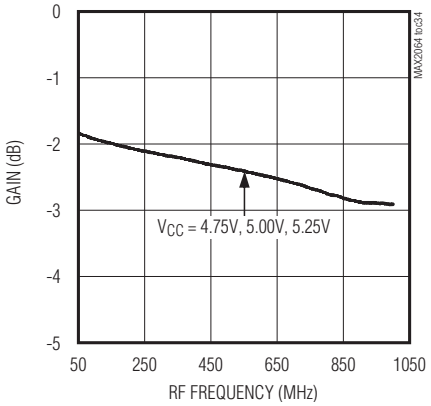
DAC VOLTAGE DRIFT vs. DAC CODE



GAIN vs. RF FREQUENCY (ANALOG ATTENUATOR ONLY)



GAIN vs. RF FREQUENCY (ANALOG ATTENUATOR ONLY)



50MHz至1000MHz、高线性度、串行/模拟控制VGA

典型工作特性(续)

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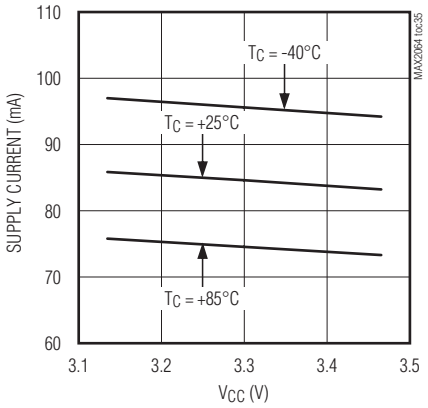
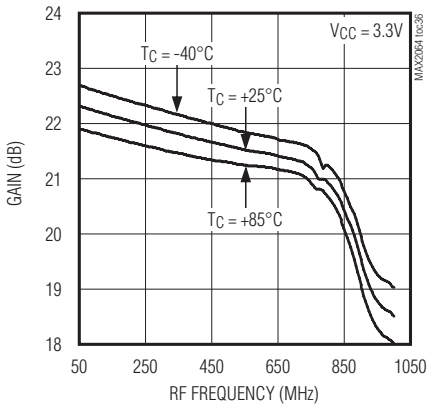
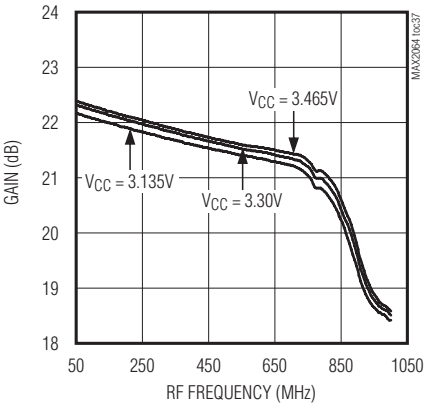
SUPPLY CURRENT vs. SUPPLY VOLTAGE



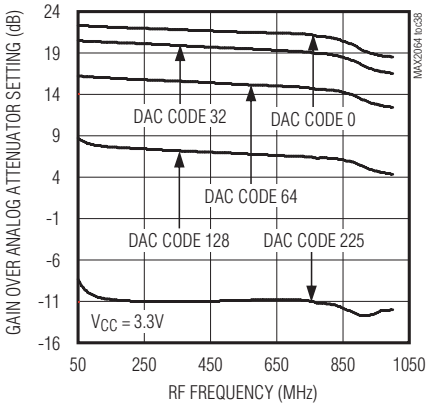
GAIN vs. RF FREQUENCY



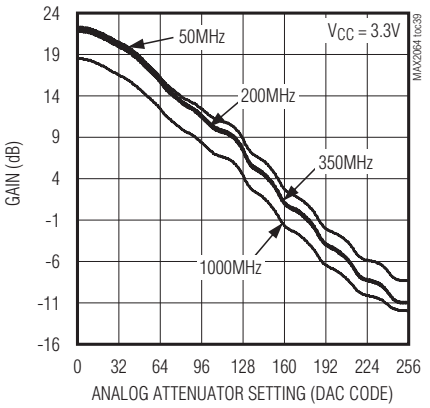
GAIN vs. RF FREQUENCY



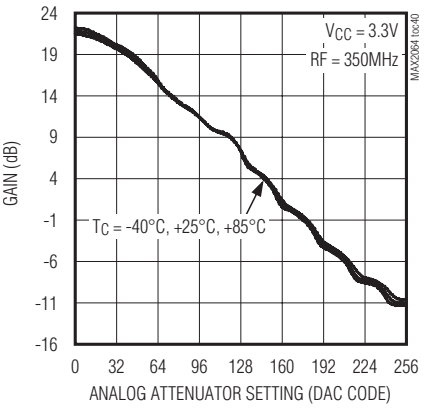
GAIN OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY



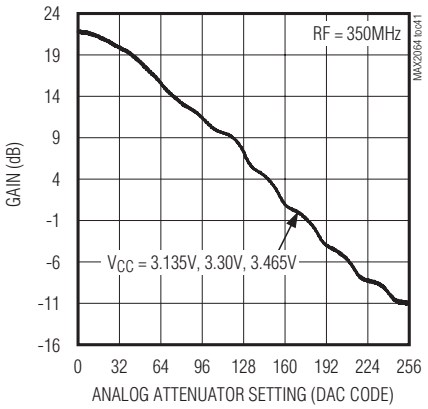
GAIN vs. ANALOG ATTENUATOR SETTING



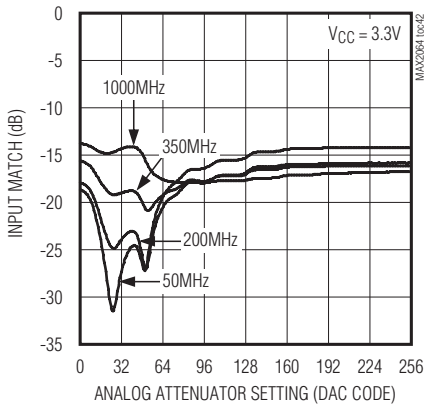
GAIN vs. ANALOG ATTENUATOR SETTING



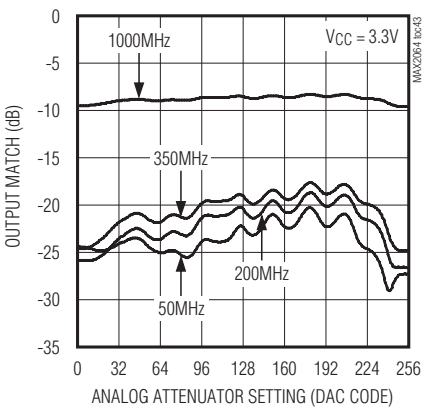
GAIN vs. ANALOG ATTENUATOR SETTING



INPUT MATCH vs. ANALOG ATTENUATOR SETTING



OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING



典型工作特性(续)

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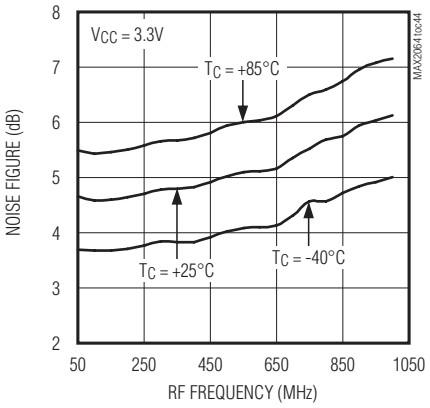
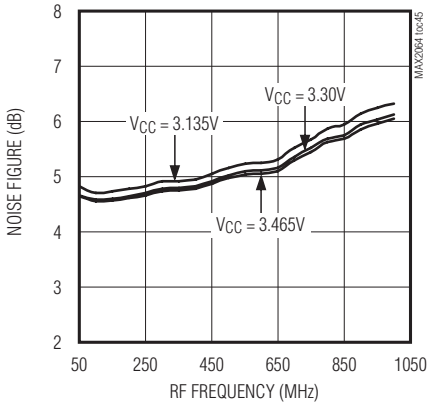
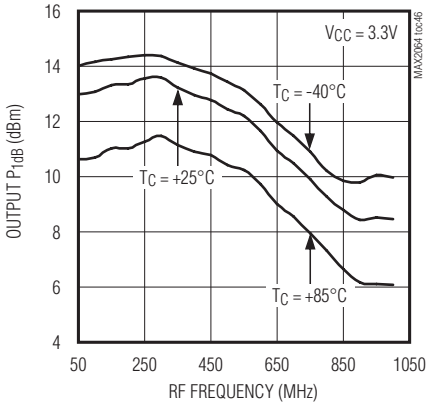
NOISE FIGURE vs. RF FREQUENCY



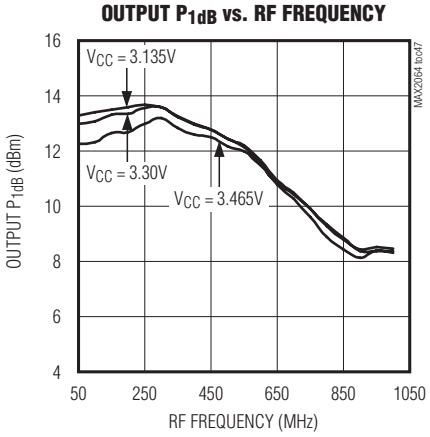
NOISE FIGURE vs. RF FREQUENCY



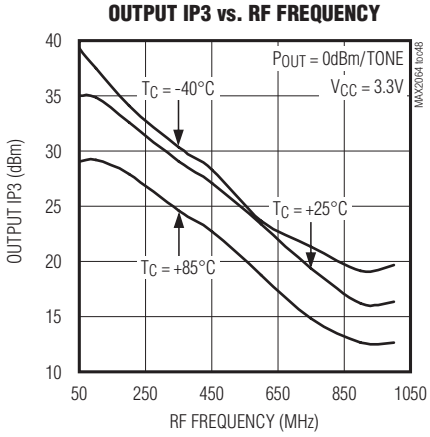
OUTPUT P_{1dB} vs. RF FREQUENCY



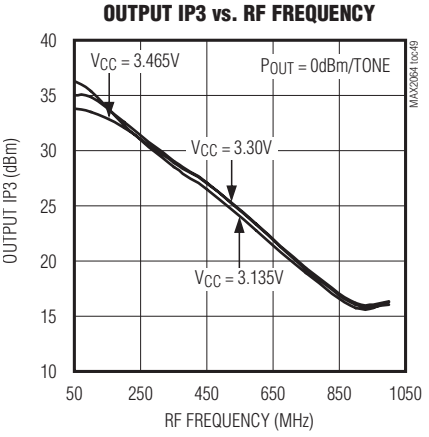
OUTPUT P_{1dB} vs. RF FREQUENCY



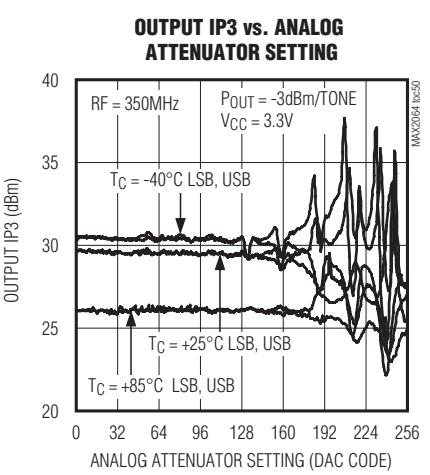
OUTPUT IP3 vs. RF FREQUENCY



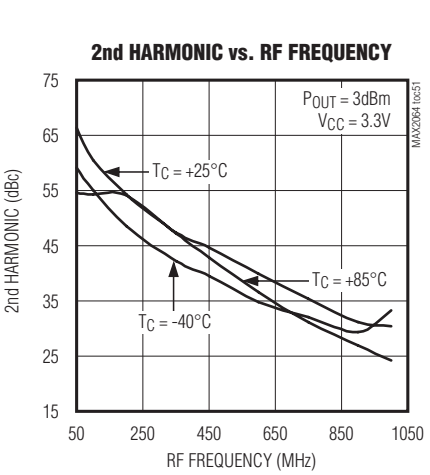
OUTPUT IP3 vs. RF FREQUENCY



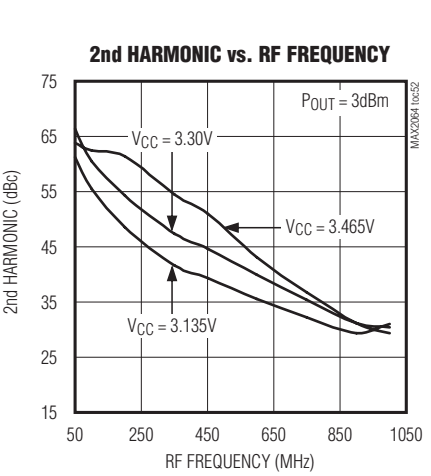
OUTPUT IP3 vs. ANALOG ATTENUATOR SETTING



2nd HARMONIC vs. RF FREQUENCY



2nd HARMONIC vs. RF FREQUENCY



50MHz至1000MHz、高线性度、串行/模拟控制VGA

典型工作特性(续)

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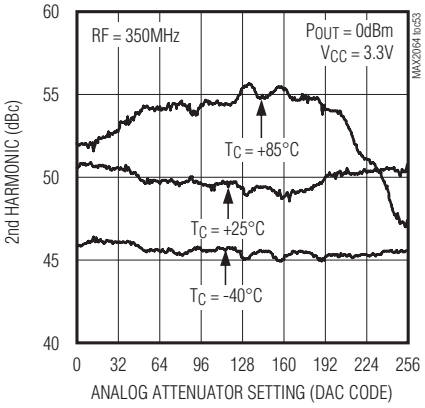
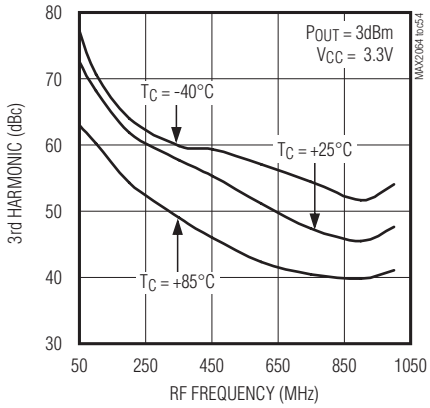
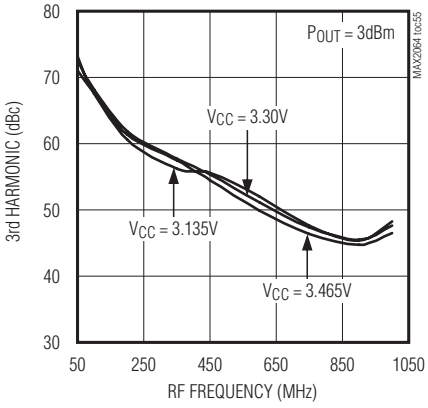
2nd HARMONIC vs. ANALOG ATTENUATOR SETTING



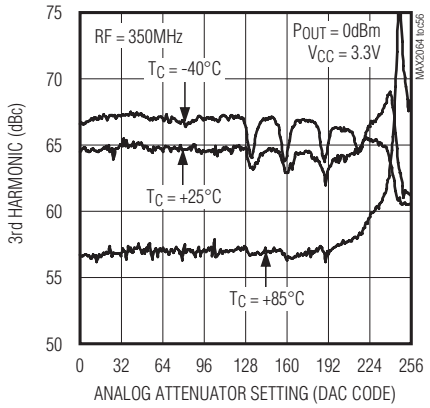
3rd HARMONIC vs. RF FREQUENCY



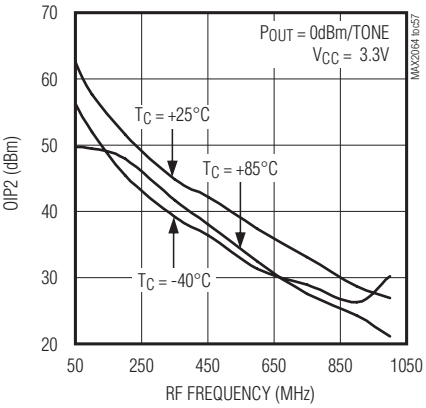
3rd HARMONIC vs. RF FREQUENCY



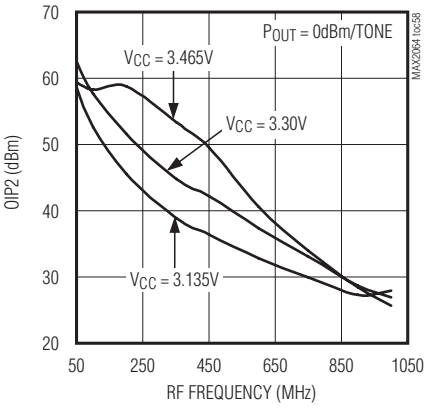
3rd HARMONIC vs. ANALOG ATTENUATOR SETTING



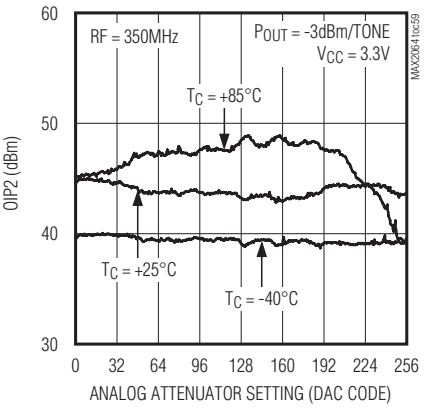
OIP2 vs. RF FREQUENCY



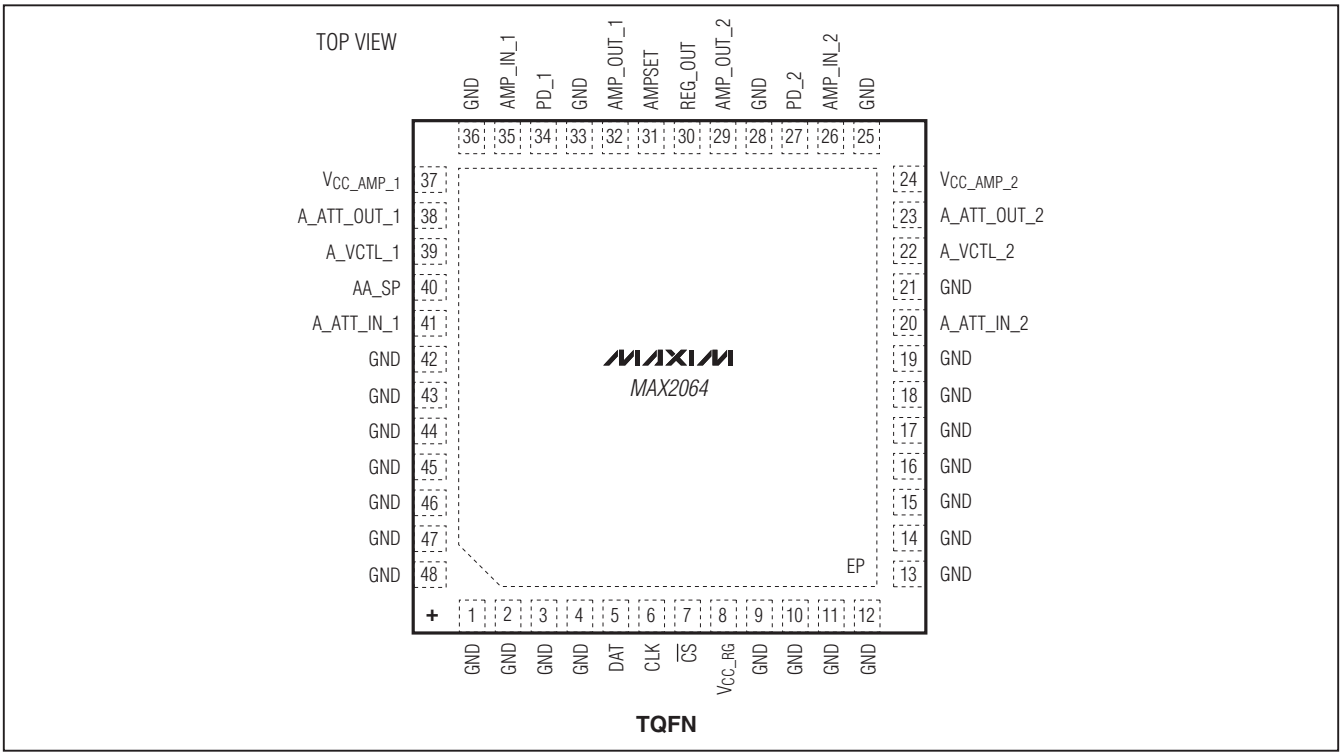
OIP2 vs. RF FREQUENCY



OIP2 vs. ANALOG ATTENUATOR SETTING



引脚配置



TQFN

引脚说明

引脚	名称	说明
1–4, 9–19, 21, 25, 28, 33, 36, 42–48	GND	地。
5	DAT	SPI数据输入。
6	CLK	SPI时钟输入。
7	$\overline{CS}$	SPI片选输入。
8	V_{CC_RG}	稳压电源输入，连接到3.3V或5V外部电源。V_{CC_RG}为驱动放大器以外的所有电路供电，利用10nF电容旁路该引脚，电容应靠近该引脚放置。
20	A_ATT_IN_2	模拟衰减器输入(50Ω)，通道2。需要连接一个1000pF隔直流电容。
22	A_VCTL_2	模拟衰减器电压控制输入，通道2。如果使用DAC 2 (AA_SP = 1)，则通过150pF电容旁路。
23	A_ATT_OUT_2	模拟衰减器输出(50Ω)，通道2。需要隔直流电容，通过1000pF电容连接到AMP_IN_2。
24	$V_{CC\_AMP\_2}$	驱动放大器电源输入，通道2。在尽可能靠近该引脚的位置安装10nF旁路电容。
26	AMP_IN_2	驱动放大器输入(50Ω)，通道2。需要连接隔直流电容，通过1000pF电容连接到A_ATT_OUT_2。
27	PD_2	关断控制，通道2，详细操作请参考表2。
29	AMP_OUT_2	放大器驱动输出(50Ω)，通道2。在AMP_OUT_2与$V_{CC_}$之间连接上拉电感。

50MHz至1000MHz、高线性度、串行/模拟控制VGA

引脚说明(续)

引脚	名称	说明
30	REG_OUT	稳压器输出，通过1µF电容旁路。
31	AMPSET	3.3V供电时，驱动放大器的偏置设置。V_{CC_AMP1}和V_{CC_AMP2}采用3.3V供电时，置为逻辑1；5V供电时，置为逻辑0。
32	AMP_OUT_1	放大器驱动输出(50Ω)，通道1。在AMP_OUT_1与$V_{CC_}$之间连接上拉电感。
34	PD_1	关断控制，通道1，详细操作请参考表2。
35	AMP_IN_1	驱动放大器输入(50Ω)，通道1。需要连接隔直流电容，通过1000pF电容连接到A_ATT_OUT_1。
37	$V_{CC\_AMP\_1}$	驱动放大器电源输入，通道1。在尽可能靠近该引脚的位置安装10nF旁路电容。
38	A_ATT_OUT_1	模拟衰减器输出(50Ω)，通道1。需要连接隔直流电容，通过1000pF电容连接到AMP_IN_1。
39	A_VCTL_1	模拟衰减器电压控制输入，通道1。如果使用片上DAC (AA_SP = 1)，则通过150pF电容旁路。
40	AA_SP	DAC使能/禁止逻辑输入，用于模拟衰减器。将AA_SP置为逻辑1，使能片上DAC电路和数字SPI控制；将AA_SP置为逻辑0，禁止片上DAC电路和数字SPI控制。当AA_SP = 0时，使用模拟控制信号(A_VCTL_1和A_VCTL_2)。
41	A_ATT_IN_1	模拟衰减器输入(50Ω)，通道1。需要隔直流电容，通过AMP_IN_1连接一个1000pF电容。
—	EP	裸焊盘，内部连接到GND。将其连接到大面积的PCB接地区域有利于改善RF性能，增强散热。

详细说明

MAX2064高线性度模拟VGA是一款通用的高性能放大器，针对50MHz至1000MHz频率范围、50Ω系统接口应用设计。

器件的每个通道集成了一个模拟衰减器，可提供33dB的增益控制，同时可优化放大器驱动设计来提供高增益、高IP3、低NF和低功耗指标。

每个模拟衰减器通过外部电压控制，或者通过由SPI兼容接口控制的8位DAC控制。有关衰减器编程的细节，请参考*应用信息*部分以及表3。

因为每个通道中两级放大电路的每一级都具有RF输入和RF输出，通过适当配置可以优化NF (第1级放大器)或OIP3 (最后一级放大器)。该器件还提供增益为24dB的放大器(放大器本身)，增益最大时NF为4.4dB (包括衰减器的插入损耗)，并提供+41dBm的高OIP3。这些特性使得器件能够为多通道接收器和发射器提供一个理想的VGA。

此外，器件工作在+5V单电源时，性能指标完全符合规格要求；如果系统允许降低性能，则可工作在+3.3V单电源增强低功耗模式。器件提供紧凑的48引脚、TQFN封装(7mm x 7mm)，带有裸焊盘。确保在T_C = -40°C至+85°C扩展级温度范围内满足电气特性要求。

模拟衰减器控制

器件集成了两级模拟衰减器，每级模拟衰减器具有33dB动态范围，利用外部电压或通过3线串行接口(SPI)控制片上8位DAC实现衰减器调节，请参考*应用信息*和表3所示衰减器设置，获得有关衰减器的详细信息。衰减器可用于静态和动态功率控制。

注意，当模拟衰减器受控于SPI总线控制的DAC时，DAC输出电压分别出现在A_VCTL_1和A_VCTL_2 (分别对应于引脚39和引脚22)。因此，SPI控制模式下，A_VCTL_1和A_VCTL_2引脚必须连接到另一端接地的电阻和电容，请参考*典型应用电路*。

表1. 控制逻辑

AA_SP	ANALOG ATTENUATOR	D/A CONVERTER
0	Controlled by external control voltage	Disabled
1	Controlled by on-chip DAC	Enabled (DAC output voltage shows on A_VCTL__ pins); DAC uses on-chip voltage reference

表2. 工作模式

RESULT	Vcc (V)	AMP_SET	PD_1	PD_2
All on	5	0	0	0
	3.3	1	0	0
AMP1 off AMP2 on	5	0	1	0
	3.3	1	1	0
AMP1 on AMP2 off	5	0	0	1
	3.3	1	0	1
All off	5	0	1	1
	3.3	1	1	1

驱动放大器

器件包括两个24dB固定增益的高性能驱动器。每个驱动放大器优化于50MHz至1000MHz频率范围的高线性度指标。

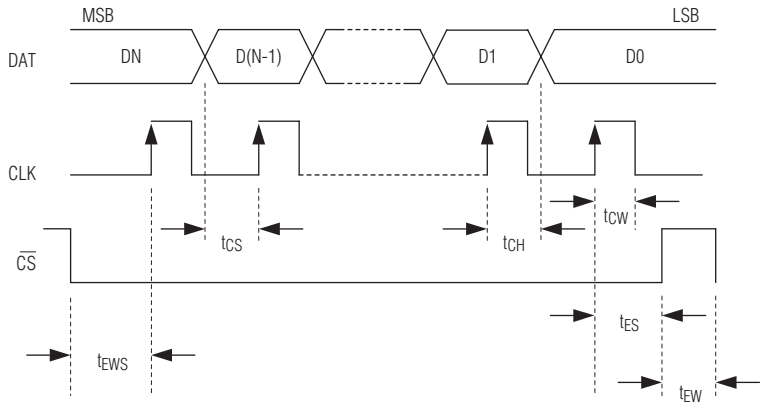
应用信息

工作模式

器件可以工作在+3.3V电源电压，但会降低线性指标。AMPSET引脚需要在不同模式下进行适当偏置，如表2所示。此外，还可以独立控制驱动放大器关断，节省直流电源的功耗，详细信息请参考表2所示偏置配置。

SPI接口和衰减器设置

该衰减器可采用5位字节通过SPI/MICROWIRE™兼容串行接口进行控制。移入56位数据，MSB在前，并通过$\overline{CS}$打包。前28位数据用于设置第一级衰减器，后续28位数据用于设置第二级衰减器。当$\overline{CS}$为低电平时，时钟有效，数据在时钟的上升沿移入。当$\overline{CS}$跳变到高电平时，数据被锁存，改变衰减器设置(图1)。表3给出了SPI数据格式的详细信息。



NOTES: DATA ENTERED ON CLOCK RISING EDGE.
ATTENUATOR REGISTER STATE CHANGE ON $\overline{CS}$ RISING EDGE.
N = NUMBER OF DATA BITS.
D0 IS AN ADDRESS BIT, D1/DN ARE DATA BITS (WHERE N ≤ 20).

图1. SPI时序图

MICROWIRE是National Semiconductor Corp.的商标。

表3. SPI数据格式

FUNCTION	BIT	DESCRIPTION
Reserved	D55 (MSB)	Bits D[55:36] are reserved. Set to logic 0.
	D54	
	D53	
	D52	
	D51	
	D50	
	D49	
	D48	
	D47	
	D46	
	D45	
	D44	
	D43	
	D42	
	D41	
	D40	
	D39	
	D38	
	D37	
	D36	
On-Chip DAC (Path 2)	D35	Bit 7 (MSB) of on-chip DAC used to program the Path 2 analog attenuator
	D34	Bit 6 of DAC
	D33	Bit 5 of DAC
	D32	Bit 4 of DAC
	D31	Bit 3 of DAC
	D30	Bit 2 of DAC
	D29	Bit 1 of DAC
	D28	Bit 0 (LSB) of DAC

表3. SPI数据格式(续)

FUNCTION	BIT	DESCRIPTION
Reserved	D27	Bits D[27:8] are reserved. Set to logic 0.
	D26	
	D25	
	D24	
	D23	
	D22	
	D21	
	D20	
	D19	
	D18	
	D17	
	D16	
	D15	
	D14	
	D13	
	D12	
	D11	
	D10	
	D9	
	D8	
On-Chip DAC (Path 1)	D7	Bit 7 (MSB) of on-chip DAC used to program the Path 1 analog attenuator
	D6	Bit 6 of DAC
	D5	Bit 5 of DAC
	D4	Bit 4 of DAC
	D3	Bit 3 of DAC
	D2	Bit 2 of DAC
	D1	Bit 1 of DAC
	D0 (LSB)	Bit 0 (LSB) of DAC

50MHz至1000MHz、高线性度、串行/模拟控制VGA

供电顺序

所采用的供电顺序为:

1) 电源上电

2) 施加控制信号

布局考虑

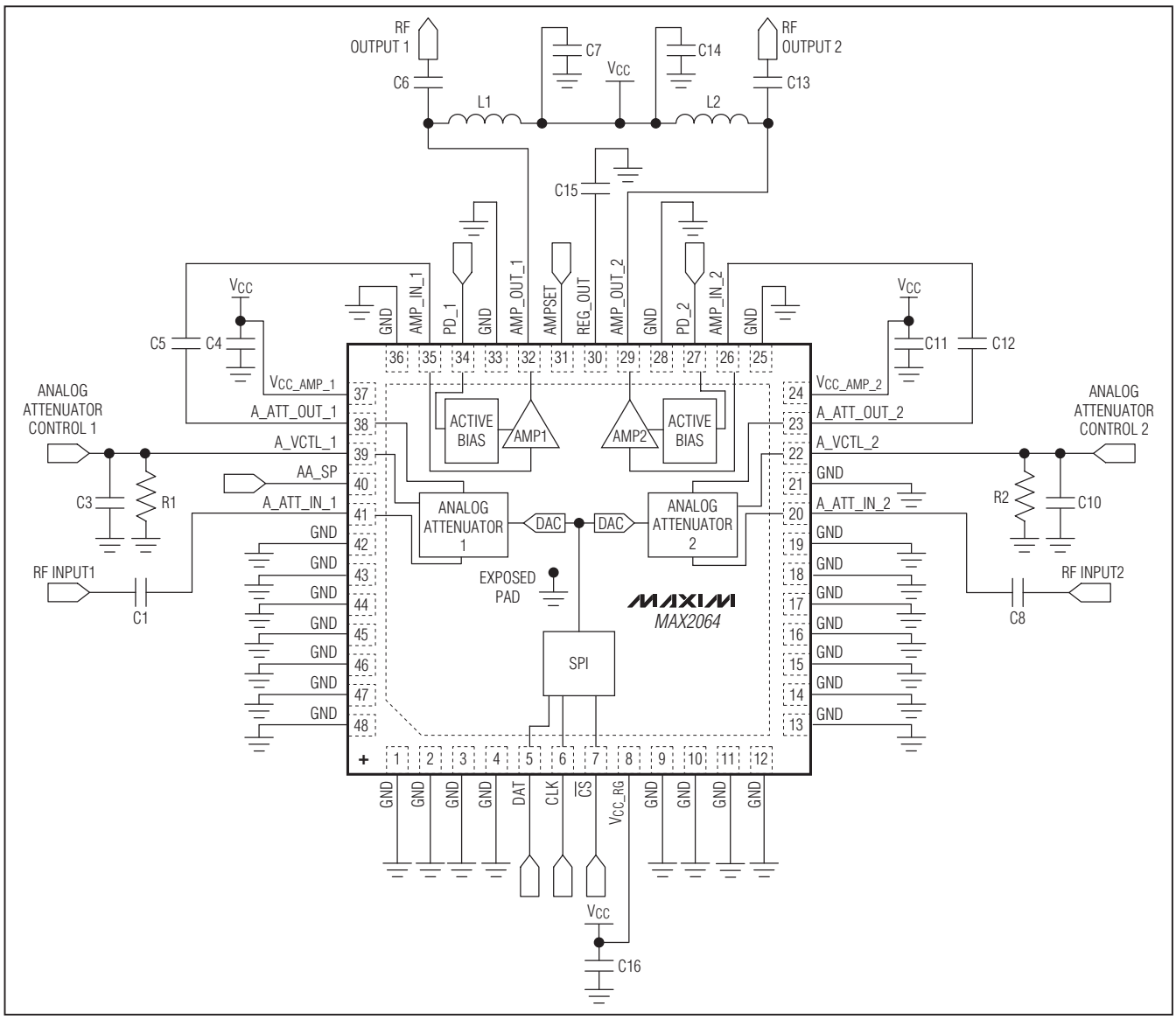
器件经过优化的引脚配置有助于实现紧凑的器件布局和相关分立元件的布局。器件采用48引脚TQFN-EP封装，其裸焊盘(EP)提供了一条到管芯的低热阻通道。安装器件的PCB设计需要利用EP散热，这一点非常关键。另外，EP与电气地的连接需要通过低电感路径。EP**必须**直接或通过一系列过孔焊接到PCB的地层。PCB布局应该在顶层提供适当的接地屏蔽，以隔离放大器的输入和输出。通道之间(输入和输出)的屏蔽对于通道间隔离非常重要。

表4. 典型应用电路的元件值

DESIGNATION	QTY	DESCRIPTION	COMPONENT SUPPLIER
C1, C5, C6, C8, C12, C13	6	1000pF ceramic capacitors (0402) GRM1555C1H102J	Murata Electronics North America, Inc.
C3, C10	2	150pF ceramic capacitors (0402) GRM1555C1H151J	Murata Electronics North America, Inc.
C4, C7, C11, C14, C16	5	10nF ceramic capacitors (0402) GRM155R71E103K	Murata Electronics North America, Inc.
C15	1	1µF ceramic capacitor (0603) GRM188R71C105K	Murata Electronics North America, Inc.
L1, L2*	2	820nH inductors (1008) Coilcraft 1008CS-821XJLC	Coilcraft, Inc.
R1, R2	2	47.5kΩ resistors (0402)	—
U1	1	48 TQFN-EP (7mm x 7mm) Maxim MAX2064ETM+	Maxim Integrated Products, Inc.

*选择电感，确保其谐振频率在工作频带以外。

典型应用电路



芯片信息

PROCESS: SiGe BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
48 TQFN-EP	T4877+7	**21-0144**	**90-0133**

50MHz至1000MHz、高线性度、串行/模拟控制VGA

修订历史

修订号	修订日期	说明	修改页
0	12/10	最初版本。	—

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