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备有评估板

MAX14808/MAX14809

八通道3级电平/四通道5级电平高压2A数字脉冲发生器，带T/R开关

概述

MAX14808/MAX14809八通道3级电平/四通道5级电平高压(HV)脉冲发生器，利用低压控制逻辑输入产生高频、高压双极性脉冲(高达±105V)，用于驱动超声系统的压电传感器。所有八个通道均具有嵌入式过压保护二极管和集成有源归零箝位电路。两款器件内置独立(浮地)电源(FPS)和电平转换器，用于实现信号转换，无需外部高压电容。MAX14808有八个集成的发送/接收(T/R)开关，MAX14809不带T/R开关。

器件具有两种工作模式：八通道三级电平脉冲发生器(集成有源归零箝位)或四通道五级电平脉冲发生器。作为八通道三级电平脉冲发生器时，每个通道由两路逻辑输入(DINN_/DINP_)控制，有源归零箝位的电流为脉冲发生器的电流的一半，1A (典型值)；作为四通道五级电平脉冲发生器时，每个通道由三路逻辑输入控制，有源归零的电流与脉冲发生器电流相同，2A (典型值)。

器件可工作在锁定或透明模式。锁定模式下，数据输入可与稳定的差分或单端时钟同步，以降低与FPGA输出信号相关的相位噪声，有助于多普勒分析；透明模式下，禁止同步功能，经过18ns延时后输出与输入对应的信号。两款器件均具有可调节最大电流(0.5A至2A)，不需要满幅电流时可降低功耗。

器件具有集成的高压毛刺箝位二极管(低寄生电容)，用于接收(Rx)和发送(Tx)隔离。两款器件均具有阻尼电路，可在突发发送结束后立即激活。阻尼电路的典型导通电阻为500Ω，对高压毛刺箝位二极管之前的脉冲发生器输出内部节点完全放电。

器件采用68引脚(10mm x 10mm) TQFN封装，带裸焊盘，工作在-40°C至+85°C扩展级温度范围。

优势和特性

- ♦ 节省空间(针对多通道系统/便携系统设计)
  - ✧ 高密度
    - • 八通道(三级电平模式)
    - • 四通道(五级电平模式)，单芯片封装
  - ✧ 集成低功耗T/R开关(MAX14808)
  - ✧ DirectDrive®架构，无需外部高压电容
  - ✧ 无需外部浮地电源(FPS)
- ♦ 高性能(增强图像质量)
  - ✧ 5MHz下提供优异的-43dBc (典型值)THD，二次谐波
  - ✧ 同步功能，不受FPGA抖动影响，提高多普勒性能
  - ✧ 18ns (典型值)传输延迟
  - ✧ 有源归零
- ♦ 节约功耗
  - ✧ 低静态功耗(5.7mW/通道，八通道模式)
  - ✧ 可编程电流功能
  - ✧ 关断模式和禁止发送模式

应用

超声医疗成像

工业探伤检测

压电驱动器

测试设备

定购信息和功能框图在数据资料的最后给出。

DirectDrive是Maxim Integrated.的注册商标。

相关型号以及配合该器件使用的推荐产品，请参见：china.maximintegrated.com/MAX14808.related。

本文是英文数据资料的译文，文中可能存在翻译上的不准确或错误。如需进一步确认，请在您的设计中参考英文资料。
有关价格、供货及订购信息，请联络Maxim亚洲销售中心：10800 852 1249 (北中国区)，10800 152 1249 (南中国区)，或访问Maxim的中文网站：china.maximintegrated.com。

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{DD} Logic Supply Voltage Range .....-0.3V to +5.6V
V_{CC} Positive Driver Supply Voltage Range .....-0.3V to +5.6V
V_{EE} Negative Driver Supply Voltage Range.....-5.6V to +0.3V
V_{NNA}, V_{NNB} High Negative
Supply Voltage Range.....-110V to +0.3V
V_{PPA}, V_{PPB} High Positive
Supply Voltage Range.....-0.3V to +110V
OUT_ Output Voltage Range .....$V_{NN\_}$ to $V_{PP\_}$
LVOUT_ Output Voltage Range
(100mA Maximum Current)..... .....-1.2V to +1.2V
DINN_, DINP_, CC_, SYNC, $\overline{LDO\_EN}$.....-0.3V to +5.6V
CLK, $\overline{CLK}$, MODE_ Voltage Range..... -0.3V to (V_{CC} + 0.3V)
THP Logic Output Voltage Range.....-0.3V to +5.6V
V_{GPA}, V_{GPB} Output Voltage
Range .....max[($V_{PP\_}$ - 5.6V), (V_{EE} + 0.6V)] to ($V_{PP\_}$ + 0.3V)
V_{GNA}, V_{GNB} Output Voltage
Range .....($V_{NN\_}$ - 0.3V) to min[(V_{CC} + 0.6V), ($V_{NN\_}$ + 5.6V)]
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 50mW/°C above +70°C) 4000mW
Operating Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Lead Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....20°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....0.5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maximintegrated.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES (V_{DD}, V_{CC}, V_{EE}, $V_{PP\_}$, $V_{NN\_}$)						
Logic Supply Voltage	V_{DD}		+1.7	+3	+5.25	V
Positive Drive Supply Voltage	V_{CC}		+4.9	+5	+5.1	V
Negative Drive Supply Voltage	V_{EE}		-5.1	-5	-4.9	V
High-Side Supply Voltage	$V_{PP\_}$		0		+105	V
Low-Side Supply Voltage	$V_{NN\_}$		-105		0	V
External Low-Side LDO Voltage	$V_{GN\_}$ - $V_{NN\_}$	$\overline{LDO\_EN}$ = high	5	5.3	5.5	V
External High-Side LDO Voltage	$V_{PP\_}$ - $V_{GP\_}$	$\overline{LDO\_EN}$ = high	5	5.3	5.5	V
External Floating Power-Supply Current from $V_{GN\_}$	$I_{VGN\_}$	$\overline{LDO\_EN}$ = high (Note 3)	50			mA
External Floating Power-Supply Current from $V_{GP\_}$	$I_{VGP\_}$	$\overline{LDO\_EN}$ = high (Note 3)	85			mA
LOGIC INPUTS/OUTPUTS (DINN_, DINP_, MODE_, SYNC, CC_, $\overline{LDO\_EN}$)						
Low-Level Input Threshold	V_{IL}				0.2 x V_{DD}	V
High-Level Input Threshold	V_{IH}		0.8 x V_{DD}			V
Logic Input Capacitance	C_{IN}			4		pF

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between VGNA and VNNA, 1µF bypass capacitor between VGNB and VNNB, 1µF bypass capacitor between VGPA and VPPA, 1µF bypass capacitor between VGPB and VPPB, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input Leakage (All Inputs Except $\overline{LDO\_EN}$)	I_{IN}	V_{IN} = 0V or V_{DD}		-1	0	+1	µA
$\overline{LDO\_EN}$ Pulldown Resistance	$R_{\overline{LDO\_EN}}$			7	10	14	kΩ
THP Low-Level Output Voltage	V_{OL}	Pullup resistor to V_{DD} (R_{PULLUP} = 1kΩ)				0.1 x V_{DD}	V
CLOCK INPUTS (CLK, $\overline{CLK}$)—DIFFERENTIAL MODE							
Differential Clock Input Voltage Range	V_{CLKD}			0.2		2	V_{P-P}
Common-Mode Voltage	V_{CLKCM}				V_{CC}/2		V
Common-Mode Voltage Range	V_{CL}			V_{CC}/2 - 0.45		V_{CC}/2 + 0.45	V
Input Resistance	R_{CLK}, $R_{\overline{CLK}}$	Differential			7		kΩ
		Common mode			23		kΩ
Input Capacitance	C_{CLK}, $C_{\overline{CLK}}$	Capacitance to GND (each input)			4		pF
CLOCK INPUTS (CLK, $\overline{CLK}$)—SINGLE-ENDED MODE ($V_{\overline{CLK}}$ < 0.1V)							
Low-Level Input	V_{IL}	CLK				0.2 x V_{DD}	V
High-Level Input	V_{IH}	CLK		0.8 x V_{DD}			V
Single-Ended Mode Selection Threshold Low	V_{IL}	$\overline{CLK}$				0.1	V
Single-Ended Mode Selection Threshold High	V_{IH}	$\overline{CLK}$		1			V
Input Capacitance (CLK)	C_{CLK}				4		pF
Logic Input Leakage (CLK)	I_{CLK}	V_{CLK} = 0V or V_{DD}		-1	0	+1	µA
Pullup Current ($\overline{CLK}$)	$I_{\overline{CLK}}$	$V_{\overline{CLK}}$ = 0V			120	180	µA
SUPPLY CURRENT—SHUTDOWN MODE (MODE0 = Low, MODE1 = Low)							
V_{DD} Supply Current	I_{DD}	All inputs connected to GND or V_{DD}				3	µA
V_{CC} Supply Current	I_{CC}	All inputs connected to GND or V_{DD}				22	µA
V_{EE} Supply Current	I_{EE}	All inputs connected to GND or V_{DD}				13	µA
$V_{PP\_}$ Supply Current	$I_{PP\_}$	All inputs connected to GND or V_{DD}				10	µA
$V_{NN\_}$ Supply Current	$I_{NN\_}$	All inputs connected to GND or V_{DD}				10	µA
SUPPLY CURRENT—DISABLE MODE (MODE0 = High, MODE1 = High)							
V_{DD} Supply Current	I_{DDQ}	All inputs connected to GND or V_{DD}	Transparent or single-ended clock mode		1.7	3	µA
			Differential clock mode, V_{CLKD} = 0.2V		110	190	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between VGNA and VNNA, 1µF bypass capacitor between VGNB and VNNB, 1µF bypass capacitor between VGPA and VPPA, 1µF bypass capacitor between VGPB and VPPB, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{EE} Supply Current	I_{EEQ}	DINN_ = DINP_ = GND			0.26	0.4	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		9.4	13	
			MAX14809		1.37	2	
V_{CC} Supply Current	I_{CCQ}	DINN_ = DINP_ = GND			0.49	0.75	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		9.6	13.2	
			MAX14809		1.6	2.3	
V_{CC} Supply Current Increase in Clocked Mode	ΔI_{CC}	Differential clock mode			3.5	5	mA
$V_{NN\_}$ Total Supply Current (Quiescent Mode)	$I_{NNQ\_}$	All inputs connected to GND or V_{DD}			195	305	µA
$V_{PP\_}$ Total Supply Current (Quiescent Mode)	$I_{PPQ\_}$	All inputs connected to GND or V_{DD}			220	340	µA
Total Power Dissipation per Channel (Disable Mode)	P_{PDIS1}	T/R switch off, damp off (transparent mode)			5.7		mW
	P_{PDIS2}	DINN_ = DINP_ = V_{DD}	MAX14808		17		
			MAX14809		7		
SUPPLY CURRENT—OCTAL THREE-LEVEL MODE, NO LOAD (MODE0 = High, MODE1 = Low)							
V_{DD} Supply Current (Quiescent Mode)	I_{DD}	All inputs connected to GND or V_{DD}	Transparent or single-ended clock mode		1.7	3	µA
			Differential clock mode, V_{CLKD} = 0.2V		110	190	
V_{EE} Supply Current (Quiescent Mode)	I_{EEQ}	DINN_ = DINP_ = GND			0.26	0.4	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		9.4	13	
			MAX14809		1.37	2	
V_{CC} Supply Current (Quiescent Mode)	I_{CCQ}	DINN_ = DINP_ = GND			0.49	0.75	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		9.6	13.2	
			MAX14809		1.6	2.3	
V_{CC} Supply Current Increase in Clocked Mode	ΔI_{CC}	Differential clock mode			3.5	5	mA
$V_{NN\_}$ Total Supply Current (Quiescent Mode)	$I_{NNQ\_}$	All inputs connected to GND or V_{DD}			195	305	µA
$V_{PP\_}$ Total Supply Current (Quiescent Mode)	$I_{PPQ\_}$	All inputs connected to GND or V_{DD}			220	340	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Power Dissipation per Channel (Quiescent Mode)	P_{PDIS1}	T/R switch off, damp off (transparent mode)			5.7		mW
	P_{PDIS2}	DINN_ = DINP_ = V_{DD} (transparent mode)	MAX14808		17		
			MAX14809		7		
V_{DD} Supply Current	I_{DD1}	CW Doppler (Note 4), transparent or single-ended clock mode			2.2	3.2	mA
	I_{DD2}	B mode (Note 5), transparent or single-ended clock mode (Figure 1a) (MAX14808)			3.3	6	µA
		B mode (Note 5), transparent or single-ended clock mode (Figure 1a) (MAX14809)			10	20	
V_{EE} Supply Current	I_{EE1}	8 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high		67	92	mA
	I_{EE2}	8 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low	MAX14808		9.7	14.8	
			MAX14809		2	3	
V_{CC} Supply Current	I_{CC1}	8 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high		45	60	mA
	I_{CC2}	8 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low	MAX14808		10	15	
			MAX14809		2.1	3.2	
V_{DD} Supply Current Increase in Clocked Mode	ΔI_{DD}	Differential clock mode			1.8		mA
V_{CC} Supply Current Increase in Clocked Mode	ΔI_{CC}	Differential clock mode			3.8		mA
$V_{NN\_}$ Supply Current	I_{NN1}	8 channels switching, CW Doppler, CC0 = high, CC1 = high, R_L = 1kΩ, C_L = 240pF (Note 4)			157	200	mA
	I_{NN2}	8 channels switching, B mode (Figure 1a), CC0 = low, CC1 = low, R_L = 1kΩ, C_L = 240pF (Note 5)			2	2.8	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between VGNA and VNNA, 1µF bypass capacitor between VGNB and VNNB, 1µF bypass capacitor between VGPA and VPPA, 1µF bypass capacitor between VGPB and VPPB, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{PP\_}$ Supply Current	I_{PP1}	8 channels switching, CW Doppler, CC0 = high, CC1 = high, R_L = 1kΩ, C_L = 240pF (Note 4)			186	230	mA
	I_{PP2}	8 channels switching, B mode (Figure 1a), CC0 = low, CC1 = low, R_L = 1kΩ, C_L = 240pF (Note 5)			3.1	4.5	
Power Dissipation per Channel (Octal Three-Level Mode)	PD_{CW}	1 channel switching, CW Doppler (Note 4)			286		mW
	PD_{PW}	1 channel switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low, R_L = 1kΩ, C_L = 240pF	MAX14808		73		
			MAX14809		66		
SUPPLY CURRENT—QUAD FIVE-LEVEL DUAL MODE, NO LOAD (MODE0 = Low, MODE1 = High)							
V_{DD} Supply Current (Quiescent Mode)	I_{DDQ}	All inputs connected to GND or V_{DD}	Transparent or single-ended clock mode		1.7	3	µA
			Differential clock mode, V_{CLKD} = 0.2V		110	190	
V_{EE} Supply Current (Quiescent Mode)	I_{EEQ}	DINN_ = DINP_ = GND			0.26	0.4	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		5.4	7.7	
			MAX14809		1.35	2	
V_{CC} Supply Current (Quiescent Mode)	I_{CCQ}	DINN_ = DINP_ = GND			0.49	0.75	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		5.6	7.8	
			MAX14809		1.6	2.3	
V_{CC} Supply Current Increase	ΔI_{CC}	Differential clock mode			3.5	5	mA
$V_{NN\_}$ Supply Current (Quiescent Mode)	$I_{NNQ\_}$	All inputs connected to GND or V_{DD}			195	305	µA
$V_{PP\_}$ Supply Current (Quiescent Mode)	$I_{PPQ\_}$	All inputs connected to GND or V_{DD}			220	340	µA
Power Dissipation per Channel (Quiescent Mode)	P_{PDIS1}	T/R switch off, DAMP off (transparent mode)			11.3		mW
	P_{PDIS2}	DINN_ = DINP_ = V_{DD} (transparent mode)	MAX14808		24.1		
			MAX14809		14.1		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between VGNA and VNNA, 1µF bypass capacitor between VGNB and VNNB, 1µF bypass capacitor between VGPA and VPPA, 1µF bypass capacitor between VGPB and VPPB, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Supply Current	I_{DD1}	4 channels switching, CW Doppler (Note 4)			1.4		mA
	I_{DD2}	4 channels switching, B mode (Note 5) (Figure 1a)			4.3		µA
V_{EE} Supply Current	I_{EE1}	4 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high		33		mA
	I_{EE2}	4 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low	MAX14808		5.9		
			MAX14809		1.6		
V_{CC} Supply Current	I_{CC1}	4 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high		22		mA
	I_{CC2}	4 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low	MAX14808		6		
			MAX14809		1.8		
V_{DD} Supply Current Increase	ΔI_{DD}	Differential clock mode			1.8		mA
V_{CC} Supply Current Increase	ΔI_{CC}	Differential clock mode			3.8		mA
$V_{NN\_}$ Supply Current	I_{NN1}	4 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high, R_L = 1kΩ, C_L = 240pF		90		mA
	I_{NN2}	4 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low			1.3		
$V_{PP\_}$ Supply Current	I_{PP1}	4 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high, R_L = 1kΩ, C_L = 240pF		103		mA
	I_{PP2}	4 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low			2.2		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between VGNA and VNNA, 1µF bypass capacitor between VGNB and VNNB, 1µF bypass capacitor between VGPA and VPPA, 1µF bypass capacitor between VGPB and VPPB, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Power Dissipation per Channel (Quad Five-Level Dual Mode)	PD_{CW}	1 channel switching, CW Doppler (Note 4), R_L = 1kΩ, C_L = 240pF			311		mW
	PD_{PW}	1 channel switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low, R_L = 1kΩ, C_L = 240pF	MAX14808		102		
			MAX14809		92		
SUPPLY CURRENT—OCTAL THREE-LEVEL, NO LOAD (MODE0 = High, MODE1 = Low, $\overline{LDO\_EN}$ = High, $V_{PP\_}$ - $V_{GP\_}$ = +5V, $V_{GN\_}$ - $V_{NN\_}$ = +5V)							
V_{EE} Supply Current (Quiescent Mode)	$I_{EEQ\_}$	All inputs connected to GND			25	46	µA
V_{CC} Supply Current (Quiescent Mode)	$I_{CCQ\_}$	All inputs connected to GND			280	420	µA
$V_{NN\_}$ Supply Current (Quiescent Mode)	$I_{NNQ\_}$	All inputs connected to GND			40	62	µA
$V_{PP\_}$ Supply Current (Quiescent Mode)	$I_{PPQ\_}$	All inputs connected to GND			40	62	µA
OUTPUT STAGE							
V_{NNA}, V_{NNB} Connected Low-Side Output Impedance	R_{OLS}	$I_{OUT\_}$ = -50mA	CC0 = low, CC1 = low		8.5		Ω
			CC0 = low, CC1 = high		10		
			CC0 = high, CC1 = low		13.5		
			CC0 = high, CC1 = high		26	48	
V_{PPA}, V_{PPB} Connected High-Side Output Impedance	R_{OHS}	$I_{OUT\_}$ = +50mA	CC0 = low, CC1 = low		9		Ω
			CC0 = low, CC1 = high		10.5		
			CC0 = high, CC1 = low		14.5		
			CC0 = high, CC1 = high		27	53	
Clamp nFET Output Impedance	R_{ONG}	$I_{OUT\_}$ = -50mA,			13.5		Ω
Clamp pFET Output Impedance	R_{OPG}	$I_{OUT\_}$ = +50mA			13.5		Ω
Active Damp Output Impedance	R_{DAMP}	Before grass-clipping diode			500		Ω

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{NNA}, V_{NNB} Connected Low-Side Output Current	I_{OLS}	V_{DS} = +100V	CC0 = low, CC1 = low		2.0		A
			CC0 = low, CC1 = high		1.5		
			CC0 = high, CC1 = low		1.0		
			CC0 = high, CC1 = high		0.5		
V_{PPA}, V_{PPB} Connected High-Side Output Current	I_{OHS}	V_{DS} = +100V	CC0 = low, CC1 = low		2.0		A
			CC0 = low, CC1 = high		1.5		
			CC0 = high, CC1 = low		1.0		
			CC0 = high, CC1 = high		0.5		
GND-Connected nFET Output Current	I_{ONG}	V_{DS} = +100V			1		A
GND-Connected pFET Output Current	I_{OPG}	V_{DS} = +100V			1		A
Diode Voltage Drop (Blocking Diode and Grass-Clipping Diode)	V_{DROP}	$I_{OUT\_}$ = ±50mA			1.7		V
LVOUT_Diode Clamping Voltage	LV_{CLAMP}	I_{LOAD} = 1mA (MAX14808 only)		-0.9		+1	V
Grass-Clipping Diode Reverse Capacitance	C_{REV}				2.5		pF
OUT_ Equivalent Large-Signal Shunt Capacitance	C_{HS}	$200V_{P-P}$ signal			80		pF
T/R Switch On Impedance	R_{ON}	MAX14808 only			11.5		Ω
T/R Switch Off Impedance	R_{OFF}	MAX14808 only		1			MΩ
LVOUT_ Output Offset	LV_{OFF}	LVOUT_, OUT_ unconnected, V_{CC} = +5V, V_{EE} = -5V		-40	0	+40	mV
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold	t_{SDN}	Temperature rising			+145		°C
Thermal-Shutdown Hysteresis	t_{HYS}				20		°C

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, V_{GNA} connected to V_{NNA} with 1µF capacitor, V_{GNB} connected to V_{NNB} with 1µF capacitor, V_{GPA} connected to V_{PPA} with 1µF capacitor, V_{GPB} connected to V_{PPB} with 1µF capacitor, $V_{\overline{LDO\_EN}}$ = 0V, V_{CC0} = 0V, V_{CC1} = 0V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input to Output Rise Propagation Delay	t_{PLH}	From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a)			18		ns
Logic Input to Output Fall Propagation Delay	t_{PHL}	From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a)			18		ns
Logic Input to Output Rise to GND Propagation Delay	t_{PL0}	From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a)			18		ns
Logic Input to Output Fall to GND Propagation Delay	t_{PH0}	From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a)			18		ns
OUT_ Fall Time (V_{PPA} to V_{NNA}, V_{PPB} to V_{NNB})	t_{FPN}	Figure 2b			30	48	ns
OUT_ Rise Time (V_{NNA} to V_{PPA}, V_{NNB} to V_{PPB})	t_{RNP}	Figure 2b			30	48	ns
OUT_ Rise Time (GND to V_{PPA}, GND to V_{PPB})	t_{R0P}	Figure 2b			15	22.5	ns
OUT_ Fall Time (GND to V_{NNA}, GND to V_{NNB})	t_{F0N}	Figure 2b			15	22.5	ns
OUT_ Rise Time (V_{NNA} to GND, V_{NNB} to GND)	t_{RN0}	20% to 80% transition (Figure 2b)	Three-level mode		21		ns
			Five-level dual mode		13		
OUT_ Fall Time (V_{PPA} to GND, V_{PPB} to GND)	t_{FP0}	20% to 80% transition (Figure 2b)	Three-level mode		21		ns
			Five-level dual mode		13		
T/R Switch Turn-On Time	t_{ONTRSW}	(MAX14808 only) Figure 3			0.65	1.2	µs
T/R Switch Turn-Off Time	$t_{OFFTRSW}$	(MAX14808 only) Figure 3 (Note 6)			0.02	0.1	µs
Output Enable Time (Shutdown Mode to Normal Operation)	t_{EN1}					100	µs
Output Disable Time (Normal Operation to Shutdown Mode)	t_{DIS1}					10	µs

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, V_{GNA} connected to V_{NNA} with 1µF capacitor, V_{GNB} connected to V_{NNB} with 1µF capacitor, V_{GPA} connected to V_{PPA} with 1µF capacitor, V_{GPB} connected to V_{PPB} with 1µF capacitor, $V_{\overline{LDO\_EN}}$ = 0V, V_{CC0} = 0V, V_{CC1} = 0V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Enable Time (Transmit Disable Mode to Normal Operation)	t_{EN2}					50	ns
Output Disable Time (Normal Operation to Transmit Disable Mode)	t_{DIS2}					65	ns
Output Enable Time (Normal Operation to Sync Mode)	t_{EN3}					4	µs
Output Disable Time (Sync Mode to Normal Operation)	t_{DIS3}					500	ns
CLK Frequency	f_{CLK}	V_{DD} = 2.5V	MAX14808			160	MHz
			MAX14809			200	
Input Setup Time (DINN_, DINP_)	t_{SETUP}	V_{DD} = 2.5V	MAX14808			3	ns
			MAX14809			2	
Input Hold Time (DINN_, DINP_)	t_{HOLD}	V_{DD} = 2.5V	MAX14808			3	ns
			MAX14809			1.5	
Second-Harmonic Distortion (Low Voltage)	THD2LV	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +5V, V_{PPB} = -V_{NNB} = +5V, square wave (all modes)			-40		dBc
Second-Harmonic Distortion (High Voltage)	THD2HV	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +100V, V_{PPB} = -V_{NNB} = +100V, square wave (all modes)			-43		dBc
Pulse Cancellation	PC1	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +100V, V_{PPB} = -V_{NNB} = +100V, 2 periods, all harmonics of the summed signed with respect to the carrier			-40		dBc
	PC2	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +100V, V_{PPB} = -V_{NNB} = +100V, 2 periods, $[(V_0 + V_{180})_{RMS}/(2 \times V_{0RMS})]_{dB}$			-40		
Pulser Bandwidth	BW	V_{PP} = +60V, V_{NNA} = -60V (Figure 4)			20		MHz
RMS Output Jitter	t_J	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +5V, V_{PPB} = -V_{NNB} = +5V, both in clocked mode or transparent mode (Figure 5)			6.25		ps

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, V_{GNA} connected to V_{NNA} with 1µF capacitor, V_{GNB} connected to V_{NNB} with 1µF capacitor, V_{GPA} connected to V_{PPA} with 1µF capacitor, V_{GPB} connected to V_{PPB} with 1µF capacitor, $V_{\overline{LDO\_EN}}$ = 0V, V_{CC0} = 0V, V_{CC1} = 0V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
T/R Switch Harmonic Distortion (MAX14808)	THD_{TRSW}	R_{LOAD} = 200Ω, V_{SIGNAL} = 100mV_{P-P}		-50		dB
T/R Switch Turn-On/Off Voltage Spike (MAX14808)	V_{SPIKE}	R_{LOAD} = 1kΩ at both sides of T/R switch		50		mV
Crosstalk	CT	f = 5MHz, adjacent channels, $R_{LOUT\_}$ = 200Ω		-51		dB

Note 2: All devices are 100% production tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design.
Note 3: Maximum operating current from $V_{GN\_}$ and $V_{GP\_}$ external power sources can vary depending on application requirements. The suggested minimum values assume 8 channels running in continuous transmission (CWD) at 5MHz with CC0 = CC1 = high.
Note 4: CW Doppler: continuous wave, f = 5MHz, V_{DD} = +3V, V_{CC} = -V_{EE} = +5V, $V_{PP\_}$ = -$V_{NN\_}$ = +5V.
Note 5: B mode: f = 5MHz, PRF = 5kHz, 1 period, V_{DD} = +3V, V_{CC} = -V_{EE} = +5V, $V_{PP\_}$ = -$V_{NN\_}$ = +100V.
Note 6: T/R switch turn-off time is the time required to switch off the bias current of the T/R switch. The off-isolation is not guaranteed.

时序图

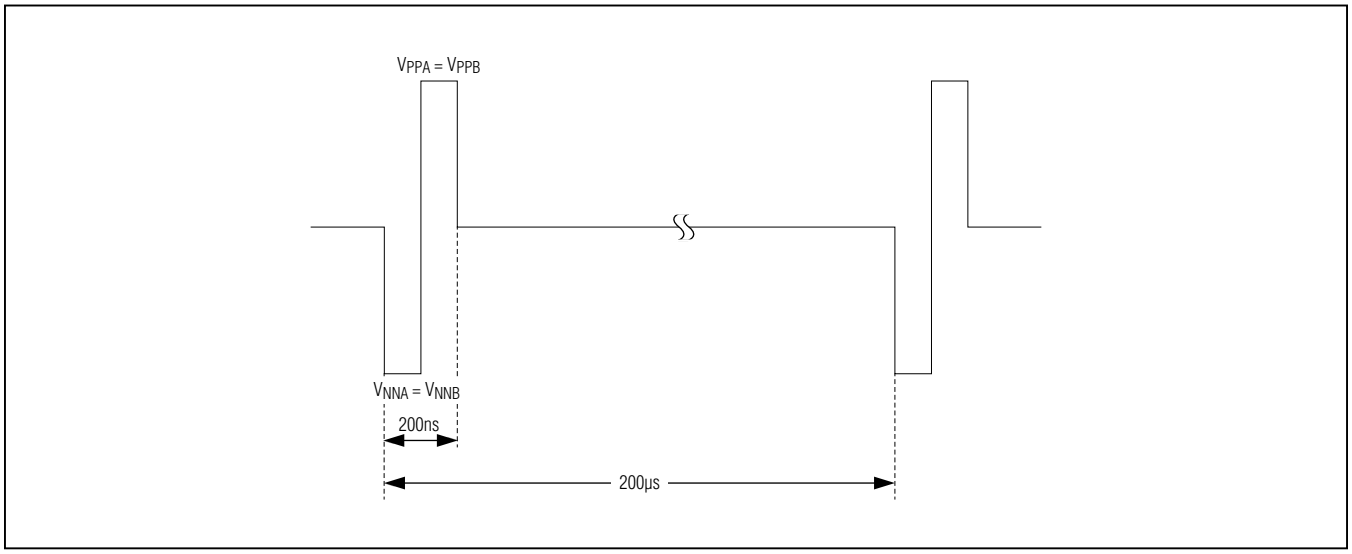


图1a. 高压突发测试(三级)

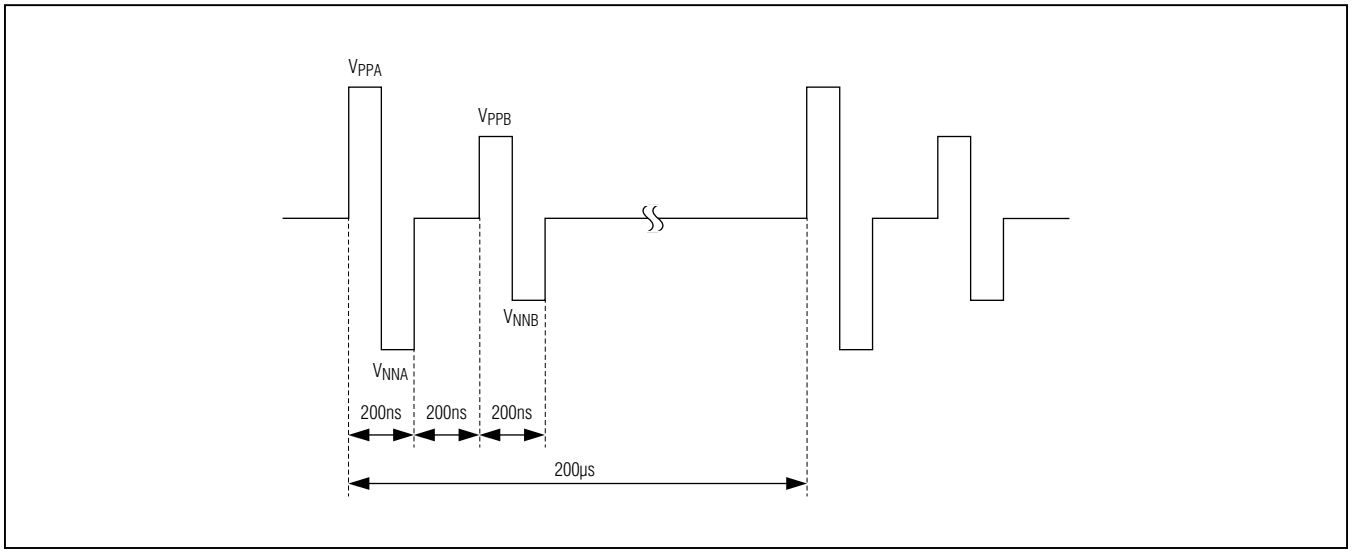


图1b. 高压突发测试(五级)

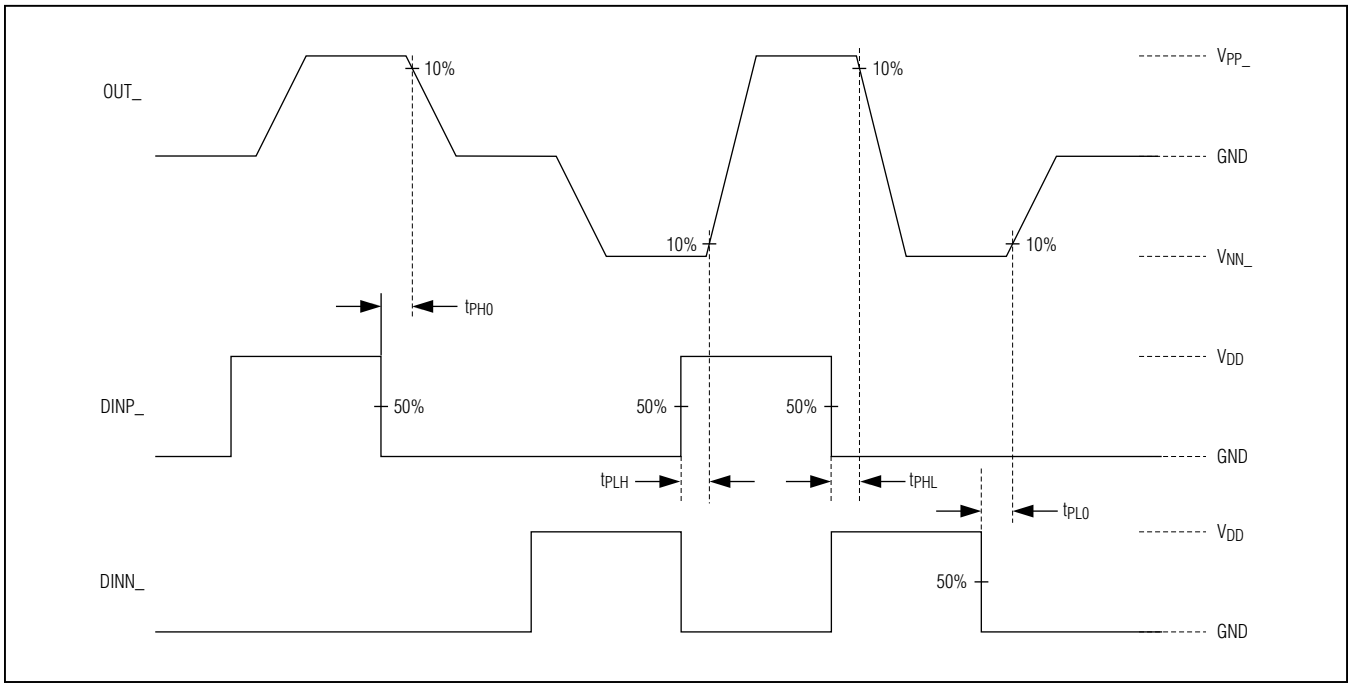


图2a. 传输延时

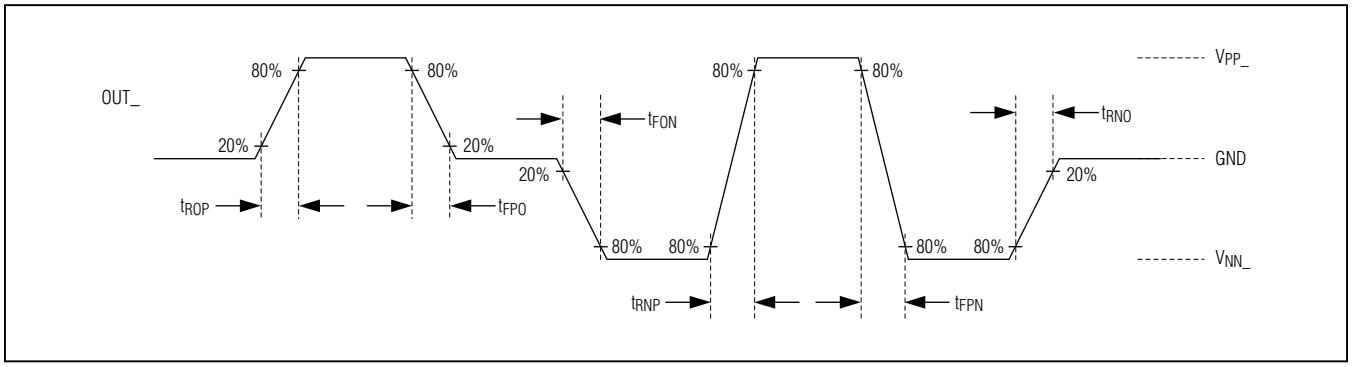


图2b. 输出上升/下降时间

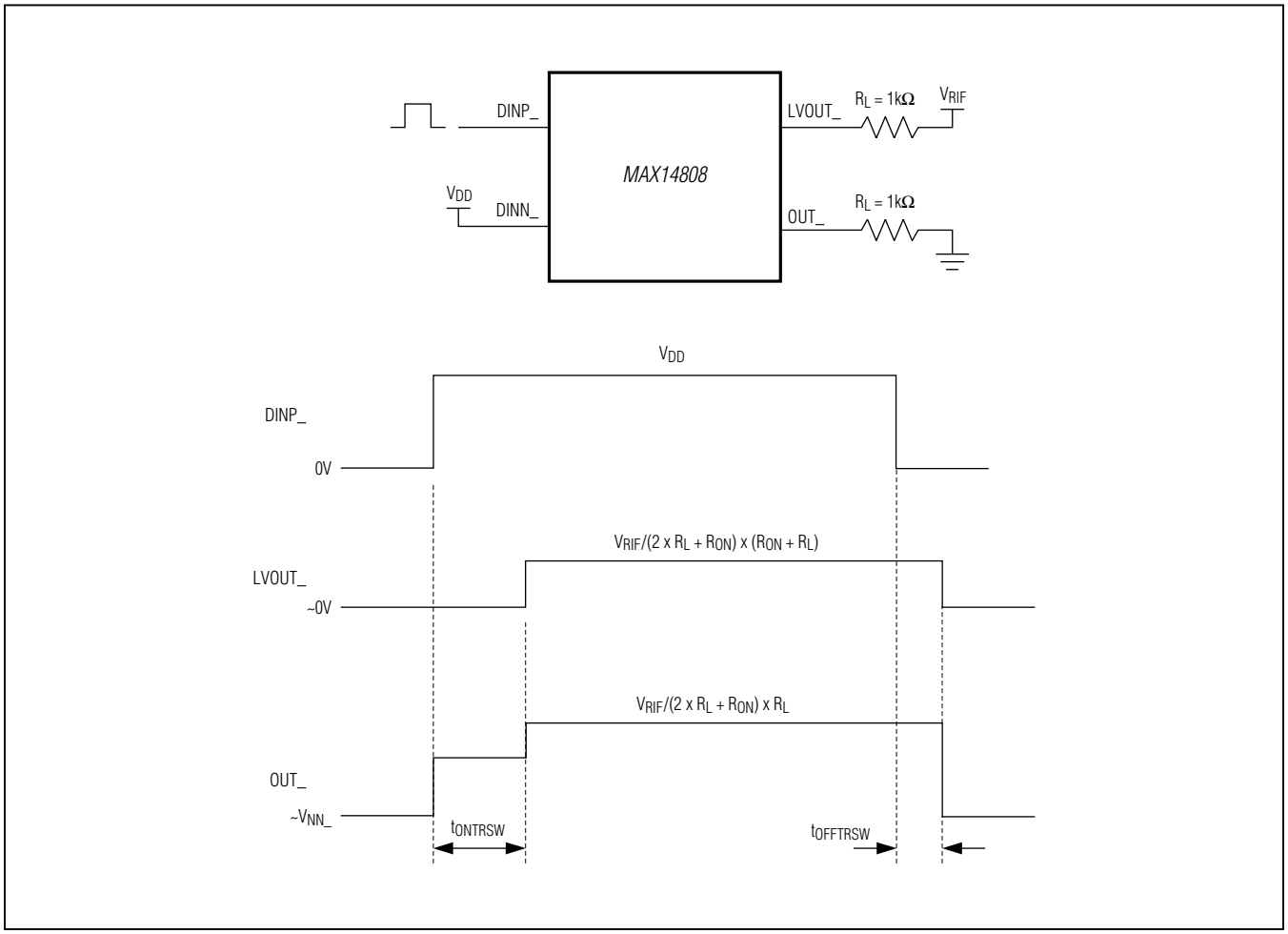


图3. T/R开关导通/关断

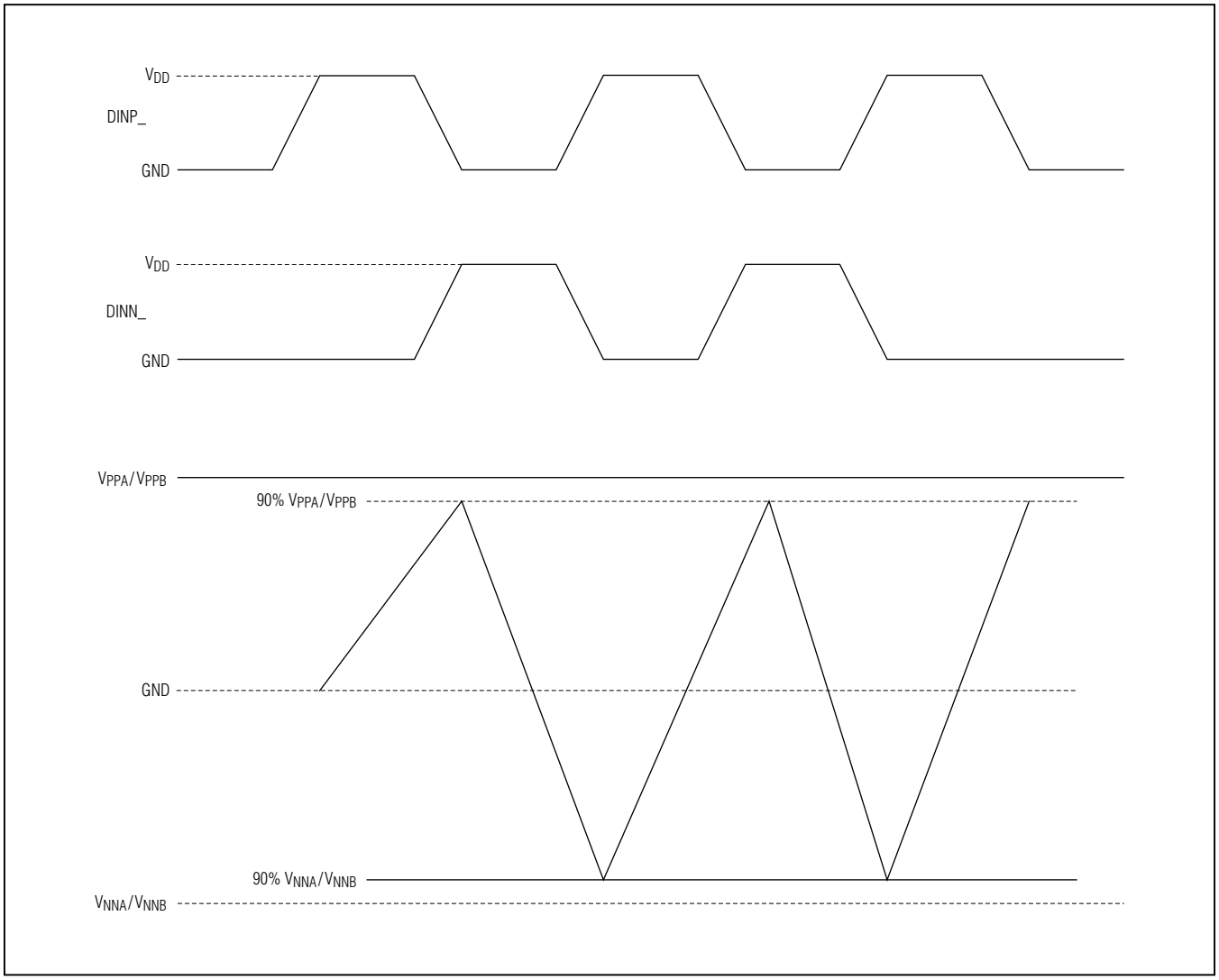

VDD
DINP_
GND
VDD
DINN_
GND
VPPA/VPPB
90% VPPA/VPPB
GND
90% VNNA/VNNB
VNNA/VNNB

图4. 带宽

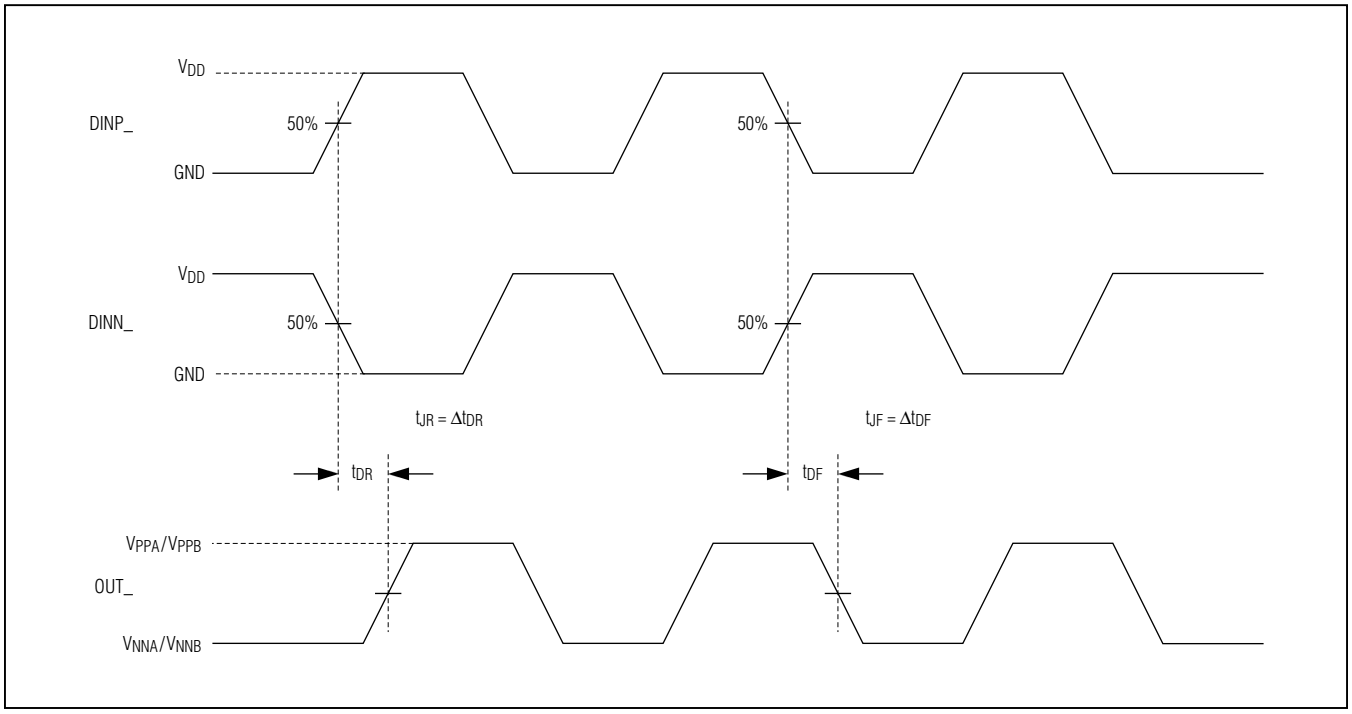
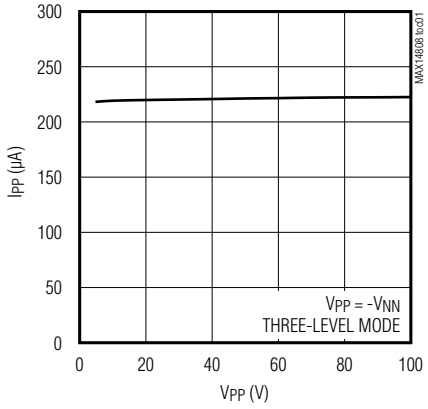


图5. 抖动时间

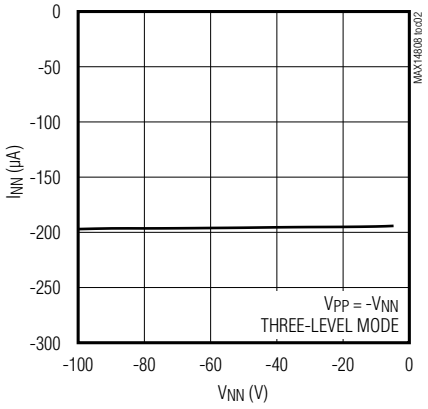
典型工作特性

(V_{DD} = +5V, V_{CC} = +5V, V_{EE} = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.)

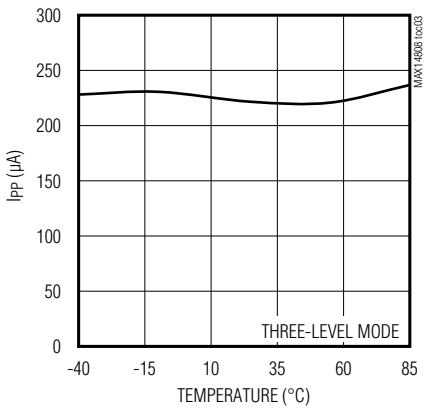
IPP QUIESCENT CURRENT vs. VPP



INN QUIESCENT CURRENT vs. VNN



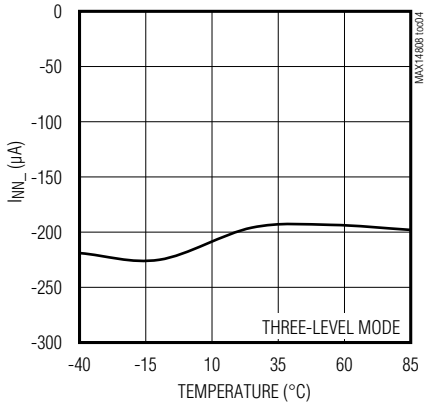
IPP QUIESCENT CURRENT vs. TEMPERATURE



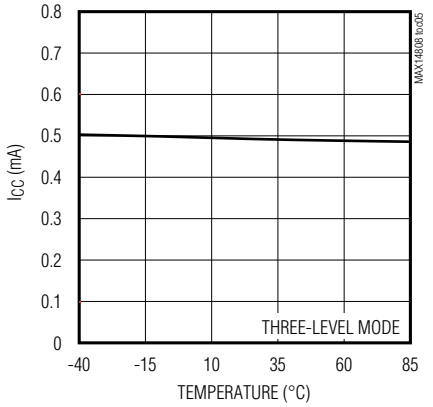
典型工作特性(续)

(V_{DD} = +5V, V_{CC} = +5V, V_{EE} = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.)

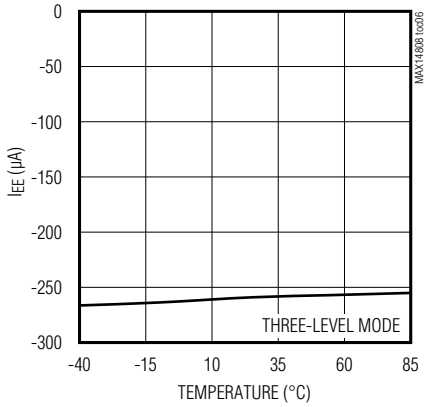
$I_{NN\_}$ QUIESCENT CURRENT vs. TEMPERATURE



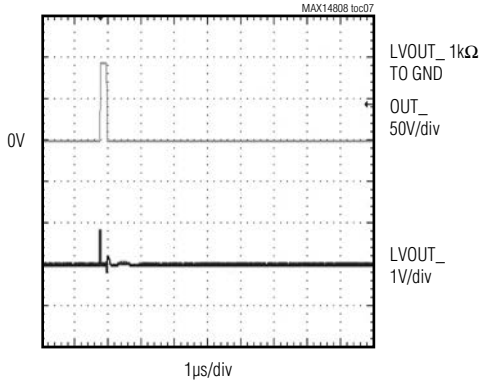
I_{CC} QUIESCENT CURRENT vs. TEMPERATURE



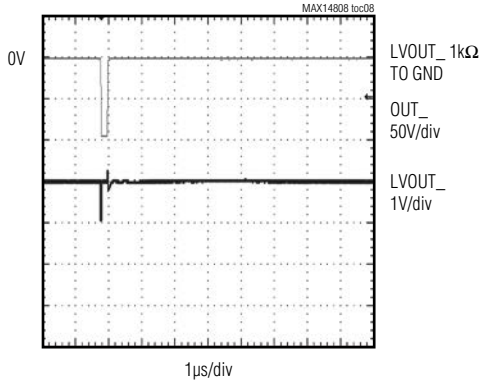
I_{EE} QUIESCENT CURRENT vs. TEMPERATURE



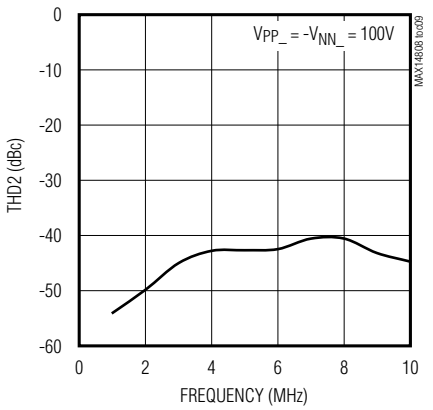
LOW TO HIGH TRANSITION VOLTAGE SPIKE



HIGH TO LOW TRANSITION SPIKE



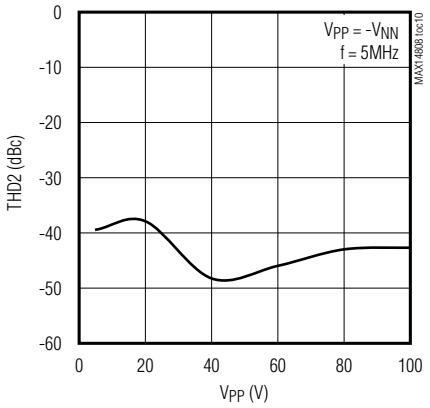
THD2 vs. FREQUENCY



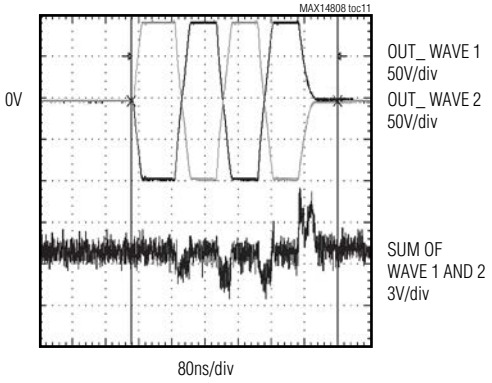
典型工作特性(续)

(V_{DD} = +5V, V_{CC} = +5V, V_{EE} = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.)

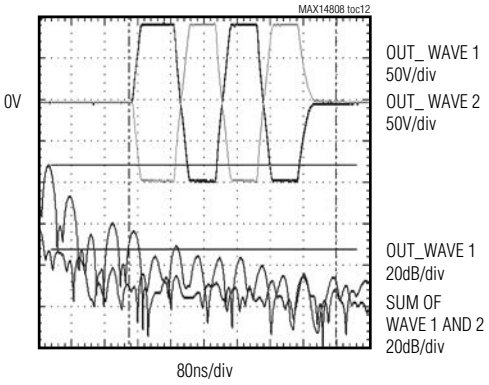
THD2 vs. VPP



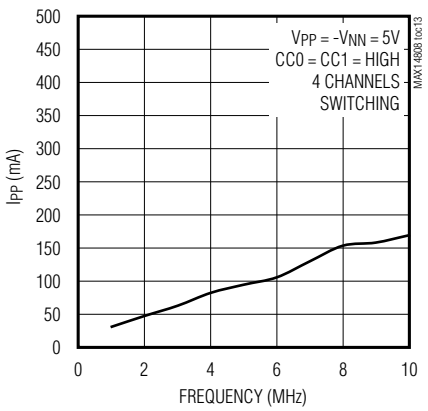
PULSE CANCELLATION



PULSE CANCELLATION FFT



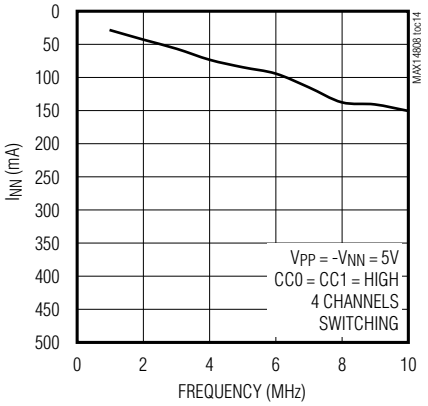
IPP vs. FREQUENCY



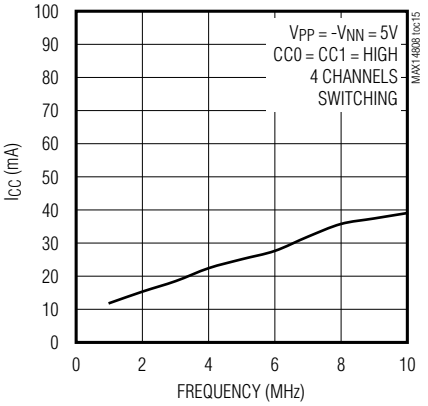
典型工作特性(续)

(V_{DD} = +5V, V_{CC} = +5V, V_{EE} = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.)

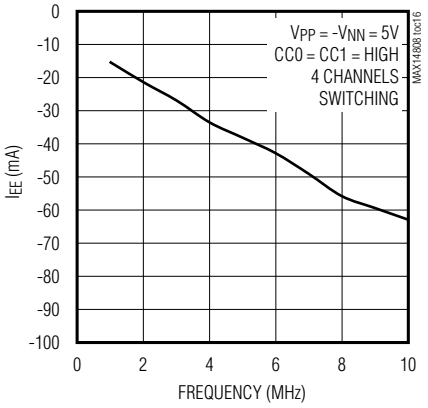
I_{NN} vs. FREQUENCY



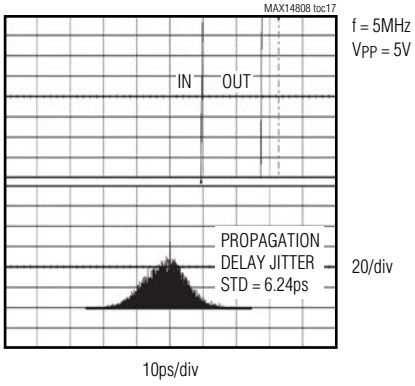
I_{CC} vs. FREQUENCY



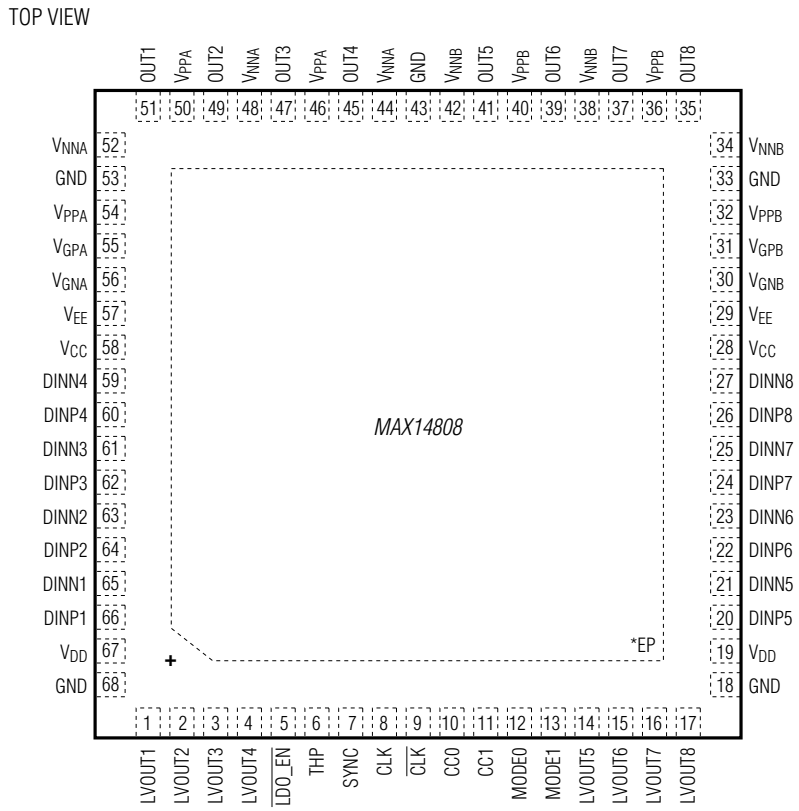
I_{EE} vs. FREQUENCY



OUTPUT JITTER



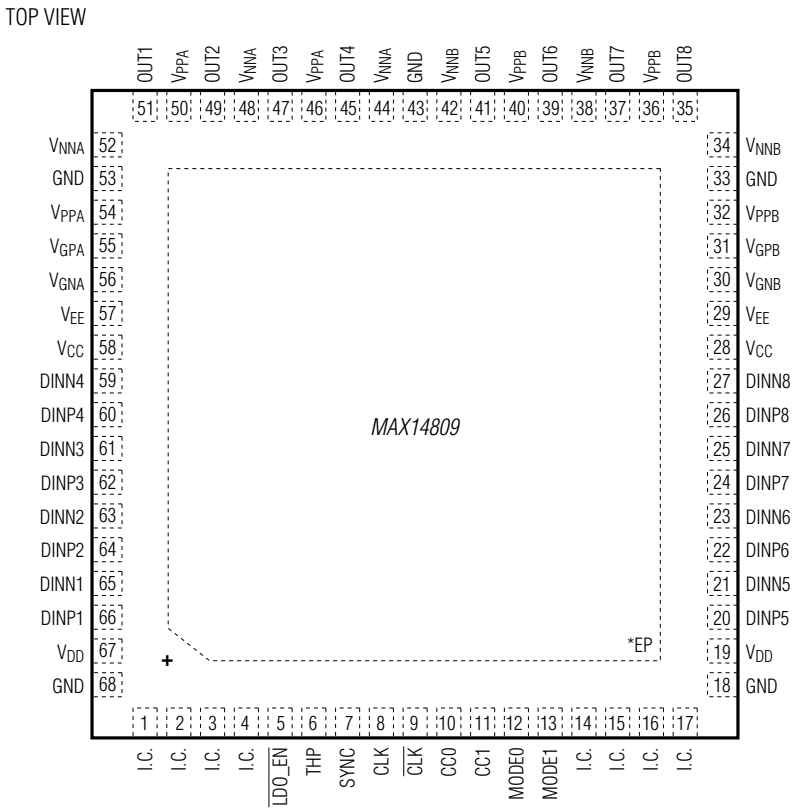
引脚配置



TQFN
(10mm x 10mm x 0.75mm)

*CONNECT EP TO GND

引脚配置(续)



TQFN
(10mm x 10mm x 0.75mm)

*CONNECT EP TO GND

引脚说明

引脚		名称	功能
MAX14808	MAX14809		
1	—	LVOUT1	低压T/R开关输出1
2	—	LVOUT2	低压T/R开关输出2
3	—	LVOUT3	低压T/R开关输出3
4	—	LVOUT4	低压T/R开关输出4
—	1–4, 14–17	I.C.	内部连接，通过外部将I.C.连接至GND。
5	5	$\overline{\text{LDO\_EN}}$	内部电源发生器控制输入。使用V_{GPA}、V_{GPB}、V_{GNA}和V_{GNB}上的外部电源时，如果将$\overline{\text{LDO_EN}}$驱动为高电平，则禁止内部电源。LDO_EN具有10kΩ内部下拉电阻，下拉至GND。
6	6	THP	热保护开漏输出。结温超过+150°C时，触发THP报警，可吸收3mA电流至GND。
7	7	SYNC	CMOS控制输入。将SYNC驱动为高电平时使能时钟输入模式；将SYNC驱动为低电平时工作在透明传输模式(见*真值表*部分)。
8	8	CLK	CMOS控制输入，时钟同相输入。差分时钟模式下，在CLK和$\overline{\text{CLK}}$的上升沿移入数据；单端时钟模式下，在CLK上升沿移入数据。时钟最大频率为160MHz。
9	9	$\overline{\text{CLK}}$	CMOS控制输入，时钟反相输入。差分时钟模式下，在CLK和$\overline{\text{CLK}}$的上升沿移入数据。时钟最大频率为160MHz。如果将$\overline{\text{CLK}}$连接至GND，CLK输入为单端逻辑时钟输入；否则，CLK和$\overline{\text{CLK}}$为自偏压差分时钟输入。
10	10	CC0	电流控制输入，控制电流驱动(见*真值表*部分)。
11	11	CC1	电流控制输入，控制电流驱动(见*真值表*部分)。
12	12	MODE0	模式控制输入，控制工作模式(见*真值表*部分)。
13	13	MODE1	模式控制输入，控制工作模式(见*真值表*部分)。
14	—	LVOUT5	低压T/R开关输出5。
15	—	LVOUT6	低压T/R开关输出6。
16	—	LVOUT7	低压T/R开关输出7。
17	—	LVOUT8	低压T/R开关输出8。
18, 33, 43, 53, 68	18, 33, 43, 53, 68	GND	地。
19, 67	19, 67	V_{DD}	逻辑电路供电电源，利用0.1µF电容将V_{DD} (两个引脚)旁路至GND，尽量靠近器件放置电容。
20	20	DINP5	数字信号输入5正端(见*真值表*部分)。
21	21	DINN5	数字信号输入5负端(见*真值表*部分)。
22	22	DINP6	数字信号输入6正端(见*真值表*部分)。
23	23	DINN6	数字信号输入6负端(见*真值表*部分)。
24	24	DINP7	数字信号输入7正端(见*真值表*部分)。
25	25	DINN7	数字信号输入7负端(见*真值表*部分)。
26	26	DINP8	数字信号输入8正端(见*真值表*部分)。
27	27	DINN8	数字信号输入8负端(见*真值表*部分)。

引脚说明(续)

引脚		名称	功能
MAX14808	MAX14809		
28, 58	28, 58	V_{CC}	V_{CC}电源电压，利用0.1µF电容将V_{CC} (两个引脚)旁路至GND，尽量靠近器件放置电容。
29, 57	29, 57	V_{EE}	V_{EE}电源电压，利用0.1µF电容将V_{EE} (两个引脚)旁路至GND，尽量靠近器件放置电容。
30	30	V_{GNB}	驱动器电压输出，将1µF电容连接至V_{NNB}，尽量靠近器件放置电容。
31	31	V_{GPB}	驱动器电压输出，将1µF电容连接至V_{PPB}，尽量靠近器件放置电容。
32, 36, 40	32, 36, 40	V_{PPB}	高压正电源输入，利用0.1µF电容将V_{PPB}旁路至GND，尽量靠近器件放置电容。
34, 38, 42	34, 38, 42	V_{NNB}	高压负电源输入，利用0.1µF电容将V_{NNB}旁路至GND，尽量靠近器件放置电容。
35	35	OUT8	脉冲发生器输出8。
37	37	OUT7	脉冲发生器输出7。
39	39	OUT6	脉冲发生器输出6。
41	41	OUT5	脉冲发生器输出5。
44, 48, 52	44, 48, 52	V_{NNA}	高压负电源输入，利用0.1µF电容将V_{NNA}旁路至GND，尽量靠近器件放置电容。
45	45	OUT4	脉冲发生器输出4。
46, 50, 54	46, 50, 54	V_{PPA}	高压正电源输入，利用0.1µF电容将V_{PPA}旁路至GND，尽量靠近器件放置电容。
47	47	OUT3	脉冲发生器输出3。
49	49	OUT2	脉冲发生器输出2。
51	51	OUT1	脉冲发生器输出1。
55	55	V_{GPA}	驱动器电压输出，将1µF电容连接至V_{PPA}，尽量靠近器件放置电容。
56	56	V_{GNA}	驱动器电压输出，将1µF电容连接至V_{NNA}，尽量靠近器件放置电容。
59	59	DINN4	数字信号输入4负端(见*真值表*部分)。
60	60	DINP4	数字信号输入4正端(见*真值表*部分)。
61	61	DINN3	数字信号输入3负端(见*真值表*部分)。
62	62	DINP3	数字信号输入3正端(见*真值表*部分)。
63	63	DINN2	数字信号输入2负端(见*真值表*部分)。
64	64	DINP2	数字信号输入2正端(见*真值表*部分)。
65	65	DINN1	数字信号输入1负端(见*真值表*部分)。
66	66	DINP1	数字信号输入1正端(见*真值表*部分)。
—	—	EP	裸焊盘，将EP连接至GND。不要将其作为一个电气连接点。

详细说明

MAX14808/MAX14809八通道三级电平/四通道五级电平高压(HV)脉冲发生器，利用低压控制逻辑输入产生高频、高压双极性脉冲(高达±105V)，用于驱动超声系统的压电传感器。全部八个通道均具有嵌入式过压保护二极管和集成有源归零箝位电路。两款器件均内置独立(浮地)电源(FPS)和电平转换器，用于实现信号转换，无需外部高压电容。MAX14808有八个集成的发送/接收(T/R)开关，MAX14809没有T/R开关。

器件具有两种工作模式：八通道三级电平脉冲发生器(集成有源归零箝位)或四通道五级电平脉冲发生器。作为八通道三级电平脉冲发生器时，每个通道由两路逻辑输入(DINN_/DINP_)控制，有源归零箝位的电流为脉冲发生器的电流的一半，1A (典型值)；作为四通道五级电平脉冲发生器时，每个通道由三路逻辑输入控制，有源归零电流与脉冲发生器电流相同，2A (典型值)。

器件可工作在锁定或透明模式。锁定模式下，数据输入与稳定的差分或单端时钟同步，以降低与FPGA输出信号相关的相位噪声，有助于多普勒分析；透明模式下，禁止同步功能，经过18ns延时后输出对应于输入的信号。两款器件均具有可调节最大电流(0.5A至2A)，不需要满幅电流时可降低功耗。

器件具有集成的高压毛刺箝位二极管(低寄生电容)，用于接收(Rx)和发送(Tx)隔离。两款器件均具有阻尼电路，可在发送突发结束后立即激活。阻尼电路的典型导通电阻为500Ω，对高压毛刺箝位二极管之前的脉冲发生器输出内部节点完全放电。

工作模式

器件具有四种工作模式：关断、八通道三级电平、四通道五级电平，以及禁止发送模式。利用MODE0和MODE1输入选择工作模式。

真值表

表1. 关断模式(MODE0 = 低电平，MODE1 = 低电平)

INPUTS		OUTPUTS	
DINN_	**DINP_**	**OUT_**	**LVOUT_ (MAX14808 ONLY)**
X	X	High impedance	High impedance (T/R switch off)

X = 无关。

表2. 八通道三级电平模式(MODE0 = 高电平，MODE1 = 低电平，V_{NNA} = V_{NNB}，V_{PPA} = V_{PPB})

INPUTS		OUTPUTS	
DINN_	**DINP_**	**OUT_**	**LVOUT_ (MAX14808 ONLY)**
0	0	Clamp on (damp off)	T/R switch off (LVOUT_ = GND)
1	0	V_{NNA}/V_{NNB} (damp off)	T/R switch off (LVOUT_ = GND)
0	1	V_{PPA}/V_{PPB} (damp off)	T/R switch off (LVOUT_ = GND)
1	1	Clamp on (damp on)	T/R switch on

0 = 逻辑低，1 = 逻辑高。

表3. 四通道五级电平模式(MODE0 = 低电平，MODE1 = 高电平) (注7)

INPUTS				OUTPUTS		
DINNx x = 1, 2, 3, 4	**DINPx x = 1, 2, 3, 4**	**DINNy y = 5, 6, 7, 8**	**DINPy y = 5, 6, 7, 8**	**OUTx = OUTy**	**LVOUTy y = 1, 2, 3, 4 (MAX14808 ONLY)**	**LVOUTy y = 5, 6, 7, 8 (MAX14808 ONLY)**
0	0	X	0	High impedance (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
0	0	X	1	Clamp on (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
0	1	0	X	V_{PPB} (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
1	0	0	X	V_{NNB} (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
0	1	1	X	V_{PPA} (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
1	0	1	X	V_{NNA} (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
1	1	1	X	Clamp on (damp on)	T/R switch on	T/R switch off

X = 无关，0 = 逻辑低，1 = 逻辑高。

***注7**: 对于五级电平、双模式工作，只需要三路控制输入(DINNx、DINPx、DINNy)。DINPy可连接至GND或VDD。*

表4. 禁止发送模式(MODE0 = 高电平，MODE1 = 高电平)

INPUTS		OUTPUTS	
DINN_	**DINP_**	**OUT_**	**LVOUT_ (MAX14808 ONLY)**
0	0	High impedance (damp off)	T/R switch off (LVOUT_ = GND)
1	0	High impedance (damp off)	T/R switch off (LVOUT_ = GND)
0	1	High impedance (damp off)	T/R switch off (LVOUT_ = GND)
1	1	High impedance (damp on)	T/R switch on

0 = 逻辑低，1 = 逻辑高。

关断模式

禁止全部通道，不能进行发送和接收。该模式下功耗最低。

八通道三级电平模式

器件工作在八路独立通道，每个通道均可产生三级脉冲。每通道的高边和低边FET能够提供2.0A电流，箝位电路能够产生1A电流。

四通道双模式

器件工作在四路独立通道，每个通道均可产生五级脉冲。器件采用独立的两路电源(V_{NNA}、V_{NNB}、V_{PPA}和V_{PPB})供电，产生摆幅在GND、V_{PPA}和V_{NNA}之间或GND、V_{PPB}和V_{NNB}之间的脉冲。每个通道的高边和低边以及箝位电路能够提供2.0A电流。

禁止发送模式

禁止全部八路高压发送通道，不能发送脉冲。T/R开关(仅限MAX14808)可导通(接收低压信号)或关断(隔离)。

电流驱动选择

可设置器件脉冲发生器的电流驱动能力，两个控制输入(CC0、CC1)控制电流驱动大小(表5)。

表5. 电流驱动选择

INPUTS		PULSER OUTPUT CURRENT (typ)
CC0	CC1	
0	0	2A
1	0	1.5A
0	1	1A
1	1	0.5A

同步功能

器件可利用稳定的时钟信号同步所有数据输入通道。超声系统中，FPGA输出信号往往容易受到高抖动的影响。抖动产生相位噪声，不利于多普勒分析。输入时钟可为差分信号或单端信号，最高160MHz。在CLK输入的上升沿($\overline{CLK}$下降沿)移入数据。将$\overline{CLK}$接GND时，为单端工作模式。同步功能可由SYNC控制输入使能或禁止。将SYNC输入驱动为低电平时，禁止同步功能(无外部时钟信号)；将SYNC输入驱动为高电平时，使能同步功能(需外接时钟信号)，图6所示为CLK和$\overline{CLK}$输入电路的简化原理图。

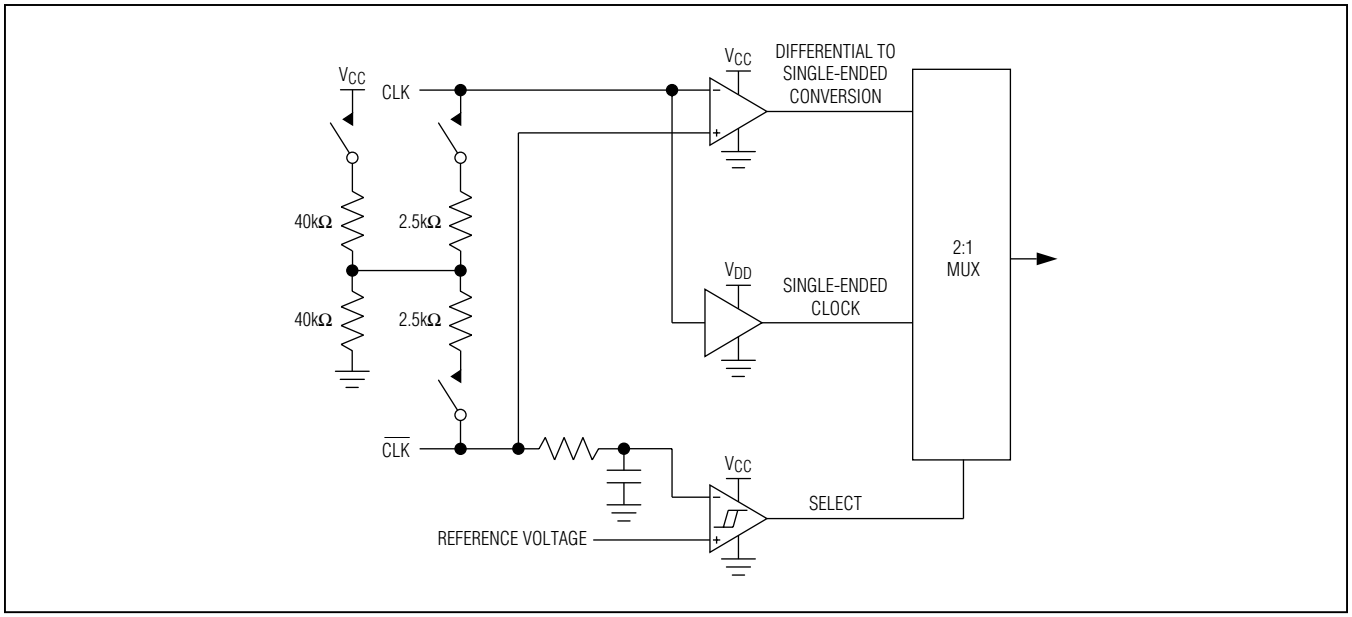


图6. CLK和$\overline{CLK}$输入简化原理图

T/R开关(MAX14808)

每个通道都具有低功耗T/R开关，T/R开关在传输后的恢复时间小于1.2µs。T/R开关同样受控于脉冲发生器的数字输入(见*真值表*部分)，无需专用的输入信号开启/关闭T/R开关。集成T/R开关无需任何特殊时序，可与数字脉冲器同步工作。为减小传输期间的漏电流，建议在开启一次突发发送模式之前将T/R开关关断3µs。

高压毛刺箝位二极管

每个脉冲发生器的输出端有一对反向并联配置的二极管(即高压毛刺箝位二极管)。二极管的反向电容极低，在接收通路与实际脉冲发生器输出之间实现完美隔离。

有源阻尼电路

内部脉冲发生器输出节点(高压毛刺箝位二极管之前)和GND之间集成有源阻尼电路。该电路用于对脉冲发生器输出内部节点的放电，使二极管在突发发送结束后快速退出高阻状态。这样做主要有两个好处：

1) 高压毛刺箝位二极管隔离更有效。

2) 抑制节点的低频振荡，有助于提高多普勒性能。

独立(浮地)电源使能($\overline{LDO\_EN}$)

器件具有$\overline{LDO_EN}$控制输入，以使能/禁止内部FPS。允许使用外部高性能电源，以节省系统功耗。只有要求极低功耗的特殊应用中，才会考虑该选项，低功耗嵌入式FPS能够满足大多数情况的功耗要求。将$\overline{LDO_EN}$驱动为低电平或保持浮空时，使能内部FPS；将$\overline{LDO_EN}$驱动为高电平时，禁止内部FPS。

温度报警输出

器件具有一路热保护开漏输出(THP)。内部结温超过+150°C时，器件自动进入关断模式，触发THP报警指示；管芯温度下降至+130°C以下时，器件重新进入常规工作模式，解除THP报警状态。

电源排序

使用嵌入式FPS时($\overline{LDO\_EN}$ = 低电平)，器件不要求任何上电/关断排序。使用外部FPS时($\overline{LDO\_EN}$ = 高电平)，整个上电/关断瞬间必须满足条件$V_{GP_} > (V_{EE} - 0.6V)$及$V_{GN_} < (V_{CC} + 0.6V)$ (见*Electrical Characteristics*表)。

应用信息

裸焊盘和布局

器件在TQFN封装的下方提供裸焊盘(EP)，以提高散热能力。通过外部将EP连接至GND，不要在封装下方布线，以免短路。为改善散热，将EP连接至PCB元件层的大尺寸焊盘。该焊盘应通过多个过孔连接到大面积散热覆铜区域，形成良好的散热通路。

器件的高速脉冲发生器要求在其电源输入连接低电感旁路电容。建议遵守高速PCB走线设计原则，注意采用最短走线长度及足够宽度，以减小电感。建议使用表贴元件。

典型应用电路

图7所示为MAX14808在八通道三级电平脉冲发送中的应用。

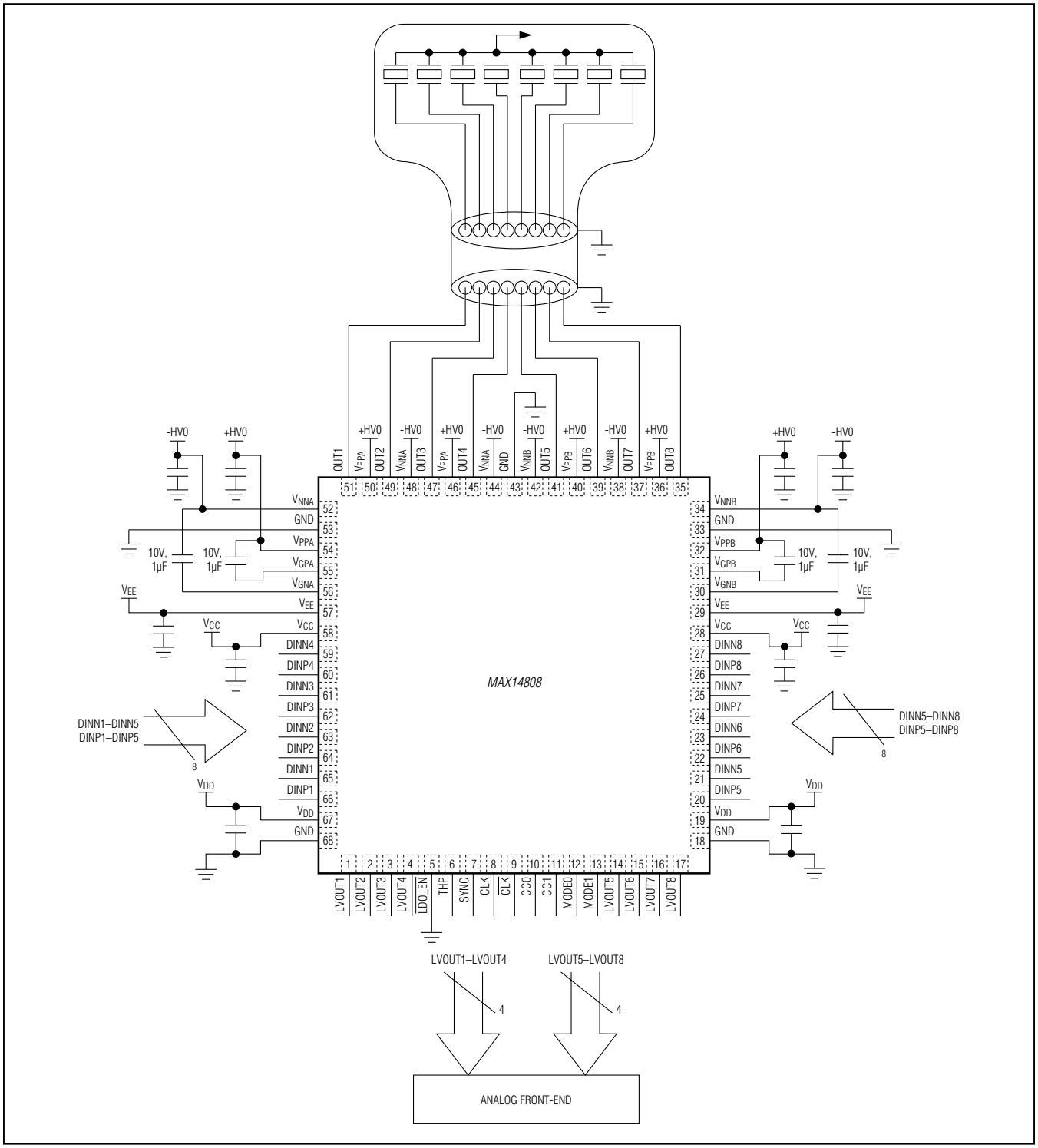
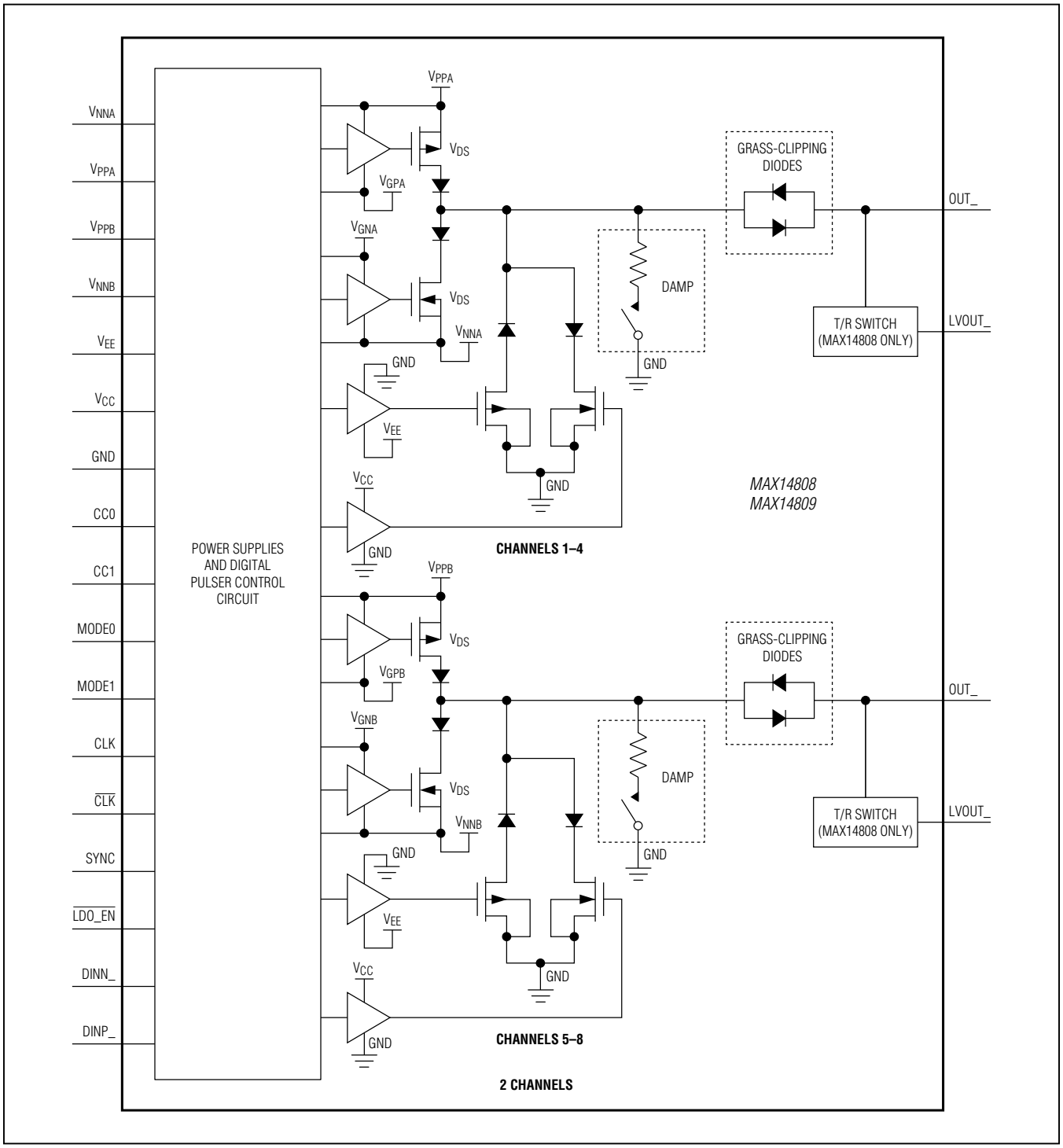


图7. 八通道三级电平脉冲应用(MAX14808)

功能框图


VNNA
VPPA
VPPB
VNNB
VEE
VCC
GND
CC0
CC1
MODE0
MODE1
CLK
CLK
SYNC
LDO_EN
DINN_
DINP_
POWER SUPPLIES AND DIGITAL PULSER CONTROL CIRCUIT
VPPA
VDS
VGPA
VGNA
VNNA
DAMP
GRASS-CLIPPING DIODES
OUT_
T/R SWITCH (MAX14808 ONLY)
LVOUT_
VEE
VCC
GND
MAX14808
MAX14809
CHANNELS 1–4
VPPB
VGPB
VGNB
VNNB
CHANNELS 5–8
2 CHANNELS

八通道3级电平/四通道5级电平高压2A数字脉冲发生器，带T/R开关

定购信息

器件	发送通道	T/R开关	温度范围	引脚–封装
MAX14808ETK+	Yes	Yes	-40°C至+85°C	68 TQFN-EP*
MAX14809ETK+	Yes	No	-40°C至+85°C	68 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*

芯片信息

PROCESS: BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询**china.maximintegrated.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
68 TQFN-EP	T6800+4	**21-0142**	**90-0101**

修订历史

修订号	修订日期	说明	修改页
0	9/12	最初版本。	—
1	3/13	更新了*DC电气特性*和*AC电气特性*表；更新了*典型工作特性*部分中的TOC 9；去掉了MAX14809*定购信息*中的未来产品记号。	5–8, 11, 17, 30

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