http://www.analog.com/zh/circuits-from-the-lab/CN0321/vc.html

CN0321: Fully Isolated, Single Channel Voltage and 4 mA to 20 mA Output with HART
CN0321：具有 HART 的完全隔离、单通道电压、4 mA 至 20 mA 输出

Benefits & Features
优势和特性

- Voltage and 4mA to 20mA output
  电压和 4mA 至 20mA 输出
- Fully isolated
  完全隔离
- HART connectivity
  HART 连接能力

Devices Connected/Referenced

连接/参考器件

AD5422 16-Bit Current and Voltage Output DAC

AD5422 16 位电流和电压输出 DAC

AD5700-1 Low Power HART Modem with Internal RC Oscillator

AD5700-1 集成内部 RC 振荡器的低功耗 HART 调制解调器

ADP2441 36 V, 1 A, Synchronous, Step-Down DC-to-DC Regulator

ADP2441 36 V、1 A 同步降压 DC-DC 稳压器

ADuM3471 Quad Isolator with Integrated Transformer Driver and PWM Controller

ADuM3471 集成变压驱动器和 PWM 控制器的四通道隔离器

ADuM3482 Small, 3.75 kV rms Quad Digital Isolator

ADuM3482 3.75 kV rms 小型四通道数字隔离器

EVALUATION AND DESIGN SUPPORT
评估和设计支持

Circuit Evaluation Boards

电路评估板

CN0321 Evaluation Board (EVAL-CN0321-SDPZ)

CN0321 评估板(EVAL-CN0321-SDPZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

系统演示平台(EVAL-SDP-CB1Z)

Design and Integration Files

设计和集成文件

Schematics, Layout Files, Bill of Materials

原理图、布局文件、物料清单

CIRCUIT FUNCTION AND BENEFITS

电路功能与优势

This circuit provides a complete, fully isolated, analog output channel suitable for programmable logic controllers (PLCs) and distributed control system (DCS) modules that require standard 4 mA to 20 mA HART®[1]-compatible current outputs and unipolar or bipolar output voltage ranges. It provides a flexible building block for channel-to-channel isolated PLC/DCS output modules or any other industrial application that requires a fully isolated analog output. The circuit also includes external protection on the analog output terminals.

该电路提供一款完整的、完全隔离、模拟输出通道，适合需要标准 4 mA 至 20 mA HART®[1] 兼容型电流输出和单极性/双极性输出电压范围的可编程逻辑控制器(PLC)和分布式控制系统(DCS)模块。它为通道间隔离 PLC/DCS 输出模块或其他所有需要完全隔离式模拟输出的工业应用提供了灵活的构建块。电路在模拟输出端还提供了外部保护功能。

The AD5422 16-bit digital-to-analog converter (DAC) is software configurable and provides all the necessary current and voltage outputs.

AD5422 16 位数模转换器(DAC)可通过软件配置，提供全部必须的电流和电压输出。

The AD5700-1, the industry's lowest power and smallest footprint HART-compliant IC modem, is used in conjunction with the AD5422 to form a complete HART-compatible 4 mA to 20 mA solution. The AD5700-1 includes a precision internal oscillator that provides additional space savings, especially in channel-to-channel isolated applications.

AD5700-1 是低功耗，小尺寸的 HART 兼容型 IC 调制解调器，与 AD5422 配合使用，组成完整的 HART 兼容型 4 mA 至 20 mA 解决方案。AD5700-1 集成内部精密振荡器，可额外节省空间，尤其在通道间隔离应用中。

PLC/DCS solutions must be isolated from the local system controller to protect against ground loops and to ensure robustness against external events. Traditional solutions use discrete ICs for both power and digital isolation. When multichannel isolation is needed, the cost and space of providing discrete power solutions becomes a big disadvantage. Solutions based on optoisolators typically have reasonable output regulation but require additional external components, thereby increasing board area. Power modules are often bulky and can provide poor output regulation. The circuit in Figure 1 uses the ADuM347x family of isolators and power regulation circuitry along with associated feedback isolation. External transformers are used to transfer power across the isolation barrier.

PLC/DCS 解决方案必须与本地系统控制器隔离，以防形成接地环路，同时确保不受外部事件影响。传统解决方案利用分立 IC 提供电源和数字隔离。当需要多通道隔离时，分立电源解决方案的成本和空间会变得非常不利。基于光隔离器的解决方案通常具有合理的输出调节，但需要额外的外部元件，因而会使电路板面积增大。电源模块常常体积庞大，而且输出调节可能不佳。图 1 中的电路使用 ADuM347x 系列隔离器和电源调节电路，以及相应的反馈隔离。使用外部变压器将功率传输到隔离栅的另一端。

The ADuM3482 provides the UART signal isolation for the AD5700-1.

ADuM3482 为 AD5700-1 提供 UART 信号隔离。

The ADP2441, 36 V step-down dc-to-dc regulator, accepts an industrial standard 24 V supply, with wide tolerance on the input voltage. It steps this down to 5 V to power all controller side circuitry. The circuit

also includes standard external protection on the 24 V supply terminals, as well as protection against dc overvoltage of +36 V down to −28 V.

ADP2441 是 36 V 降压 DC-DC 稳压器，采用工业标准 24 V 电源，具有宽输入电压容差。它可将电压降为 5 V，为所有控制器侧电路供电。该电路还在 24 V 电源端集成了标准外部保护，同时还可提供+36 V 至−28 V 的直流过压保护。

[1] HART is a registered trademark of the HART Communication Foundation.

[1] HART 是 HART 通信基金会的注册商标。

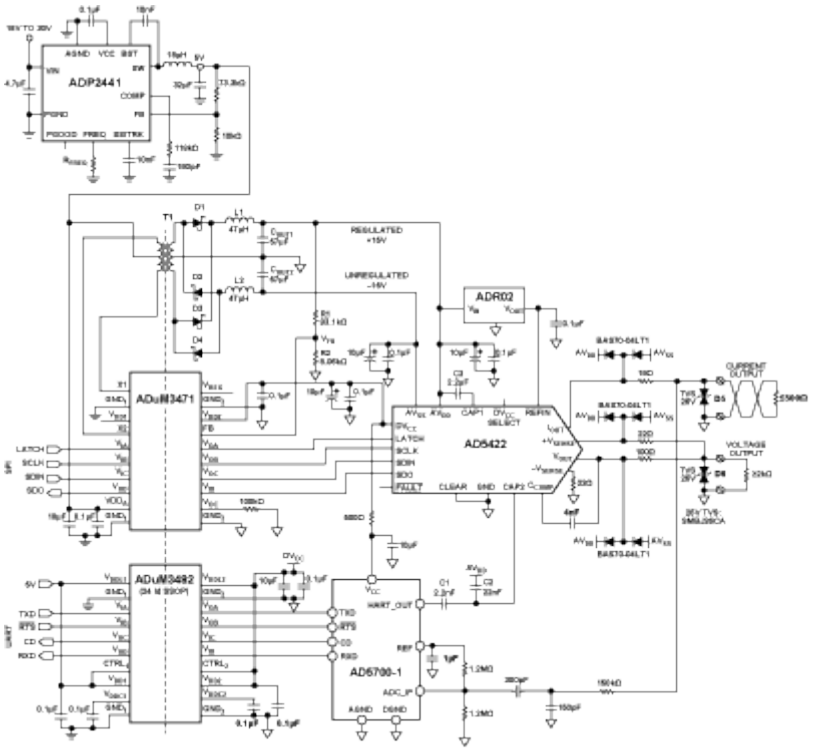

Figure 1. Functional Block Diagram (Simplified Schematic: All Connections and Decoupling Not Shown)

图 1. 功能框图（原理示意图：未显示所有连接和去耦）

Enlarge

放大

CIRCUIT DESCRIPTION

电路描述

Analog Output

模拟输出

For industrial control modules, standard analog output voltage and current ranges include ±5 V, ±10 V, 0 V to +5 V, 0 V to +10 V, +4 mA to +20 mA, and 0 mA to +20 mA. The AD5422 is a precision, fully

integrated 16-bit DAC that offers a programmable current source and programmable voltage output designed to meet the requirements of industrial process control applications.

对于工业控制模块，标准模拟输出电压和电流范围包括±5 V、±10 V、0 V 至+5 V、0 V 至+10 V、+4 mA 至+20 mA 和 0 mA 至+20 mA。AD5422 是精密、完全集成、16 位 ADC，内置可编程电流源和可编程电压输出，设计用于满足工业过程控制应用的需要。

The AD5422 provides all the output ranges previously listed, with the current output ranges and voltage output ranges available on separate pins. An overrange feature of 10% is available on all the voltage ranges, and a 0 mA to 20 mA overrange is available on the current output. Analog outputs are short- and open-circuit protected.

AD5422 提供前面列出的所有输出范围，电流输出范围和电压输出范围分别以独立引脚提供。针对所有电压范围提供 10%超量程功能，并且针对电流输出提供 0 mA 至 20 mA 超量程。模拟输出受短路和开路保护。

The AD5422 has an on-board 10 ppm/°C reference. For higher performance over temperature, this design uses an ADR02 reference. The ADR02 is a 5 V precision reference that allows for an input voltage of up to 36 V. It has a 0.05% maximum accuracy error and a 3 ppm/°C maximum temperature drift. This drift contributes approximately 0.02% error across the industrial temperature range.

AD5422 具有一个片上 10 ppm/°C 基准电压源。为了在额定温度范围内达到更高的性能，该设计使用了 ADR02 基准电压源。ADR02 是一款 5 V 精密基准电压源，允许高达 36 V 的输入电压。其最大精度误差为 0.05%，最大温度漂移为 3 ppm/°C。该漂移在工业温度范围内会贡献大约 0.02%误差。

The AD5422 allows for an internal or external precision, current setting resistor for the current output circuitry. This design uses the internal current sensing resistor option; however, even higher accuracy can be achieved by using a precision external 15 kΩ resistor.

AD5422 支持以内部或外部精密电流设置电阻作为电流输出电路。本设计使用内部电流检测电阻选项；但通过使用精密外部 15 kΩ 电阻，可达到更高的精度。

By leaving the DV_{CC} SELECT pin of the AD5422 floating, an internal 4.5 V power supply is connected to the DV_{CC} pin which is used as a digital power supply for the AD5700-1 and the field side of the isolators. Alternatively, the 5 V output low dropout (LDO) regulator on the ADuM3471 can be used. The LDO provides a tighter regulated 5 V rail; however, it does not allow for dc overvoltages of greater than 20 V due to the absolute maximum ratings on the regulator input pin of the ADuM3471.

通过浮空 AD5422 的 DV_{CC} SELECT 引脚，内部 4.5 V 电源可连接至 DV_{CC} 引脚，用于 AD5700-1 的数字电源和隔离器的现场端。也可使用 ADuM3471 上的 5 V 输出型低压差(LDO)稳压器。LDO 提供更紧凑的 5 V 稳压供电轨；但由于 ADuM3471 稳压器输入引脚上的绝对最大额定值，它不允许高于 20 V 的直流过压。

The output connector configuration for the EVAL-CN0321-SDPZ hardware is shown in Table 1.

EVAL-CN0321-SDPZ 硬件的输出连接器配置见表 1。

Table 1. Output Terminals

Terminal Name	Output Type
OUT2	Voltage output ranges
GND	Ground
OUT1	Current output ranges

HART Compatibility

HART 兼容性

The AD5700-1 is used in conjunction with the AD5422 to form a complete HART-compatible 4 mA to 20 mA solution. The AD5700-1 0.5% precision internal oscillator provides significant space savings in channel-to-channel isolated applications where a clock crystal would otherwise be needed per channel. The crystal would typically be bigger than the AD5700-1 IC itself; therefore, the internal oscillator results in significant space saving.

AD5700-1 与 AD5422 搭配使用，组成完整的 HART 兼容型 4 mA 至 20 mA 解决方案。AD5700-1 是 0.5% 精密内部振荡器，可极大节省通道间隔离的应用空间；这类应用原本需要针对每通道使用时钟晶体。晶体通常比 AD5700-1 IC 本身要大；因此，内部振荡器节省下来的面积空间是巨大的。

The HART modem output is attenuated by C1 and C2 and ac-coupled into the AD5422 via the CAP2 pin. Additional information can be found in the AN-1065 Application Note. Circuit Note CN-0278 describes an alternate HART coupling method using the R_{SET} pin that offers greater power supply rejection; however, it requires an external precision current setting resistor.

HART 调制解调器输出通过 C1 和 C2 衰减，并通过 CAP2 引脚交流耦合至 AD5422。其他信息参见 AN-1065 应用笔记。电路笔记 CN-0278 描述了一种使用 R_{SET} 引脚的替代 HART 耦合方式，具有更高的电源抑制性能，但需要使用一个外部精确电流设置电阻。

Isolated Power

隔离电源

The voltage output headroom required by the AD5422 is 0.8 V maximum, and the current output needs a 2.5 V headroom maximum. Therefore, a >12.5 V supply is required to output a 20 mA current through a 500 Ω load. In this design, the minimum supply voltage (overtemperature) is no lower than 13.5 V, which allows for some additional headroom.

AD5422 需要的电压输出裕量最大值为 0.8 V，并且电流输出需要最大值为 2.5 V 的裕量。因此，需要一个大于 12.5 V 的电源，以便通过 500 Ω 负载输出 20 mA 电流。在本设计中，最小电源电压（过温）不超过 13.5 V，允许具有一定裕量。

The ADuM347x devices are quad-channel digital isolators with integrated pulse-width modulation (PWM) controllers and low impedance transformer drivers (X1 and X2). The only additional components required for an isolated dc-to-dc converter are a transformer and simple full-wave diode rectifier. The devices provide up to 2 W of regulated, isolated power when supplied from a 5.0 V or 3.3 V input, which eliminates the need for a separate isolated dc-to-dc converter.

ADuM347x 为四通道数字隔离器，集成脉冲宽度调制(PWM)控制器和低阻抗变压驱动器（X1 和 X2）。隔离式 DC/DC 转换器仅需要以下额外器件：变压器和简单的全波二极管整流器。采用 5.0 V 或 3.3 V 输入电源时，器件最多可提供 2 W 的调节隔离功率，因而无需另外使用隔离式 DC-DC 转换器。

The iCoupler® chip-scale transformer technology is used to isolate the logic signals, and the integrated transformer driver with isolated secondary side control provides high efficiency for the isolated dc-to-dc converter. The internal oscillator frequency is adjustable from 200 kHz to 1 MHz and is determined by the R_{OC} value. When R_{OC} = 100 kΩ, the switching frequency is 500 kHz.

iCoupler®芯片级变压器技术用于隔离逻辑信号；集成的变压器驱动器带隔离副边控制功能，可以提高隔离式 DC/DC 转换器的效率。内部振荡器频率可以在 200 kHz 至 1 MHz 范围内调整，由 R_{OC} 的值决定。当 R_{OC} = 100 kΩ 时，开关频率为 500 kHz。

The ADuM3471 regulation is from the positive 15 V supply. The feedback for regulation is from the divider network (R1 and R2). The resistors are chosen such that the feedback voltage is 1.25 V when the output voltage is 15 V. The feedback voltage is compared with the ADuM3471 internal feedback setpoint voltage of 1.25 V. Regulation is achieved by varying the duty cycle of the PWM signals driving the external transformer.

ADuM3471 调节来自 15 V 正电源。调节反馈来自分压器网络（R1 和 R2）。电阻根据以下要求选择：当输出电压为 15 V 时，反馈电压为 1.25 V。反馈电压与 ADuM3471 内部反馈设定点电压 1.25 V 相比较。调节通过改变驱动外部变压器的 PWM 信号的占空比来实现。

The negative supply is loosely regulated and could potentially be as low as −26.4 V if unloaded. For this reason, a 25 V Zener diode was placed on the negative supply. This diode draws a small current from the supply when it is lightly loaded; however, it ensures that it clamps at around 25 V

负电源的调节不太严格，且空载时可能低至−26.4 V。因此，在负电源处放置一个 25 V 齐纳二极管。轻载时，二极管从电源获取小电流，但可确保其箝位在 25 V 左右。

Another approach is to use an isolation transformer with a 4:1 turns ratio; when it is unloaded, the negative rail does not go as low. In applications that require higher compliance voltages or very low power dissipation, a different power supply design should be considered.

另一种方法是使用匝数比为 4:1 的隔离式变压器；当其空载时，负供电轨不会过低。在要求较高顺从电压或极低功耗的应用中，应当考虑其它电源设计。

Input Power

输入功率

The circuit in Figure 1 is powered by a 24 V supply. The ADP2441 is used to step the 24 V down to 5 V to supply all controller side circuitry.
图 1 中的电路采用 24 V 电源供电。ADP2441 用于将 24 V 降压为 5 V，为所有控制器侧电路供电。

The ADP2441 can accept up to 36 V, reliable transient protection of the supply input is also more easily achieved.
ADP2441 可接受最高 36 V 的电压，并且可更加轻松地达到可靠的电源输入瞬变保护。

The ADP2441 also features a number of other safety/reliability functions, such as undervoltage lockout (UVLO), a precision enable feature, a power good pin, and overcurrent limit protection. It can achieve up to 90% efficiency for an input of 24 V and an output of 5 V.
ADP2441 还具有其他各种安全性/可靠性功能，如欠压闭锁(UVLO)、精确使能特性、电源良好引脚和过流限值保护。对于 24 V 输入和 5 V 输出，它能达到最高 90%效率。

Isolation

隔离

The ADuM3471 power isolation circuitry includes four fully isolated voltage channels with a 2.5 kV isolation rating. These four channels are used to isolate the four data lines (SCLK, LATCH, SDIN, and SDO) of the AD5422. Isolation of the SDO line is not essential for the operation of the circuit; however, it does allow access to diagnostic and fault features, as well as register readback.

ADuM3471 电源隔离电路包括四个完全隔离的电压通道，隔离额定值为 2.5 kV。这四个通道用于隔离

AD5422 的四条数据线路（SCLK、LATCH、SDIN 和 SDO）。SDO 线路隔离对于电路运行而言并非必要，但允许访问诊断和故障特性，以及寄存器回读。

The ADuM3482 is a 3.75 kV quad channel digital isolator in a small 20-lead SSOP package (7.2 mm × 7.8 mm). The ADuM3482 core operates between 3.0 V and 5.5 V, whereas the I/O supply can range from 1.8 V to 5.5 V. These devices can be used to interface directly with 1.8 V logic. This isolator is used to isolate the UART signals for the AD5700-1 HART modem.

ADuM3482 是一款 3.75 kV 四通道数字隔离器，采用小型 20 引脚 SSOP 封装(7.2 mm × 7.8 mm)。ADuM3482 内核工作电压范围为 3.0 V 至 5.5 V，而 I/O 电源范围为 1.8 V 至 5.5 V。这些器件可用于直接与 1.8 V 逻辑器件接口。该隔离器用于隔离 AD5700-1 HART 调制解调器的 UART 信号。

Further information on *i*Coupler products is available at www.analog.com/icoupler.
有关 *i*Coupler 产品的更多信息，请访问 www.analog.com/icouplers。

DC Overvoltage Protection
直流过压保护

The circuit in Figure 1 allows for continuous +36 V and −28 V dc overvoltage protection. This means the circuit is protected in cases where a dc power supply line is accidentally connected to the output.
图 1 中的电路允许对+36 V 和−28 V 进行连续直流过压保护。这意味着，电路受直流电源线路意外连接输出的保护。

During an overvoltage condition, the supplies are pulled up or down via the external protection diodes. The resistance between these diodes and the output terminals limits the peak current.
在过压条件中，电源通过外部保护二极管拉高或拉低。这些二极管和输出端之间的电阻限制了峰值电流。

The maximum/minimum voltage on the output terminals is limited by the breakdown voltage on any circuitry connected to the output or power supplies. The current and voltage outputs of the AD5422 can tolerate +48 V down to−28 V. The AV_{SS} input can tolerate −28 V, and the AV_{DD} can tolerate +48 V. The ADR02 reference can tolerate 36 V on its supply. The ADC_IP pin of the AD5700-1 is protected by a 150 kΩ resistor that limits any current, followed by a 300 pF capacitor to block any dc current. Do not expose other ICs to higher voltages during the dc overvoltage condition.

输出端的最大/最小电压受限于任意连接输出或电源电路的击穿电压。AD5422 的电流和电压输出可耐受+48 V 至最低−28 V。AV_{SS} 输入可耐受−28 V，AV_{DD} 可耐受+48 V。ADR02 基准电压源输入可耐受 36 V。AD5700-1 的 ADC_IP 引脚受 150 kΩ 电阻保护，该电阻限制所有电流，后接一个 300 pF 隔直电容。在直流过压条件下，勿将其他 IC 暴露在较高的电压下。

Transient Voltage Protection
瞬变电压保护

The AD5422 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5422 from excessively high voltage transients, external power diodes and a surge current limiting resistor may be required, as is shown in Figure 1.
AD5422 内置 ESD 保护二极管，可防止正常操作造成的损害。但是，工业控制环境会使 I/O 电路遭受高得多的瞬变。为了防止过高瞬态电压影响 AD5422，可能需要外部功率二极管和浪涌电流限制电阻，如图 1 所示。

The constraint on the resistor value in the current output path, shown in Figure 1 as 18 Ω, is that during normal operation, the output level at I_{OUT} must remain within its voltage compliance limit of AV_{DD} − 2.5 V, and the two protection diodes and resistor must have the appropriate power ratings. With 18 Ω, for a 4 mA to 20 mA output, the compliance limit at

the terminal is decreased by V = I_{MAX} × R = 0.36 V.

对电流输出路径上电阻值的制约条件（图 1 中的 18 Ω）是：正常工作时，I_{OUT} 输出电平必须保持在其顺从电压限值内，即 AV_{DD} − 2.5 V，并且两个保护二极管和电阻必须具有适当的额定功率。在 18 Ω 下，对于 4 mA 至 20 mA 输出，引脚上的电压限值会降低 V = I_{MAX} × R = 0.36 V。

The constraint on the resistor value in the voltage output path, shown in Figure 1 as 100 Ω, is that there must be 0.8 V headroom over the output voltage. The effect of this resistor can be minimized by using the +V_{SENSE} input. Shown in Figure 1, the +V_{SENSE} input is protected by a 22 Ω resistor. There is also a corresponding 22 Ω resistor on the −V_{SENSE} path. These two 22 Ω resistors cause some absolute gain error that may need to be calibrated out at room temperature; the reason for this error is that there is only about 70 kΩ impedance in the internal feedback circuitry of the AD5422. The advantage of sensing the voltage at the output and not at the V_{OUT} pin of the AD5422 is that the protection resistor for the V_{OUT} pin has a varying voltage across it, depending on the load current drawn. Sensing at the terminal avoids this error source.

对电压输出路径上电阻值的制约条件（图 1 中的 100 Ω）是：整个输出电压范围内必须具有 0.8 V 裕量。电阻效应可通过+V_{SENSE} 输入降至最低。如图 1 所示，+V_{SENSE} 输入受 22 Ω 电阻保护。相应地，−V_{SENSE} 路径上还有一个 22 Ω 电阻。这两个 22 Ω 电阻会导致绝对增益误差，该误差可能需要在室温下加以校准；产生该误差的原因是 AD5422 的内部反馈电路阻抗仅为 70 kΩ。在 AD5422 的输出端（而非 V_{OUT} 引脚）检测电压的优势是，V_{OUT} 引脚的保护电阻两端具有可变电压，具体取决于所获取的负载电流。在输出端检测可避开此误差源。

Further protection is provided with transient voltage suppressors (TVS) or transorbs. These are available as both unidirectional and bidirectional suppressors and in a wide range of standoff and breakdown voltage ratings. Size the TVS with the lowest breakdown voltage possible while not conducting in the functional range of the current output. As previously discussed, it is recommended that all remotely connected nodes be protected.

还可以通过瞬态电压抑制器(TVS)或瞬态吸收器实现进一步的保护。这些元件包括单向和双向抑制器，可提供各种各样的隔离和击穿电压额定值。TVS 应尽量采用最低击穿电压定标，同时在电流正常输出的范围内不导通。如前所述，建议保护所有远程连接节点。

COMMON VARIATIONS

常见变化

This circuit is proven to work well with good stability and accuracy with the component values shown. When the application needs the 4 mA to 20 mA current output only, a single-supply scheme can be used. In this case, the positive AVDD supply for the AD5422 can be 24 V, for example, and the output compliance is 24 V − 2.5 V = 21.5 V. With an output current of 20 mA, a load resistance as high as 1 kΩ is possible.

经验证，采用图中所示的元件值，该电路能够稳定地工作，并具有良好的精度。如果应用只需要 4 mA 至 20 mA 电流输出，则可以使用单电源方案。这种情况下，AD5422 的正 AVDD 电源可以达到比如 24 V，而输出顺从电压为 24 V − 2.5 V = 21.5 V。输出电流为 20 mA 时，可以驱动高达 1 kΩ 的负载电阻。

For applications not requiring 16-bit resolution, the 12-bit AD5412 is available. For applications that require only current outputs, the AD5420 (16-bit) and AD5410 (12-bit) are available.

如果应用不需要 16 位分辨率，可以使用 12 位产品 AD5412。对于仅需电流输出的应用，可以使用 AD5420（16 位）和 AD5410（12 位）。

For applications that require voltage and current outputs on the same terminal, see Circuit Note CN-0278 for a technique.

对于需要在同一个引脚输出电压和电流的应用，参见电路笔记 CN-0278 中的技巧。

If overvoltage protection is not required, a reference with a lower maximum supply voltage can be used such as the ADR4550 or the ADR445.

若不需要过压保护，则可以采用数值较低的最大电源电压，如 ADR4550 或 ADR445。

The ADuM347x isolators (ADUM3470, ADuM3471, ADuM3472, ADuM3473, and ADuM3474) provide four independent isolation channels in a variety of input/output channel configurations. These devices are also available with either a maximum data rate of 1 Mbps (A grade) or 25 Mbps (C grade).

ADuM347x 隔离器（ADUM3470、ADuM3471、ADuM3472、ADuM3473 和 ADuM3474）提供四个独立的隔离通道，支持多种输入/输出通道配置。这些器件还提供 1 Mbps（A 级）或 25 Mbps（C 级）的最大数据速率。

The AD5700 modem can be used instead of the AD5700-1; however, either an external crystal or a CMOS clock is required.

可使用 AD5700 调制解调器，而非 AD5700-1；但需要使用外部晶体或 CMOS 时钟。

CIRCUIT EVALUATION AND TEST

电路评估与测试

Equipment Required

设备要求

The following equipment is required:

需要使用以下设备：

- The EVAL-SDP-CB1Z system demonstration platform (SDP-B)
  EVAL-SDP-CB1Z 系统演示平台(SDP-B)
- The EVAL-CN0321-SDPZ evaluation board and software
  EVAL-CN0321-SDPZ 评估板和软件
- A PC (Windows® 32-bit or 64-bit)
  PC（Windows® 32 位或 64 位）
- A 24 V power supply
  24 V 电源
- A precision voltmeter, such as Agilent 34410A
  精密电压表，如 Agilent 34410A
- A digital test filter (such as the HCF_TOOL-31 available from the HART Communication Foundation)
  数字测试滤波器（如 HCF_TOOL-31，可从 HART 通信基金会获得）
- A 500 Ω precision load resistor
  500 Ω 精密负载电阻

- An oscilloscope, Tektronix DS1012B or equivalent
  Tektronix DS1012B 示波器或等同产品

Figure 2. Test Setup Functional Diagram

图 2. 测试设置功能框图

Enlarge
放大

Test Setup Functional Diagram

测试设置功能框图

A diagram of the test setup is shown in Figure 2.

测试设置的框图如图 2 所示。

Software Installation

软件安装

The evaluation kit includes self-installing software on a CD. The software is compatible with Windows XP (SP2), Vista (32-bit and 64-bit) or Windows 7 (32-bit and 64-bit). If the setup file does not run automatically, run the **setup.exe** file from the CD.

评估套件包括一张光盘，其中含有自安装软件。该软件兼容 Windows XP (SP2)、Vista（32 位或 64 位），或 Windows 7（32 位或 64 位）。如果安装文件未自动运行，可以运行光盘中的 **setup.exe** 文件。

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

请先安装评估软件，再将评估板和 SDP 板连接到 PC 的 USB 端口，确保 PC 能够正确识别评估系统。

1. Connect the EVAL-SDP-CB1Z via the USB port of the PC using the supplied cable.
   使用附带的电缆，通过 PC 的 USB 端口连接 EVAL-SDP-CB1Z。
2. Connect the EVAL-CN0321-SDPZ evaluation board to Connector A. If Connector B is used, the UART of the EVAL-SDP-CB1Z will not function as required.
   连接 EVAL-CN0321-SDPZ 评估板至连接器 A。若使用了连接器 B，则 EVAL-SDP-CB1Z 的 UART 将无法正常工作。
3. Power up the EVAL-CN0321-SDPZ by applying 24 V to the J1 connector.
   对 J1 连接器施加 24 V，可上电 EVAL-CN0321-SDPZ。
4. Start the EVAL-CN0321-SDPZ software and proceed through any dialog boxes that appear. This completes the installation.
   启动 EVAL-CN0321-SDPZ 软件，然后确认出现的所有对话框。这样就完成了安装。

Software

软件

The main software window is shown in Figure 3. Click **Advanced** for more options for configuring the AD5422.

软件主窗口如图 3 所示。点击 **Advanced** 可提供配置 AD5422 的更多选项。

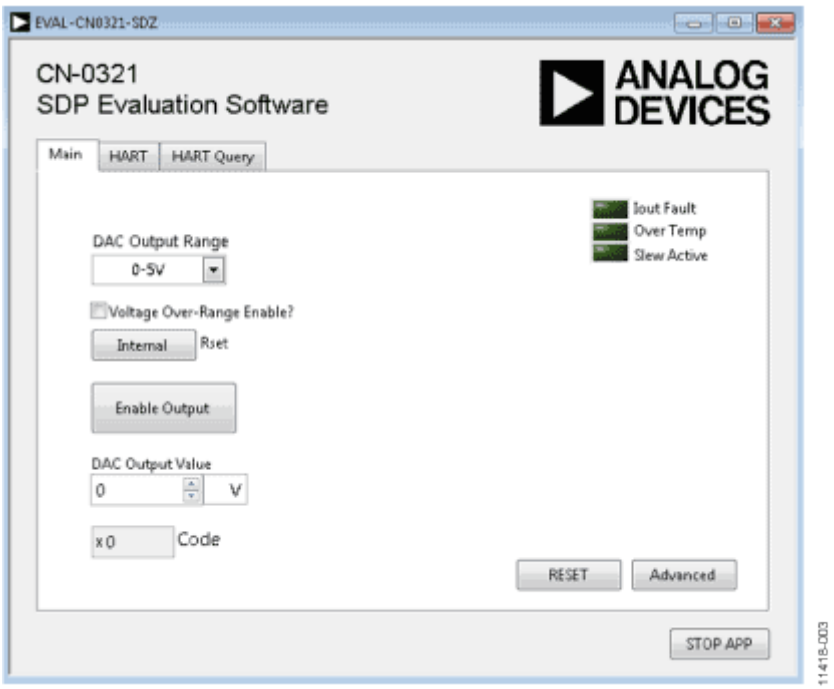

Figure 3. Main Software Window 图 3. 软件主窗口

Enlarge

放大

For **HART** communications, ensure a current output range is enabled and then select the **HART** tab. From the HART tab, data can be entered into the **Command** box and sent over the 4 mA to 20 mA loop, and the software can be set to poll for any data on the 4 mA to 20 mA loop. Alternately, by selecting the **HART Query** tab, a connected HART-compatible actuator can be queried for its device address and device type.

对于 **HART** 通信而言，确保开启了电流输出范围，然后选择 **HART** 页面。在 HART 页面上，数据可输入 **Command** 命令框，然后发送 4 mA 至 20 mA 环路；软件可以设为轮询 4 mA 至 20 mA 环路上的任意数据。也可选择 **HART Query** 页面，查询所连接 HART 兼容型执行器的器件地址和器件类型。

Absolute Accuracy Performance

绝对精度性能

The specification for the total unadjusted error (TUE) for the AD5422 in current output mode using the internal RSET is 0.08% FSR typical at 25°C.

在电流输出模式下，AD5422 使用内部 RSET 的总不可调整误差(TUE)规格为 0.08%（FSR 典型值，25°C）。

The total error of the ADR02 reference (B grade) is 0.06% maximum at 25°C.

ADR02 基准电压源（B 级）的总误差为 0.06%（最大值，25°C）。

Table 2. Measured Current Output Error (4 mA to 20 mA Range)

Code (Hex)	Current at Output (mA)	Error (%FSR)
0000	3.992	−0.049
4000	7.995	−0.034
8000	11.997	−0.018
B000	16.000	+0.001
FFFF	20.003	+0.020

The results are well within the expected values.

结果位于预期值范围内。

Similarly, for voltage output mode, the AD5422 TUE is 0.01% FSR typical at 25°C.

类似地，对于电压输出模式，AD5422 的 TUE 为 0.01%（FSR 典型值，25°C）。

The ADR02 reference error (B grade) is 0.06% maximum at 25°C.

ADR02 基准电压源（B 级）的误差为 0.06%（最大值，25°C）。

Table 3 shows the measured voltage output error for the circuit in the ±10 V output range.

表 3 显示±10 V 输出范围内，电路的测量电压输出误差。

Table 3. Measured Voltage Output Error (±10 V Range)

Code (Hex)	Voltage at Output (V)	Error (%FSR)
0000	−10.010	−0.050
4000	−5.005	−0.023
8000	+0.001	+0.003
B000	+5.006	+0.031
FFFF	+10.011	+0.057

The voltage output shown in Table 3 also includes the error in the circuit for the 22 Ω protection resistors on the $+V_{SENSE}$ and $-V_{SENSE}$ inputs of the AD5422. The $+V_{SENSE}$ and $-V_{SENSE}$ inputs are internally connected to a ~70 kΩ feedback resistor. The additional 22 Ω resistors externally add a gain error of roughly 22 kΩ/70 kΩ, or 0.031%. This initial error can be removed by calibration.

表 3 中的电压输出包括 AD5422 电路$+V_{SENSE}$ 和$-V_{SENSE}$ 输入上的 22 Ω 保护电阻误差。$+V_{SENSE}$ 和$-V_{SENSE}$ 输入内部连接至数值约为 70 kΩ 的反馈电阻。额外的 22 Ω 电阻从外部加入约为 22 kΩ/70 kΩ（或 0.031%）的增益误差。该初始误差可通过校准消除。

Integral Nonlinearity (INL) Performance

积分非线性(INL)性能

The INL of the AD5422 was tested using both linear supplies and the isolated dc-to-dc switching supplies to ensure no loss in system accuracy was incurred because of the switching supplies. Figure 4 shows the INL for both the linear supplies and the switching supplies. There is no noticeable performance loss when using the switching supplies as compared to the linear supplies.

AD5422 的 INL 在线性电源和隔离式 DC/DC 开关电源两种情况下进行测试，确保系统精度不会因为开关电源而有所损失。图 4 显示的是线性电源以及开关电源下的 INL。与线性电源相比，使用开关电源时性能没

有明显损失。

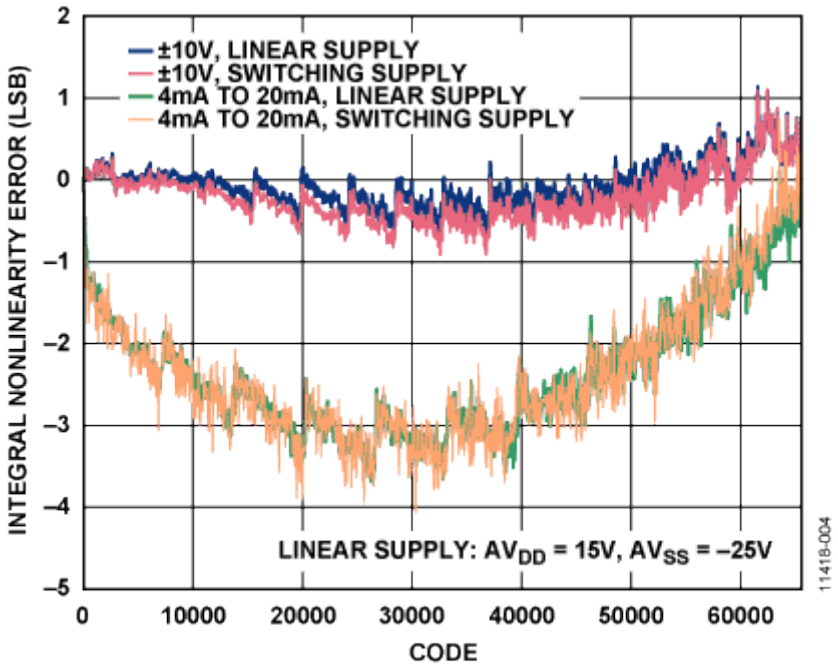

Figure 4. Measured INL of Circuit with Linear and Switching Supply

图 4. 使用线性电源和开关电源的电路实测 INL

Enlarge

放大

The average output noise was also tested and compared over time when using a linear supply and switching supply, as shown in Figure 5. Note that there is a slight offset in output noise measured over time. This offset is not much larger than 1 LSB and could be introduced by a slightly different measurement setup or the drift in the reference during the time between the two measurements.

此外还测试并比较了线性电源和开关电源两种情况下一定时间内的平均输出噪声，如图 5 所示。注意，一定时间内测得的输出噪声存在细微的偏差。这一偏差不超过 1 LSB，可能由略为不同的测量设置引入，或两次测量间隔期间的基准电压漂移引入。

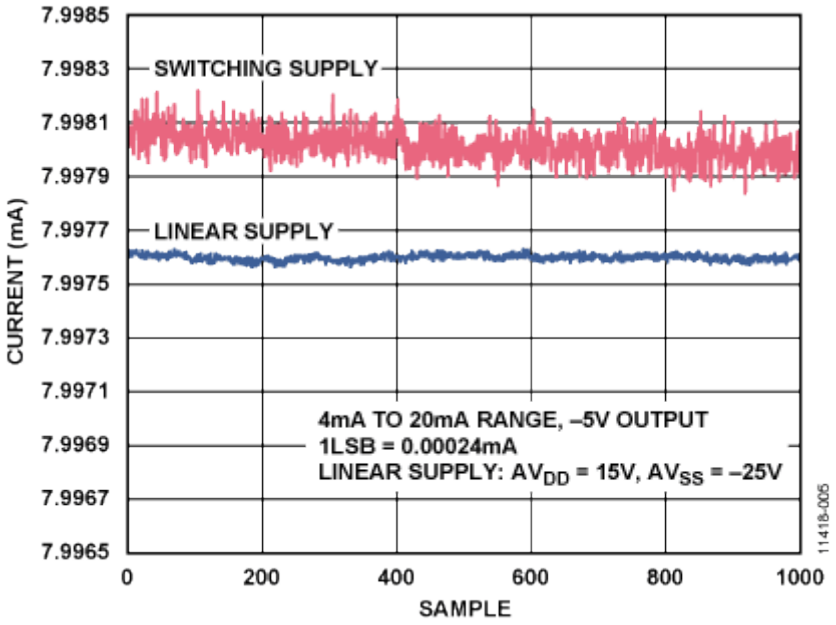

Figure 5. Measured Average DAC Output Noise, 1000 Sample, Meter Set to NPLC = 1

图 5. 实测平均 DAC 输出噪声，1000 次采样，电表设为 NPLC = 1

Enlarge

放大

HART Compliance

HART 兼容性

For the circuit in Figure 1 to be HART-compliant, it must meet the HART physical layer specifications. There are a number of physical layer specifications included in the HART specification documents. For evaluating the performance of the hardware, the output noise during silence and the analog rate of change test were used.

图 1 中的电路要与 HART 兼容，必须符合 HART 物理层规范。HART 规范文档中包含了众多物理层规范。为了评估硬件性能，采用静默期间的输出噪声和模拟变化率测试。

Output Noise During Silence Test

静默期间的输出噪声测试

When a HART device is not transmitting (silence), it should not couple noise onto the network. Excessive noise may interfere with the reception of HART signals by the device itself or other devices on the network.

当 HART 设备没有进行传输（静默）时，噪声不应耦合至网络上。噪声过高可能会干扰设备本身或网络上的其它设备对 HART 信号的接收。

The voltage noise measured across a 500 Ω load in the loop must contain no more than 2.2 mV rms of combined broadband and correlated noise in the HART extended frequency band. In addition, the noise must not exceed 138 mV rms outside the HART extended frequency band.

对于在环路中的 500 Ω 负载上测得的电压噪声，其包含的宽带噪声和 HART 扩展频带中的相关噪声总和不能超过 2.2 mV rms。此外，HART 扩展频带外的噪声不应超过 138 mV rms。

This noise was measured by a true rms meter connected across the 500 Ω load. This noise was measured directly for the out-of-band noise and measured through the HCF_TOOL-31 filter for the in-band noise. An oscilloscope was also used to examine the noise waveform.

500 Ω 负载上的噪声采用真均方根测量仪测得。此噪声作为带外噪声直接进行测量，作为带内噪声通过 HCF_TOOL-31 滤波器测量。也可使用示波器来检查噪声波形。

The captured noise waveform is shown in Figure 6, and the results are summarized in Table 4.

图 6 显示捕获的噪声波形，结果总结在表 4 中。

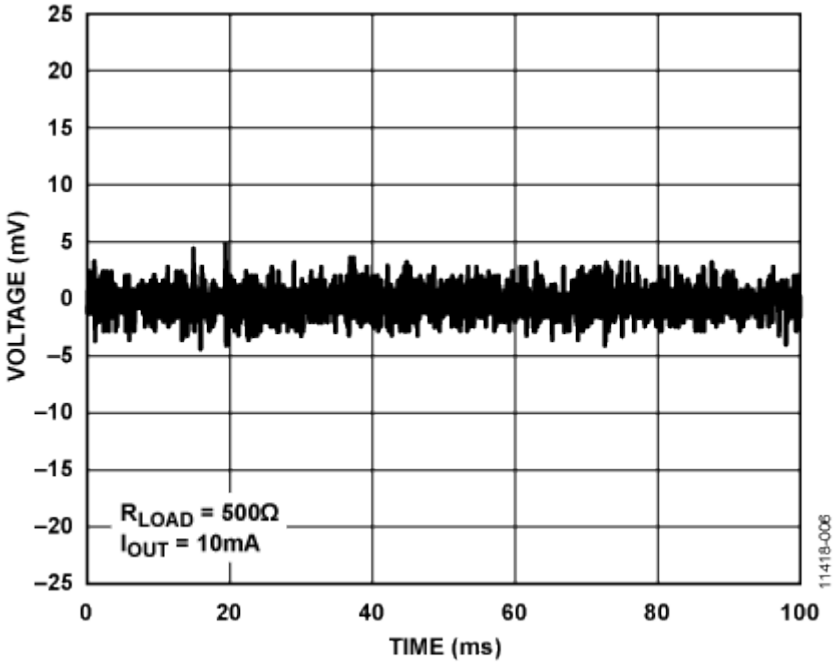

Figure 6. Output Noise During Silence Waveform

图 6. 静默波形下的输出噪声

Enlarge

放大

Table 4. Output Noise During Silence

Output Noise	Measured (mV)	
Outside Extended Frequency Range	0.6	<138
Inside Extended Frequency Range	0.126	<2.2

Analog Rate of Change

模拟变化率

The analog rate of change test ensures that when a device regulates the analog output current, the maximum rate of change of the analog current does not interfere with HART communications. Step changes in current disrupt HART signaling.

模拟变化率测试可确保器件调节模拟输出电流时，模拟电流的最大变化率不会干扰 HART 通信。电流的阶跃变化会扰乱 HART 信号传输。

The worst-case change in the analog output current must not produce a disturbance higher than 15 mV peak, measured across a 500 Ω load in the HART extended frequency band.

最差情况下的模拟输出电流变化一定不能产生高于 15 mV 峰值电压的干扰，此数值在 HART 扩展频带下，通过对 500 Ω 负载进行测量得到。

The AD5422 DAC and output driver are relatively fast. Therefore, to meet the required system specifications, the output current change is limited by the hardware slew rate limit using capacitors on the CAP1 and CAP2 pins of the AD5422 and the digital slew rate control feature of the AD5422 . This is outlined in more detail in the AN-1065 Application Note.

AD5422 AC 和输出驱动器相对较快。因此，为了满足所需的系统规格，输出电流变化受限于使用 AD5422 CAP1 和 CAP2 引脚电容时的硬件压摆率限值，以及 AD5422 的数字压摆率控制特性。详见 AN-1065 应用笔记。

This test was performed using an oscilloscope coupled to a 500 Ω load through the HCF_TOOL-31 filter.

使用一个示波器执行该测试，并通过 HCF_TOOL-31 滤波器耦合至 500 Ω 负载。

The result is shown in Figure 7. The 4 mA and 20 mA output line (see blue line in Figure 7) shows the periodic steps between 4 mA and 20 mA, sensed directly across a 500 Ω load. The output of the filter × 10 line (see red line in Figure 7) is the signal captured on the HCF_TOOL-31 filter output, amplified 10×, within the 150 mV peak limits.

结果如图 7 所示。4 mA 至 20 mA 输出线路（见图 7 中的蓝线）显示 4 mA 和 20 mA 之间的周期性步进，直接在 500 Ω 负载上测得。滤波器放大 10 倍的输出（见图 7 中的红线）是 HCF_TOOL-31 滤波器输出端捕获的信号，将其放大 10 倍，并处于 150 mV 峰值限制之内。

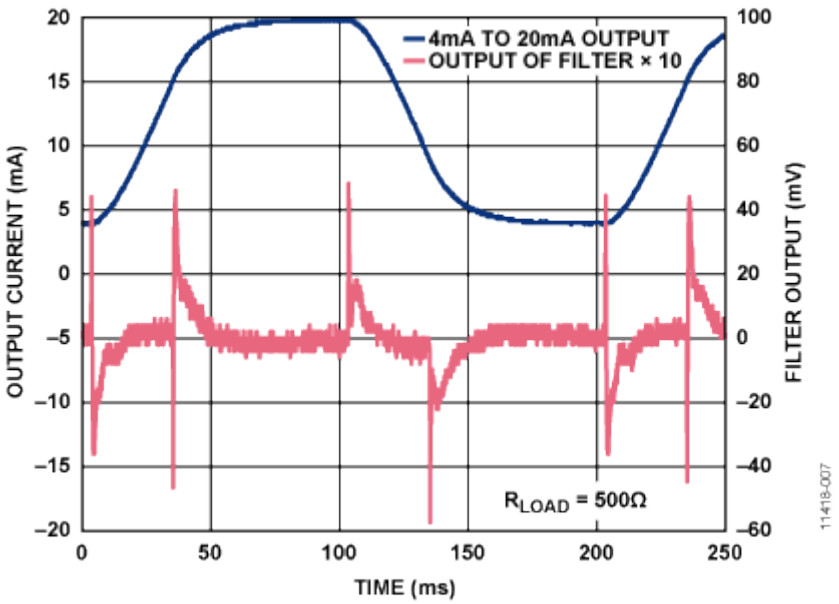

Figure 7. Analog Rate of Change Waveform

图 7. 模拟变化率波形

Enlarge

放大