http://www.analog.com/zh/circuits-from-the-lab/CN0311/vc.html

Broadband, Low Error Vector Magnitude (EVM) Direct Conversion Transmitter Using LO Divide-by-2 Modulator (CN0311)

使用 LO 二分频调制器的宽带低误差矢量幅度(EVM)直接变频发射机(CN0311)

Devices Connected/Referenced

连接/参考器件

ADF4351 Fractional-N PLL IC with Integrated VCO

ADF4351 集成 VCO 的小数 N 分频 PLL IC

ADL5385 Wideband Transmit Modulator

ADL5385：宽带发射调制器

ADP150 Low Noise 3.3 V LDO

ADP150：低噪声 3.3 V LDO

ADP3334 Low Noise Adjustable LDO

ADP3334：低噪声可调 LDO

EVALUATION AND DESIGN SUPPORT

评估和设计支持

Circuit Evaluation Boards

电路评估板

ADF4351 Evaluation Board (EVAL-ADF4351EB1Z)

ADF4351评估板(EVAL-ADF4351EB1Z)

ADL5385 Evaluation Board (ADL5385-EVALZ)

ADL5385评估板(ADL5385-EVALZ)

Design and Integration Files

设计和集成文件

Schematics, Layout Files, Bill of Materials

原理图、布局文件、物料清单

CIRCUIT FUNCTION AND BENEFITS

电路功能与优势

This circuit is a complete implementation of the analog portion of a broadband direct conversion transmitter (analog baseband in, RF out). RF frequencies from 30 MHz to 2.2 GHz are supported by using a phase-locked loop (PLL) with a broadband integrated voltage controlled oscillator (VCO). Unlike

modulators that use a divide-by-1 local oscillator (LO) stage (as described in CN-0285), harmonic filtering of the LO is not required.

本电路为宽带直接变频发射机模拟部分的完整实施方案（模拟基带输入、RF 输出）。通过使用锁相环(PLL)和宽带集成电压控制振荡器(VCO)，本电路支持 30 MHz 至 2.2 GHz 范围内的 RF 频率。与使用一分频本地振荡器(LO)级的调制器不同（如 CN-0285 中所述），本电路无需进行 LO 的谐波滤波。

To achieve optimum performance, the only requirement is that the LO inputs of the modulator be driven differentially. The ADF4351 provides differential RF outputs and is, therefore, an excellent match. This PLL-to-modulator interface is applicable to all I/Q modulators and I/Q demodulators that contain a 2XLO-based phase splitter. Low noise LDOs ensure that the power management scheme has no adverse impact on phase noise and error vector magnitude (EVM). This combination of components represents an industry-leading direct conversion transmitter performance over a frequency range of 30 MHz to 2.2 GHz. For frequencies above 2.2 GHz, it is recommended to use a divide-by-1 modulator, as described in CN-0285.

获得最佳性能的唯一要求，就是以差分方式驱动调制器的 LO 输入。ADF4351 可提供差分 RF 输出，因此极其适用于本电路。PLL 转调制器接口适用于所有集成 2XLO 分相器的 I/Q 调制器和 I/Q 解调器。低噪声 LDO 确保电源管理方案对相位噪声和误差矢量幅度(EVM)没有不利影响。这种器件组合可以提供 30 MHz 至 2.2 GHz 频率范围内业界先进的直接变频发射机性能。对于 2.2 GHz 以上的频率，则推荐使用一分频调制器，如 CN-0285 所述。

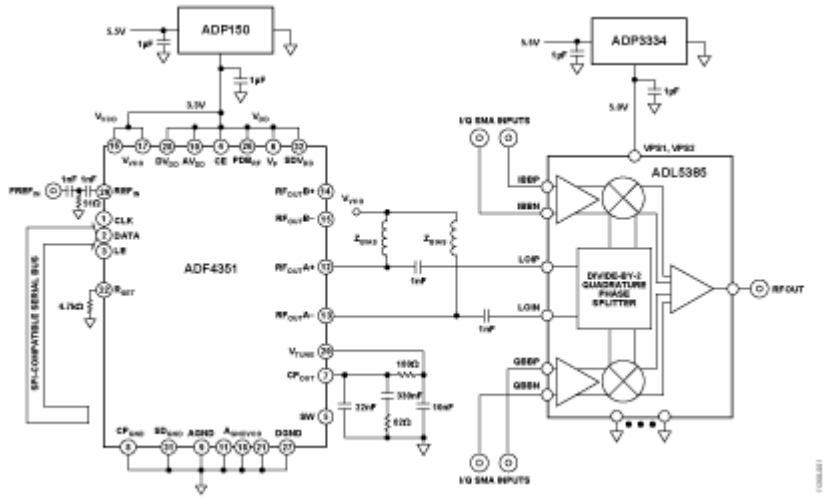

Figure 1. Direct Conversion Transmitter (Simplified Schematic: All Connections and Decoupling Not Shown)

图 1. 直接变频发射机（原理示意图：未显示所有连接和去耦）

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CIRCUIT DESCRIPTION

电路描述

The circuit shown in Figure 1 uses the ADF4351, a fully integrated fractional-N PLL IC, and the ADL5385 wideband transmit modulator. The ADF4351 provides the local oscillator (the LO is twice the modulator RF output frequency) signal for the ADL5385 transmit quadrature modulator, which upconverts the analog I/Q signals to RF. Taken together, the two devices provide a wideband, baseband I/Q-to-RF transmit solution.

图 1 所示电路使用完全集成的小数 N 分频 PLL IC ADF4351 和宽带发射调制器 ADL5385。ADF4351 向发射正交调制器 ADL5385 提供本振（LO 频率为调制器 RF 输出频率的两倍）信号，后者将模拟 I/Q 信号上变频为 RF 信号。两个器件共同提供宽带基带 I/Q 至 RF 发射解决方案。

The ADF4351 is powered off the ultralow noise 3.3 V ADP150 regulator for optimal LO phase noise performance. The ADL5385 is powered off a 5 V ADP3334 LDO. The ADP150 LDO has an output voltage noise of only 9 μV rms, integrated from 10 Hz to 100 kHz, and helps to optimize VCO phase noise and reduce the impact of VCO pushing (equivalent to power supply rejection). See CN-0147 for more details on powering the ADF4351 with the ADP150 LDO.

ADF4351 采用超低噪声 3.3 V ADP150 调节器供电，以实现最佳 LO 相位噪声性能。ADL5385 则采用 5 V ADP3334 LDO 供电。ADP150 LDO 的输出电压噪声仅为 9 μV rms（10 Hz 至 100 kHz 积分），有助于优化 VCO 相位噪声并减少 VCO 推压的影响（等效于电源抑制）。有关使用 ADP150 LDO 对 ADF4351 供电的更多详情，请参见 CN-0147。

The ADL5385 uses a divide-by-2 block to generate the quadrature LO signals. The quadrature accuracy is, thus, dependent on the duty cycle accuracy of the incoming LO signal (as well as the matching of the internal divider flip-flops). Any imbalance in the rise and fall times causes even-order harmonics to appear, as evident on the ADF4351 RF outputs. When driving the modulator LO inputs differentially, even-order cancellation of harmonics is achieved, improving the overall quadrature generation. (See "Wideband A/D Converter Front-End Design Considerations: When to Use a Double Transformer Configuration." Rob Reeder and Ramya Ramachandran. Analog Dialogue, 40-07.)

ADL5385 采用二分频模块产生正交 LO 信号。因此，正交精度取决于输入 LO 信号的占空比精度（以及内部分频器触发器的匹配）。上升和下降时间的任何不平衡都会导致偶数阶谐波出现，影响 ADF4351 RF 的输出。当以差分形式驱动调制器 LO 输入时，可以消除偶数阶谐波，改善总体正交产生性能。（详见"宽带 ADC 前端设计考虑：何时使用双变压器配置。"作者：Rob Reeder 和 Ramya Ramachandran，模拟对话，40-07）

Because sideband suppression performance is dependent on the modulator quadrature accuracy, better sideband suppression is achievable when driving the LO input ports differentially vs. single-ended. The ADF4351 has differential RF outputs compared to the single-ended output available on most of the competitor's PLL devices with integrated VCOs.

由于边带抑制性能取决于调制器的正交精度，相比单端方式，以差分方式驱动 LO 输入端口能获得更佳的边带抑制。比起大部分集成 VCO 的竞争型 PLL 器件所采用的单端输出，ADF4351 可提供差分 RF 输出。

The ADF4351 output match consists of the Z_{BIAS} pull-up and, to a lesser extent, the decoupling capacitors on the supply node. To get a broadband match, it is recommended to use either a resistive load (Z_{BIAS} = 50 Ω) or a resistive in parallel with a reactive load for Z_{BIAS}. The latter gives slightly higher output power, depending on the inductor chosen. Use an inductor value of 19 nH or greater for LO operation below 1 GHz. The measured results in this circuit were performed using Z_{BIAS} = 50 Ω and an output power setting of 5 dBm. When using the 50 Ω resistor, this setting gives approximately 0 dBm on each output across the full band, or 3 dBm differentially. The ADL5385 LO input drive level specification is −10 dBm to +5 dBm; therefore, it is possible to reduce the ADF4351 output power to save current.

ADF4351 输出匹配包括 Z_{BIAS} 上拉电阻，电源节点的去耦电容也起到一定的作用。为实现宽带匹配，建议使用阻性负载(Z_{BIAS} = 50 Ω)，或者将一个阻性负载与 Z_{BIAS} 的电抗性负载并联。后者提供的输出功率稍高，具体取决于所选的电感。对于 1 GHz 以下的 LO 工作频率，则使用数值为 19 nH 或更高的电感。利用 Z_{BIAS} = 50 Ω 可得出本电路的测量结果；输出功率设置为 5 dBm。使用 50 Ω 电阻时，此设置在全频段范围内的每输出约为 0 dBm；而使用差分输入时为 3 dBm。ADL5385 LO 的输入驱动电平规格为−10 dBm 至+5 dBm；因此，它能够降低 ADF4351 的输出功率，节省功耗。

A sweep of sideband suppression vs. RF output frequency is shown in Figure 2. In this sweep, the test conditions were as follows:

边带抑制性能与 RF 输出频率的扫描关系图如图 2 所示。在该扫描图中，测试条件如下：

- Baseband I/Q amplitude = 1.4 V p-p differential sine waves in quadrature with a 500 mV dc bias
- 基带 I/Q 幅度 = 1.4 V p-p 差分正弦波与 500 mV 直流偏置正交
- Baseband I/Q frequency (f_{BB}) = 1 MHz
- 基带 I/Q 频率(f_{BB}) = 1 MHz
- LO = 2 × RF_{OUT}
- LO = 2 × RF_{OUT}

A simplified diagram of the test setup is shown in Figure 3. A modified ADL5385 evaluation board was used because the standard ADL5385 board does not allow a differential LO input drive.

测试设置的简化框图如图 3 所示。由于标准 ADL5385 板不支持差分 LO 输入驱动，因此测试中使用了修改后的 ADL5385 评估板。

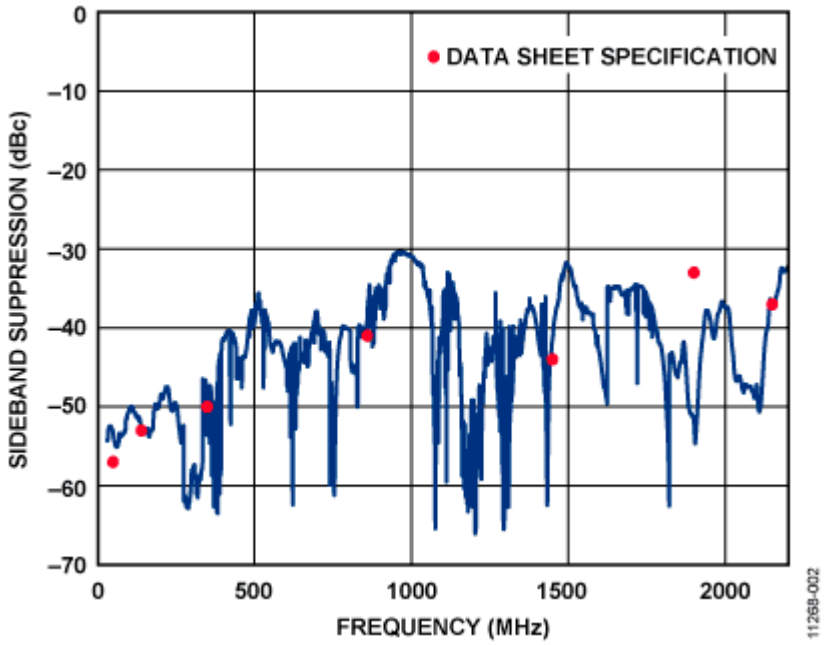

Figure 2. Sideband Suppression, RFOUT Swept from 30 MHz to 2200 MHz

图 2. 边带抑制，RFOUT 从 30 MHz 扫描至 2200 MHz

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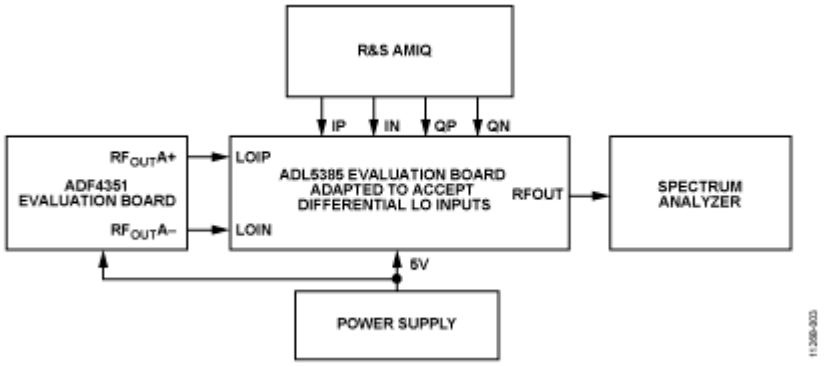

Figure 3. Sideband Suppression Measurement Test Setup (Simplified Diagram)

图 3. 测量边带抑制的测试设置（原理示意图）

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This circuit achieves comparable or improved sideband suppression performance when compared to driving the ADL5385 with a low noise RF signal generator, as used in the data sheet measurement. Using the differential RF outputs of the ADF4351 provides even-order harmonic cancellation and improves modulator quadrature accuracy. This affects sideband suppression performance and EVM. A single carrier W-CDMA composite EVM of better than 2% was measured with the circuit shown in Figure 1. The solution thus provides a low EVM broad-band solution for frequencies from 30 MHz to 2.2 GHz. For frequencies above 2.2 GHz, use a divide-by-1 modulator block, as described in CN-0285.

相比数据手册测量中利用低噪声 RF 信号发生器驱动 ADL5385，本电路获得了类似的（甚至更佳的）边带抑制性能。利用 ADF4351 的差分 RF 输出可消除偶数阶谐波，并提升调制器的正交精度。这会影响边带抑制性能和 EVM。对图 1 所示电路的测量表明，该电路的单载波 W-CDMA 复合 EVM 优于 2%。因此，该电路为 30 MHz 至 2.2 GHz 的频率提供了低 EVM 宽带解决方案。对于 2.2 GHz 以上的频率，可使用一分频调制器模块，如 CN-0285 所述。

The complete design support package can be found at http://www.analog.com/CN0311-DesignSupport.

若需完整的设计支持包，请参阅 http://www.analog.com/CN0311-DesignSupport。

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COMMON VARIATIONS
常见变化

The PLL-to-modulator interface described is applicable to all I/Q modulators that contain a 2XLO-based phase splitter. It is also applicable to 2XLO-based I/Q demodulators, such as the ADL5387.

本文所述 PLL 转调制器接口适用于所有集成 2XLO 分相器的 I/Q 调制器。它还适用于基于 2XLO 的 I/Q 解调器，如 ADL5387。

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CIRCUIT EVALUATION AND TEST
电路评估与测试

The CN-0311 uses the EVAL-ADF4351EB1Z and the ADL5385-EVALZ for the evaluation of the described circuit, allowing for quick setup and evaluation. The EVAL-ADF4351EB1Z uses the standard ADF4351 programming software contained on the CD that accompanies the evaluation board.

CN-0311 使用 EVAL-ADF4351EB1Z 和 ADL5385-EVALZ 评估所述电路，能够快速设置并进行评估。EVAL-ADF4351EB1Z 使用评估板附带光盘中的标准 ADF4351 编程软件。

Equipment Needed
设备要求

The following equipment is needed:
需要以下设备：

- A PC with a USB port that contains Windows® XP, Vista, or Windows 7
- 带 USB 端口的 Windows® XP、Vista 或 Windows 7 PC
- The EVAL-ADF4351EB1Z evaluation board
- EVAL-ADF4351EB1Z 评估板
- The ADL5385-EVALZ evaluation board,
- ADL5385-EVALZ 评估板，
- ADF4351 programming software
- ADF4351 编程软件
- Power supplies (5 V, 500 mA)
- 电源 (5 V, 500 mA)
- An I-Q signal source, such as a Rohde & Schwarz AMIQ
- I/Q 信号源，如 Rohde & Schwarz AMIQ
- A spectrum analyzer
- 频谱分析仪

Also, see the UG-435 User Guide for the EVAL-ADF4351EB1Z evaluation board, the ADF4351 data sheet, and the ADL5385 data sheet.

另外，可参考针对 EVAL-ADF4351EB1Z 评估板的 UG-435 用户指南、ADF4351 数据手册和 ADL5385 数据手册。

Getting Started

开始使用

A description of the circuit, the schematic, and a block diagram of the test setup is detailed within the CN-0311 (see Figure 1 and Figure 3). The UG-435 user guide details the installation and use of the EVAL-ADF4351EB1Z evaluation software. The UG-435 also contains the board setup instructions, and the board schematic, layout, and bill of materials. The ADL5385-EVALZ board schematic, block diagram, bill of materials, layout, and assembly information is included in the ADL5385 data sheet. See the ADF4351 data sheet and ADL5385 data sheet for device information.

测试设置的电路描述、原理图和框图详细信息参见 CN-0311（见图 1 和图 3）。UG-435 用户指南详细说明了 EVAL-ADF4351EB1Z 评估软件的安装和使用。UG-435 还包含电路板设置说明和电路板原理图、布局和物料清单。ADL5385 数据手册中含有 ADL5385-EVALZ 电路板原理图、框图、物料清单、布局和组装信息。相关器件信息，请参考 ADF4351 数据手册和 ADL5385 数据手册。

Functional Block Diagram

功能框图

The functional block diagram of the described test setup is shown in Figure 3.

本文所述测试设置的功能框图见图 3。

Setup and Test

设置和测试

After setting up the equipment, use standard RF test methods to measure the sideband suppression of the circuit.

完成设备设置后，使用标准 RF 测试方法测量电路的边带抑制性能。

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