http://www.analog.com/zh/circuits-from-the-lab/CN0278/vc.html

Complete 4 mA to 20 mA HART Solution with Additional Voltage Output Capability (CN0278)

具有额外电压输出能力的完整 4 mA 至 20 mA HART 解决方案(CN0278)

Devices Connected/Referenced

连接/参考器件

AD5700, AD5700-1 Low Power HART Modem

AD5700、AD5700-1 低功耗 HART 调制解调器

AD5422 16-Bit Current and Voltage Output DAC

AD5422 16 位电流和电压输出 DAC

EVALUATION AND DESIGN SUPPORT

评估和设计支持

Circuit Evaluation Boards

电路评估板

AD5422 Circuit Evaluation Board (EVAL-AD5422EBZ, LFCSP version)

AD5422 电路评估板（EVAL-AD5422EBZ，LFCSP 版本）

AD5700-1/AD5700 Evaluation Board (EVAL-AD5700-1EBZ)

AD5700-1/AD5700 评估板(EVAL-AD5700-1EBZ)

Design and Integration Files

设计和集成文件

Schematics, Layout Files, Bill of Materials

原理图、布局文件、物料清单

CIRCUIT FUNCTION AND BENEFITS

电路功能与优势

The circuit shown in Figure 1 uses the AD5700, the industry's lowest power and smallest footprint HART®1-compliant IC modem, and the AD5422, a 16-bit current output and voltage output DAC, to form a complete HART-compatible 4 mA to 20 mA solution. The use of the OP184 in the circuit allows the I_{OUT} and V_{OUT} pins to be shorted together, thus reducing the number of screw connections required in programmable logic control (PLC) module applications. For additional space savings, the AD5700-1 offers a 0.5% precision internal oscillator.

图 1 所示电路使用低功耗，小尺寸的 HART®[1] 兼容型 IC 调制解调器 AD5700 和 16 位电流输出和电压输出 DAC AD5422，构成完整的 HART 兼容型 4 mA 至 20 mA 解决方案。该电路中采用 OP184，使得 I_{OUT} 和 V_{OUT} 引脚能够短接在一起，从

而减少可编程逻辑控制(PLC)模块应用中所需的螺丝连接数量。为了进一步节省空间，AD5700-1 提供了精度为 0.5%的内部振荡器。

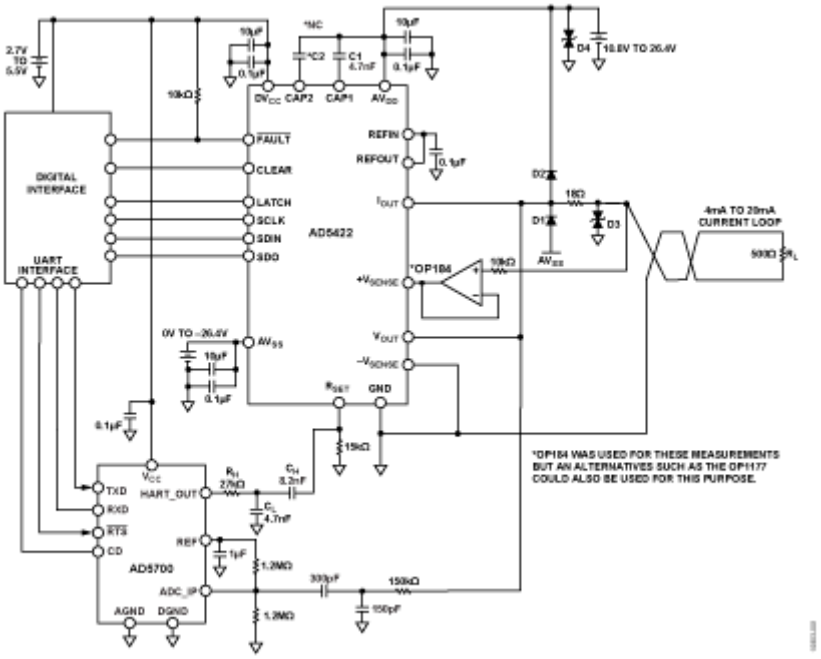

Figure 1. AD5422 HART-Enabled Circuit Simplified Schematic

图 1. AD5422 HART 使能电路原理示意图

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Application Note AN-1065 describes a manner in which the AD5420 I_{OUT} DAC can be configured for HART communication compliance. AN-1065 outlines how the AD5700 HART modem output can be attenuated and ac coupled into the AD5420 via the CAP2 pin. The same is true of the AD5422. However, if the application involves a particularly harsh environment, an alternative circuit configuration can be used which offers better power supply rejection characteristics. This alternative circuit requires the use of the external R_{SET} resistor and involves coupling the HART signal into the R_{SET} pin of the AD5420 or AD5422. The CN-0270 describes this solution for the AD5420, typical of line-powered transmitter applications. The current circuit note is relevant to the AD5422, which, unlike the AD5420, offers both a voltage and a current output pin, and so is particularly useful in PLC/distributed control system (DCS) applications. The AD5422 is available in both 40-lead LFCSP and 24-lead TSSOP packages and the relevance of this, to the circuit characteristics, is examined in the Circuit Description section.

应用笔记 AN-1065 描述了为符合 HART 通信标准而对 AD5420 I_{OUT} DAC 进行配置的方式。AN-1065 概述了 AD5700 HART 调制解调器输出如何进行衰减并通过 CAP2 引脚交流耦合至 AD5420。AD5422 也是如此。然而，如果应用中涉及特别恶劣的环境，则可采用一种电源抑制特性更加的替代电路配置。这种替代电路要求使用外部 R_{SET} 电阻，并涉及到

将 HART 信号耦合至 AD5420 或 AD5422 的 R_{SET} 引脚。CN-0270 描述了 AD5420 的这种解决方案，通常是在线路供电的发射器应用中。目前的电路笔记与 AD5422 相关；与 AD5420 不同，该器件提供电压和电流输出引脚，因此特别适合 PLC/分布式控制系统(DCS)应用。AD5422 提供 40 引脚 LFCS 和 24 引脚 TSSOP 封装，这点与电路特性的相关性将在“电路描述”部分加以介绍。

This circuit adheres to the HART physical layer specifications as defined by the HART Communication Foundation, for example, the output noise during silence and the analog rate of change specifications.

该电路符合由 HART 通信基金会定义的 HART 物理层规范，例如静默期间输出噪声和模拟变化率规格。

For many years, 4 mA to 20 mA communication has been used in process control instrumentation. This communication method is reliable and robust, and offers high immunity to environmental interference over long communication distances. A limitation, however, is that only 1-way communication of one process variable at a time is possible.

多年来，过程控制仪器仪表中一直使用 4 mA 至 20 mA 通信。此通信方式稳定可靠，对长距离通信中的环境干扰具有高抗扰度。不过，其限制是每次只能进行一个过程变量的单向通信。

The development of the highway addressable remote transducer (HART) standard provided highly capable 2-way digital communication, simultaneously with the 4 mA to 20 mA analog signaling used by traditional instrumentation equipment. This allows for features such as remote calibration, fault interrogation, and transmission of additional process variables. Put simply, HART is a digital two-way communication in which a 1 mA peak-to-peak, frequency-shift-keyed (FSK) signal is modulated on top of the 4 mA to 20 mA analog current signal.

可寻址远程传感器高速通道(HART)标准的开发实现了高性能的双向数字通信，同时支持传统仪器仪表设备所使用的 4 mA 至 20 mA 模拟信号。它衍生出各种特性，例如远程校准、故障查询和额外过程变量的传输。简言之，HART 是一种数字双向通信，可在 4 mA 至 20 mA 模拟电流信号之上调制一个 1 mA 峰峰值频移键控(FSK)信号。

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CIRCUIT DESCRIPTION

电路描述

Figure 1 shows the manner in which the AD5422 can be combined with the AD5700 HART modem and a UART interface to construct a HART-capable 4 mA to 20 mA current output, typical of PLC and DCS systems. The buffer connected to the $+V_{SENSE}$ pin is not necessary if the application does not require the I_{OUT} and V_{OUT} pins to be shorted. The HART_OUT signal from the AD5700 is attenuated and ac-coupled into the R_{SET} pin of the AD5422. If the external R_{SET} resistor is not being used, an alternative method of connecting the AD5422 and the AD5700 via the CAP2 pin can be found in Application Note AN-1065, as previously described. This method is only relevant to the 40-lead LFCSP package option of the AD5422 because the lower pin-count 24-lead TSSOP package does not contain a CAP2 pin.

图 1 显示 AD5422 如何与 AD5700 HART 调制解调器和 UART 接口配合使用，以使 PLC 和 DCS 系统常用的 4 mA 至 20 mA 电流输出支持 HART。如果应用无需短接 I_{OUT} 和 V_{OUT} 引脚，则不一定需要连接至 $+V_{SENSE}$ 引脚的缓冲器。来自 AD5700 的 HART_OUT 信号经衰减后，交流耦合至 AD5422 的 R_{SET} 引脚。如果未使用外部 R_{SET} 电阻，通过 CAP2 引

脚连接 AD5422 和 AD5700 的替代方法请参见应用笔记 AN-1065，如前文所述。此方法只适用于 AD5422 的 40 引脚 LFCSP 封装选项，因为引脚数量较少的 24 引脚 TSSOP 封装没有 CAP2 引脚。

While the method described in the current circuit note requires the use of the external R_{SET} resistor, in return, it provides better power supply rejection performance than the alternative application note solution. The use of either solution results in the AD5700 HART modem output modulating the 4 mA to 20 mA analog current (as shown in Figure 2) without affecting the dc level of the current. The diode protection circuitry (D1 to D4) is discussed in more detail in the Transient Voltage Protection section.

虽然本电流电路笔记中描述的方法需要使用外部 R_{SET} 电阻，但其电源抑制性能却高于替代应用笔记解决方案。无论使用哪一种解决方案，AD5700 HART 调制解调器输出均可在不影响电流直流电平的前提下调制 4 mA 至 20 mA 模拟电流（如图 2 所示）。二极管保护电路（D1 至 D4）将在“瞬态电压保护”部分详细论述。

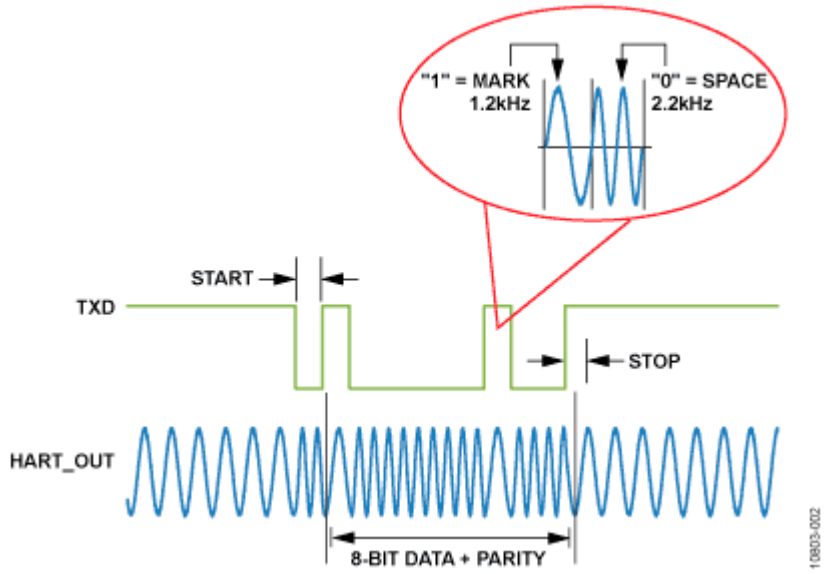

Figure 2. AD5700/ AD5700-1 Sample Modulator Waveform

图 2. AD5700/AD5700-1 样片调制器波形

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Determining the Values of the External Components

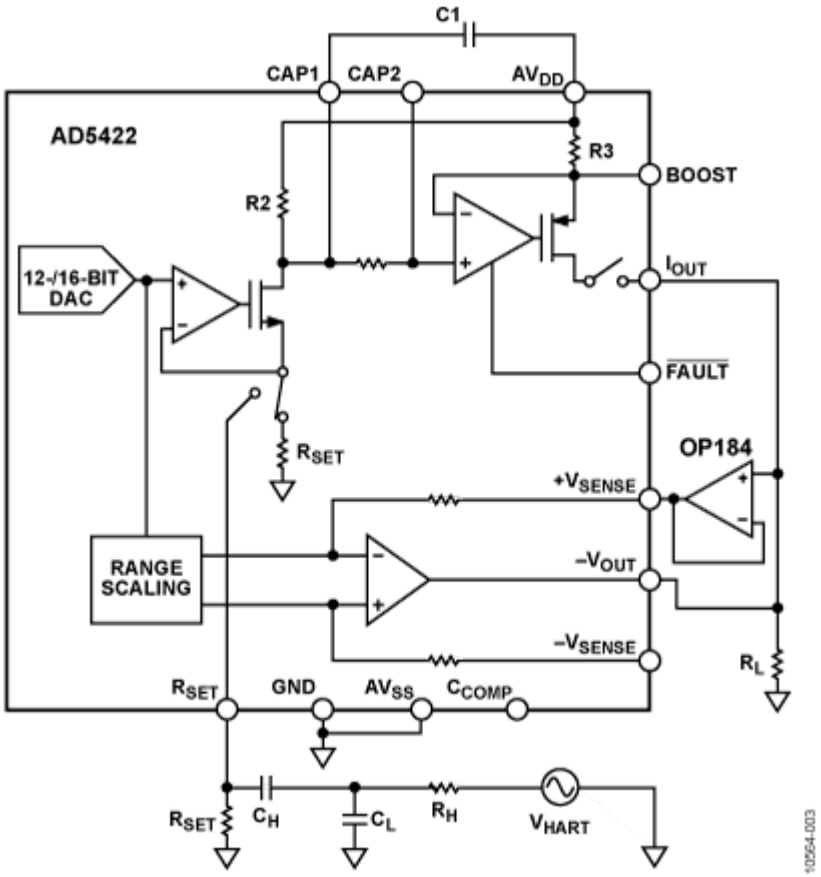
确定外部元件值

Capacitors, C1 and C2, can be used in conjunction with the digital slew rate control functionality of the part to control the slew rate of the IOUT signal of the AD5422. In determining the absolute values of the capacitors, ensure that the FSK output from the modem is passed undistorted. Thus, the bandwidth presented to the modem output signal must pass the 1200 Hz and 2200 Hz frequencies. Figure 3 shows a circuit that achieves this requirement. In this case, C2 (shown in Figure 1) is left open-circuit.

C1 和 C2 电容可配合器件的数字压摆率控制功能使用，以控制 AD5422 的 IOUT 信号压摆率。确定电容的绝对值时，要确保调制解调器的 FSK 输出无失真通过。因此，调制解调器输出信号的带宽必须通过 1200 Hz 和 2200 Hz 频率。图 3 显示了实现此要求的电路。在此情况下，C2（如图 1 所示）保持开路。

Figure 3. AD5422 and AD5700 HART Modem Connection

图 3. AD5422 和 AD5700 HART 调制解调器连接



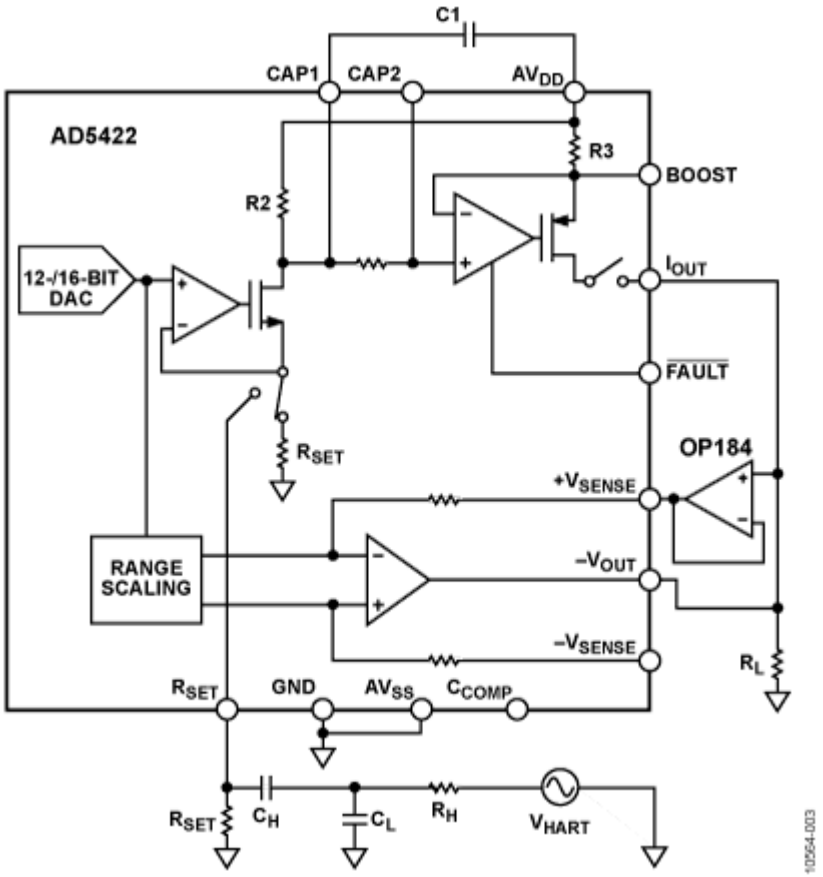


Figure 3. AD5422 and AD5700 HART Modem Connection

图 3. AD5422 和 AD5700 HART 调制解调器连接

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The low-pass and high-pass filter circuitry is formed through the interaction of R_H, C_L, C_H, and C1, along with some internal circuitry in the AD5422. In calculating the values of these components, the low-pass and high-pass frequency cutoff point targets were >10 kHz and <500 Hz, respectively. Figure 4 shows a plot of the simulated frequency response, while Table 1 shows the effect on the frequency response of increasing each component while the remaining component values are kept constant.

低通和高通滤波器电路通过 R_H、C_L、C_H 和 C1 的相互作用并配合 AD5422 的一些内部电路来形成。在计算这些元件的值时，低通和高通频率截止点目标分别为>10 kHz 和<500 Hz。图 4 显示了仿真频率响应的曲线图，表 1 显示了增加各元件而剩余元件值保持恒定对频率响应的影响。

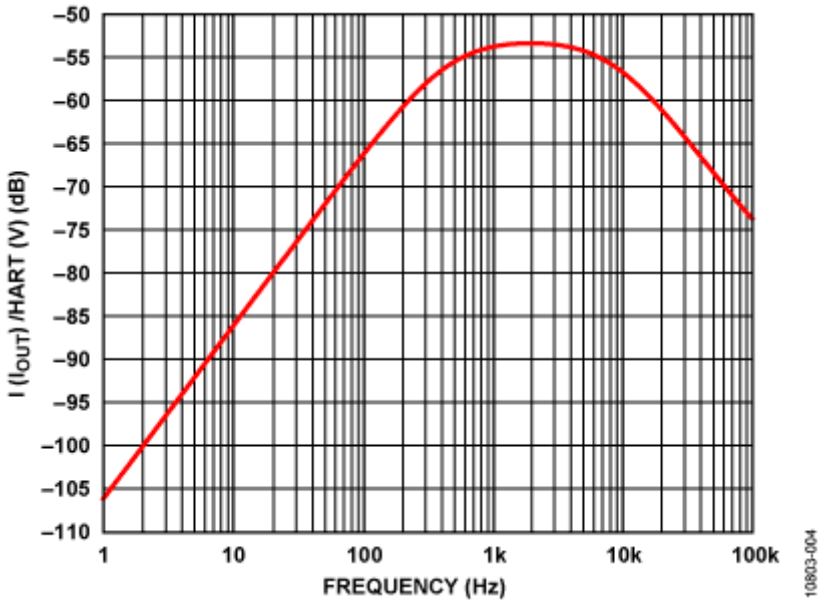

Figure 4. Simulated Frequency Response

图 4. 仿真频率响应

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Table 1. Effect on Frequency Response of Individual Component Value Increase

表 1. 个别元件值增加对频率响应的影响

Component **元件**	**C1**	**C_H**	**C_L**	**R_H**
f_L (Hz)	↓	↓	↓	↓
f_H (kHz)	↓	No change 无变化	No change 无变化	No change 无变化
G (dB)	↓	↑	↓	↓

The output of the modem is an FSK signal consisting of 1200 Hz and 2200 Hz shift frequencies. This signal must translate to a 1 mA p-p current signal. To achieve this, the signal amplitude at the R_{SET} pin must be attenuated. This is due to the internal current gain configuration in the AD5422 design. Assuming that the modem output amplitude is 500 mV p-p, its output must be attenuated by 500/150 = 3.33. This attenuation is achieved by means of R_H and C_L.

调制解调器的输出是一个 FSK 信号，包括 1200 Hz 和 2200 Hz 移频。这个信号必须转换为 1 mA 峰峰值电流信号。为此，R_{SET} 引脚上的信号幅度必须衰减。这是因为 AD5422 采用内部电流增益配置设计。假定调制解调器的输出幅度为 500 mV p-p，则其输出必须经过 500/150 = 3.33 倍衰减。此衰减通过 R_H 和 C_L 来实现。

The measurements in this circuit note were completed using the following component values:

本电路笔记中的测量使用以下元件值完成：

- C1 = 4.7 nF
- C1 = 4.7 nF
- R_H = 27 kΩ
- R_H = 27 kΩ
- C_L = 4.7 nF
- C_L = 4.7 nF
- C_H = 8.2 nF
- C_H = 8.2 nF

Figure 5 shows the individual 1200 Hz and 2200 Hz shift frequencies measured across a 500 Ω load resistor. Channel 1 shows the modulated HART signal coupled into the AD5422 output (set to output 4 mA), while Channel 2 shows the AD5700 TXD signal.

图 5 表明在 500 Ω 负载电阻上分别测得了 1200 Hz 和 2200 Hz 移频。通道 1 显示耦合至 AD5422 输出中的调制 HART 信号（设置为输出 4 mA），通道 2 则显示 AD5700 TXD 信号。

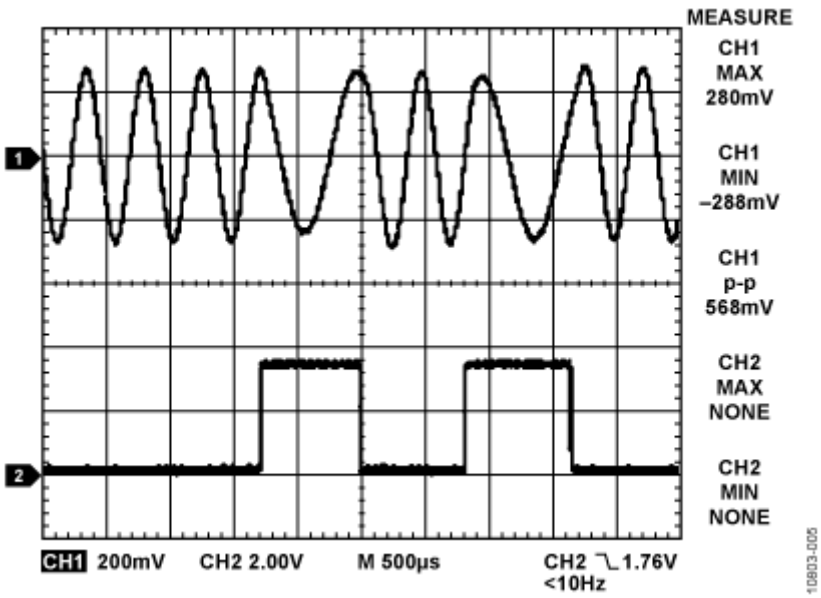

Figure 5. FSK Waveforms Measured Across a 500 Ω Load

图 5. 在 500 Ω 负载上测得的 FSK 波形

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HART Compliance

HART 兼容性

For the circuit in Figure 1 to be HART-compliant, it must meet the HART physical layer specifications. There are numerous physical layer specifications included in the HART specification documents. The two that are most important in this case are the output noise during silence and the analog rate of change.

图 1 中的电路要与 HART 兼容，必须符合 HART 物理层规范。HART 规范文档中包含了众多物理层规范。其中最重要的两个是静默期间输出噪声和模拟变化率。

Output Noise During Silence

静默期间输出噪声

When a HART device is not transmitting (silent), it should not couple noise onto the network in the HART extended frequency band. Excessive noise may interfere with reception of HART signals by the device itself or other devices on the network.

当 HART 设备没有进行传输（静默）时，不应在 HART 扩展频带中将噪声耦合到网络上。噪声过高可能会干扰设备本身或网络上其它设备对 HART 信号的接收。

The voltage noise measured across a 500 Ω load must contain no more than 2.2 mV rms of combined broadband and correlated noise in the extended frequency band. This noise was measured by connecting the HCF_TOOL-31 filter (available from the HART Communication Foundation) across the 500 Ω load and by connecting the output of the filter to a true rms meter (see Figure 6). An oscilloscope was also used to examine the output waveform peak-to-peak voltage.

对于在 500 Ω 负载上测得的电压噪声，其包含的扩展频带中的宽带噪声和相关噪声总和不能超过 2.2 mV rms。此噪声通过在 500 Ω 负载上连接 HCF_TOOL-31 滤波器（可从 HART 通信基金会获得）并将滤波器输出连接到真均方根测量仪（参见图 6）来测量。也可使用示波器来检查输出波形峰峰值电压。

The AD5422 output current was set to 4 mA, 12 mA, and 20 mA. Results with the band-pass filter in place were very similar for all three output current values, while the wide bandwidth noise increased slightly as the current output value increased. The rms values measured, with and without the HCF_TOOL-31 band-pass filter in the case of 4 mA output current, were 143 µV rms and 1.4 mV rms, respectively. Both of these values are well within the required specifications of 2.2 mV rms (with HART filter) and 138 mV rms (broadband noise without HART filter). For 12 mA output current, the rms values measured, with and without the HCF_TOOL-31 band-pass filter were 158 µV rms and 2.1 mV rms, respectively, again, both well within HART protocol specifications.

AD5422 输出电流设置为 4 mA、12 mA 和 20 mA。对于所有这三个输出电流值，有带通滤波器时的结果十分相似，不过电流输出值增加时，宽带宽噪声也略有增加。在输出电流为 4 mA 的情况下，使用和不使用 HCF_TOOL-31 带通滤波器时，测得的均方根值分别为 143 µV rms 和 1.4 µV rms。这两个值均在要求的 2.2 mV rms（使用 HART 滤波器）和 138 mV rms（不使用 HART 滤波器的宽带噪声）规范内。在输出电流为 12 mA 的情况下，使用和不使用 HCF_TOOL-31 带通滤波器时，测得的均方根值分别为 158 µV rms 和 2.1 µV rms，这两个值同样都在 HART 协议规范要求的范围内。

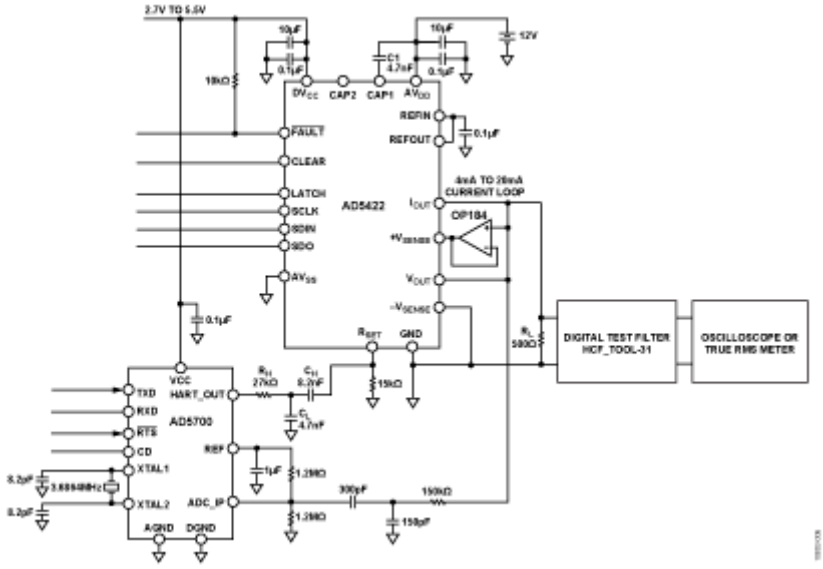

Figure 6. HART Specifications Test Circuit

图 6. HART 规范测试电路

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Figure 7 and Figure 8 show the oscilloscope plots for 4 mA and 12 mA output current, respectively. Note that the filter has a pass-band gain of 10. Channel 1 and Channel 2 on each plot show the input and output of the filter, respectively.

图 7 和图 8 分别显示 4 mA 和 12 mA 输出电流的示波器曲线图。注意，滤波器的通带增益为 10。每个曲线图上的通道 1 和通道 2 分别显示滤波器的输入和输出。

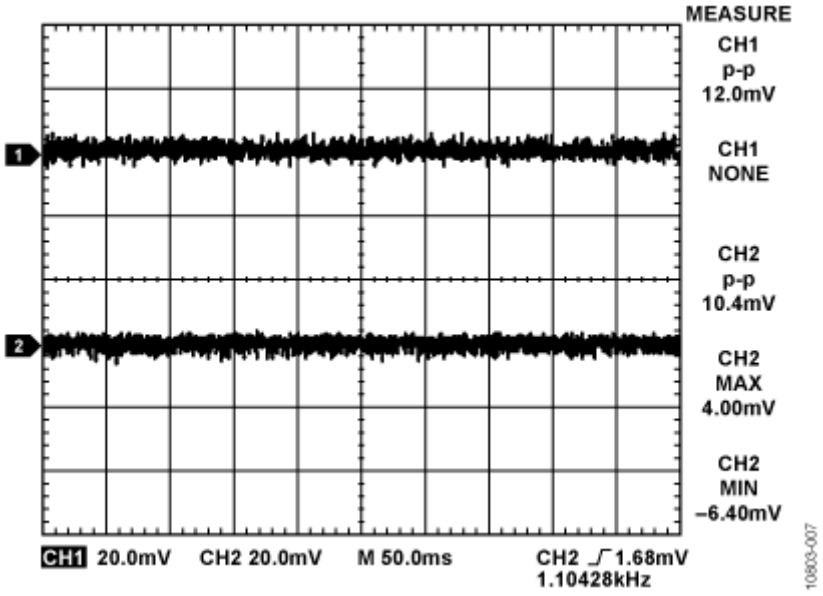

Figure 7. Noise at Input (CH1) and Output (CH2) of HART Filter with 4 mA Output Current

图 7. 输出电流为 4 mA 时 HART 滤波器输入（通道 1）和输出（通道 2）端的噪声

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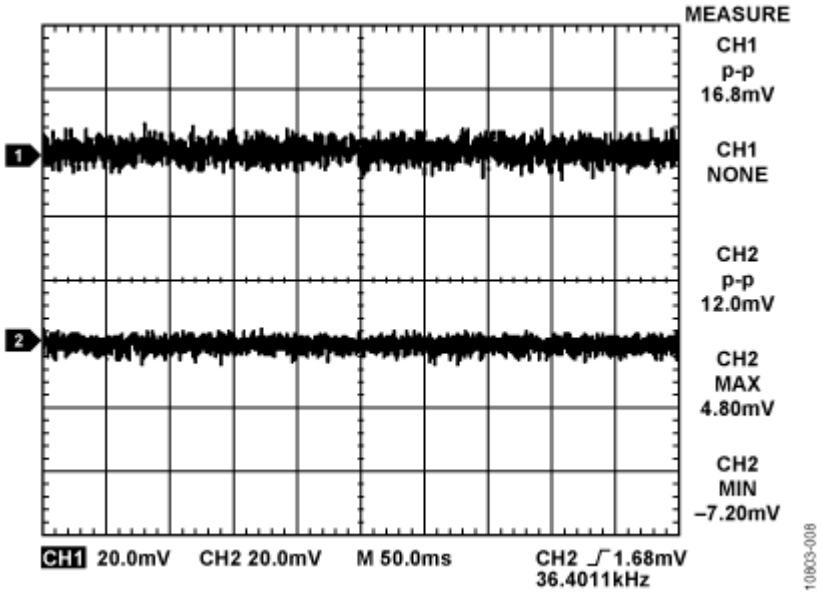

Figure 8. Noise at Input (CH1) and Output (CH2) of HART Filter with 12 mA Output Current

图 8. 输出电流为 12 mA 时 HART 滤波器输入（通道 1）和输出（通道 2）端的噪声

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Analog Rate of Change

模拟变化率

This specification ensures that when a device regulates current, the maximum rate of change of analog current does not interfere with HART communications. Step changes in current disrupt HART signaling. The same test circuit shown in Figure 6 was used. For this test, the AD5422 was programmed to output a cyclic waveform, switching from 4 mA to 20 mA with no delay at either value, to ensure the maximum rate of change. To meet the HART specifications, the waveform at the output of the filter must not exhibit a peak voltage greater than 150 mV. Meeting this requirement ensures that the maximum bandwidth of the analog signaling is within the specified dc to 25 Hz frequency band.

此规范可确保当设备调节电流时，模拟电流的最大变化率不会干扰 HART 通信。电流的阶跃变化会扰乱 HART 信号。仍然使用如图 6 所示的相同测试电路。为进行这个测试，AD5422 被编程为输出一个 4 mA 至 20 mA 切换的周期波形，该波形在两个值上都没有延迟，以获得最大变化率。为了符合 HART 规范，滤波器输出端波形的峰值电压不能大于 150 mV。符合这一要求可确保模拟信号的最大带宽处于规定的直流至 25 Hz 频带中。

The normal time for the output of the AD5422 to change from 4 mA to 20 mA is about 10 µs. This is obviously too fast and can cause major disruption to a HART network. To reduce the rate of change, the AD5422 employs two features: connecting capacitors at the CAP1 and CAP2 pins, and an internal linear digital slew rate control function (refer to the

AD5422 data sheet for details). For faster slew rates, a nonlinear digital ramp can be implemented on the controller/FPGA communicating with the AD5422.

AD5422 输出从 4 mA 变为 20 mA 的正常时间约为 10 µs。这个速度显然太快，而且会对 HART 网络造成重大破坏。为了降低变化率，AD5422 提供了两种特性：一是在 CAP1 和 CAP2 引脚处连接电容，二是提供内部线性数字压摆率控制功能（详情请参考 AD5422 数据手册）。对于较快的压摆率，可在与 AD5422 通信的控制器/FPGA 上实施一个非线性数字斜坡发生器。

It requires very large capacitor values at CAP1 and CAP2 to reduce the bandwidth below 25 Hz. The optimum solution is to use a combination of the external capacitors and the digital slew rate control function of the AD5422. The two capacitors, C1 and C2, have the effect of reducing the rate of change of the analog signal; however, not sufficiently enough to meet the specification. Enabling the slew rate control feature offers the flexibility to set the rate of change.

要使带宽降低到 25 Hz 以下，需要在 CAP1 和 CAP2 引脚处连接非常大的电容值。最佳解决方案是结合使用外部电容和 AD5422 的数字压摆率控制功能。两个电容 C1 和 C2 的作用是降低模拟信号的变化率；不过还不足以满足规范。使能压摆率控制功能可以为变化率的设置提供灵活性。

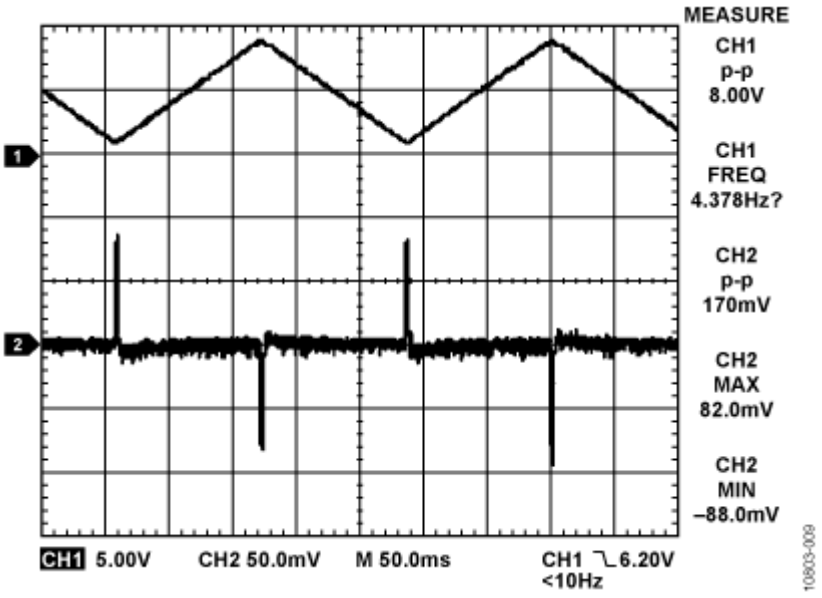

Figure 9. AD5422 Output (CH1) and HART Filter Output (CH2), SR Clock = 3, SR Step = 2, C1 = 4.7 nF, C2 = NC

图 9. AD5422 输出（通道 1）和 HART 滤波器输出（通道 2），SR 时钟= 3，SR 阶跃= 2，C1 = 4.7 nF，C2 = NC

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Figure 9 shows the output of the AD5422 and the output of the HART filter. The peak voltage at the output of the filter is within specification at 82 mV. The slew rate settings are SR clock = 3 and SR step = 2, setting the transition time from 4 mA to 20 mA at approximately 120 ms. C1 is 4.7 nF and C2 is unconnected. If this rate of change is too slow, the slew time can be reduced. With this circuit configuration of C1 = 4.7 nF and C2 unconnected, it was found that setting up an 80 ms slew time (SR clock = 1, SR step = 2) gave an analog rate of change result inside the HART specification. However, reducing the slew time further, to 60 ms (SR clock = 0, SR step = 2), pushed the result just outside of the 150 mV specification. The capacitor connected from CAP1 to AV_{DD} can be used to counteract the effect of the increased peak voltage at the output of the filter due to faster slew times. However, care must be taken when choosing this value because it has an effect on the low-pass filter frequency cutoff discussed in the Determining the Values of the External Components section.

图 9 显示了 AD5422 的输出和 HART 滤波器的输出。滤波器输出端的峰值电压为 82 mV，处于规定范围以内。压摆率设置为 SR 时钟= 3 和 SR 阶跃= 2，从 4 mA 至 20 mA 的转换时间设为约 120 ms，C1 = 4.7 nF，C2 未连接。如果这个变化率太低，可以缩短压摆时间。采用 C1 = 4.7 nF 且 C2 未连接的电路配置时，可以发现压摆时间设为 80 ms（SR 时钟= 1，SR 阶跃= 2）时，所得到的模拟变化率符合 HART 规范。然而，如果将压摆时间进一步缩短至 60 ms（SR 时钟= 0，SR 阶跃= 2），则会导致结果超出 150 mV 规格范围。从 CAP1 连接至 AV_{DD} 的电容可用于抵消滤波器输出端因压摆时间过快而导致的峰值电压增加。然而，选择此值时必须小心，因为它会影响“确定外部元件值”部分讨论的低通滤波器截止频率。

Figure 10 shows the results of changing the slew rate control settings to SR clock = 5 and SR step = 2, while leaving the C1 capacitor value unchanged at 4.7 nF. This results in a transition time of approximately 240 ms. The peak amplitude at the output of the filter can be reduced further by increasing the value of C1, configuring a slower slew rate, or a combination of both.

图 10 显示了压摆率控制设置改为 SR 时钟= 5、SR 阶跃= 2 且 C1 电容值保持 4.7 nF 不变的结果。这样，转换时间就会在 240 ms 左右。滤波器输出端的峰值幅度可通过增加 C1 值、配置更慢的压摆率或通过两者的组合来进一步降低。

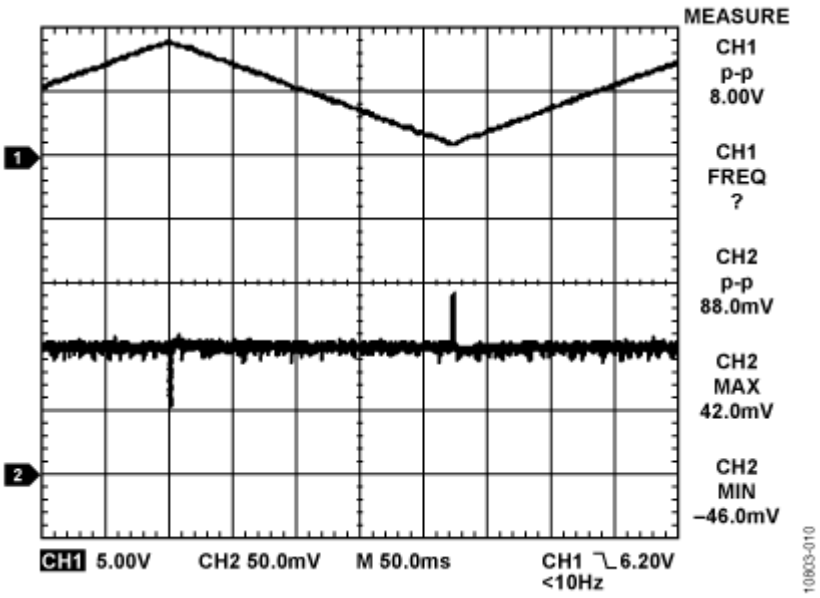

Figure 10. AD5422 Output (CH1) and HART Filter Output (CH2), SR Clock = 5, SR Step = 2, C1 = 4.7 nF, C2 = NC

图 10. AD5422 输出（通道 1）和 HART 滤波器输出（通道 2），SR 时钟= 5，SR 阶跃= 2，C1 = 4.7 nF，C2 = NC

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Transient Voltage Protection

瞬态电压保护

The AD5422 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5422 from excessively high voltage transients, external power diodes and a surge current limiting resistor may be required,as shown in Figure 1. The constraint on the resistor value, shown in Figure 1 as 18 Ω, is that during normal operation the output level at I_{OUT} must remain within its voltage compliance limit of AV_{DD} − 2.5 V, and the two protection diodes and resistor must have the appropriate power ratings. With 18 Ω, for a 4 mA to 20 mA output, the compliance limit at the terminal is decreased by V = I_{MAX} × R = 0.36 V. There is also a 10 kΩ resistor shown at the positive input of the OP184 buffer. This protects the amplifier by limiting the current during a transient event. Further protection can be provided with transient voltage suppressors (TVS) or transorbs. These are available as both unidirectional and bidirectional suppressors, and in a wide range of standoff and breakdown voltage ratings. Size the TVS with the lowest breakdown voltage possible while not conducting in the functional range of the current output. It is recommended that all remotely connected nodes be protected.

AD5422 内置 ESD 保护二极管，可防止正常操作造成的损害。但是，工业控制环境会使 I/O 电路遭受高得多的瞬变。为了防止过高瞬态电压影响 AD5422，可能需要外部功率二极管和浪涌电流限制电阻，如图 1 所示。对电阻值的约束条件（图 1 中显示为 18 Ω）是，在正常工作期间，I_{OUT} 的输出电平必须保持在其顺从电压限值(AV_{DD} − 2.5 V)以内，并且这

两个保护二极管和电阻必须具有适当的额定功率。在 18 Ω 的条件下，对于 4 mA 至 20 mA 输出，引脚处的顺从限值降低 V = I_{MAX} × R = 0.36 V。OP184 缓冲器的正输入端还连接了一个 10 kΩ 电阻，用以限制瞬态期间的电流来保护放大器。通过瞬态电压抑制器(TVS)或瞬态吸收器可实现进一步的保护。这些元件包括单向和双向抑制器，可提供各种各样的隔离和击穿电压额定值。TVS 应尽量采用最低击穿电压定标，同时在电流输出的功能范围内不导通。建议保护所有远程连接节点。

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur.

在许多过程控制应用中，需要在控制器与受控单元之间提供一个隔离栅，以保护和隔离控制电路，防止危险的共模电压破坏电路。

The iCoupler family of products from Analog Devices, Inc., provides voltage isolation in excess of 2.5 kV. Further information on iCoupler products is available at www.analog.com/icouplers. To reduce the number of isolators required, nonessential signals, such as CLEAR, can be connected to GND; FAULT and SDO can be left unconnected, reducing the isolation requirements to only three signals. However, note that either FAULT or SDO are required to provide access to the fault detection features of the AD5422.

ADI 公司的 *i*Coupler 系列产品可隔离高于 2.5 kV 的电压。有关 *i*Coupler 产品的详情，请访问 www.analog.com/icouplers。为了减少所需隔离器的数量，CLEAR 等非关键信号可以连到 GND；FAULT 和 SDO 可以不连接，从而只需要隔离三个信号。不过请注意，FAULT 或 SDO 引脚是访问 AD5422 的故障检测功能所必需的。

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COMMON VARIATIONS

常见变化

A common variation on the circuit shown in Figure 1 is to use the AD5420, which is similar to the AD5422, but contains only a current output. It therefore does not contain the OP184 buffer configuration at the output. This AD5420 and AD5700 HART modem circuit is described in more detail in CN-0270. Circuit Note CN-0065 provides extra information on an IEC 61000- compliant solution for a fully isolated output module using the AD5422 and the ADuM1401 digital isolator. Circuit Note CN-0233 contains information on providing power and data isolation using the ADuM3471 PWM controller and transformer driver with quad-channel isolators.

图 1 所示电路的一个常见变化是使用 AD5420，它类似于 AD5422，但只有一个电流输出。因此，其输出端没有 OP184 缓冲器配置。这种 AD5420 和 AD5700 HART 调制解调器电路详见 CN-0270。电路笔记 CN-0065 提供有关 IEC 61000 兼容解决方案的额外信息，该解决方案适合使用 AD5422 和 ADuM1401 数字隔离器的全隔离式输出模块。电路笔记 CN-0233 包含有关提供电源和数据隔离的信息，所使用的是 ADuM3471 PWM 控制器和具有四通道隔离器的变压器驱动器。

If multiple channels are required, the AD5755-1 quad voltage and current output DAC may be used. This product has innovative on-chip dynamic power control that minimizes package power dissipation in current mode. Each channel has a corresponding CHARTx pin so that HART signals can be coupled to the current output of the AD5755-1.

如果需要多个通道，可使用 AD5755-1 四通道电压和电流输出 DAC。该产品具有创新型片内动态电源控制功能，在电流模式下，可以最大限度地降低封装功耗。各通道均有一个相应的 CHARTx 引脚，因此 HART 信号可以耦合至 AD5755-1 的电流输出端。

The AD5421 and the AD5700 HART modem can be combined if the requirement is a loop powered, 4 mA to 20 mA HART solution. Such a HART enabled smart transmitter reference demo circuit was developed by Analog Devices and uses the AD5421, the ADuCM360, and the AD5700 modem. This circuit has been compliance tested, verified, and registered as an approved HART solution by the HART Communication Foundation.

如果需要环路供电的 4 mA 至 20 mA HART 解决方案，可以组合使用 AD5421 和 AD5700 HART 调制解调器。此类支持 HART 的智能发射机参考演示电路由 ADI 公司开发，采用了 AD5421、ADuCM360 和 AD5700 调制解调器。该电路已通过兼容性测试和验证，并注册为 HART 通信基金会认证的 HART 解决方案。

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CIRCUIT EVALUATION AND TEST

电路评估与测试

To build this circuit, it requires the use of the AD5422 evaluation board (EVAL-AD5422EBZ, LFCSP version) and the AD5700-1 evaluation board (EVAL-AD5700-1EBZ), see Figure 11. As well as the two evaluation boards, the circuit also requires three external capacitors (C1, C_H, and C_L), a resistor (R_H), a load resistor (R_L), a buffer amplifier, and a UART interface.

要构建此电路，需要使用 AD5422 评估板（EVAL-AD5422EBZ，LFCSP 版本）和 AD5700-1 评估板 (EVAL-AD5700-1EBZ)，参见图 11。除了这两个评估板之外，该电路还需要三个外部电容（C1、C_H 和 C_L）、一个电阻 (R_H)、一个负载电阻(R_L)、一个缓冲放大器以及一个 UART 接口。

Equipment Needed

设备要求

The following equipment is needed:

需要以下设备：

- The AD5422 evaluation board (EVAL-AD5422EBZ, LFCSP version)
- AD5422 评估板（EVAL-AD5422EBZ，LFCSP 版本）
- The AD5700 evaluation board (EVAL-AD5700-1EBZ)
- AD5700 评估板(EVAL-AD5700-1EBZ)
- A PC running Windows® XP with USB port
- 运行 Windows® XP 的 PC，带 USB 端口
- A host controller and an UART interface (standard microcontroller, for example, ADuC7060).
- 主机控制器和 UART 接口（标准微控制器，例如 ADuC7060）
- A power supply, 10.8 V to 60 V
- 10.8 V 至 60 V 的电源
- A digital test filter (HCF_TOOL-31 available from the HART Communication Foundation)

- 数字测试滤波器（HCF_TOOL-31，可从 HART 通信基金会获得）
- A load resistor, 500 Ω
- 500 Ω 负载电阻
- The OP184 amplifier (on separate breadboard with connecting wires)
- OP184 放大器（位于单独的试验板上且带有连接线）
- External capacitors, C1 (4.7 nF), C_H (8.2 nF), and C_L (4.7 nF); and a resistor, R_H (27 kΩ)
- 外部电容 C1 (4.7 nF)、C_H (8.2 nF)和 C_L (4.7 nF)；电阻 R_H (27 kΩ)
- An oscilloscope, Tektronix DS1012B or equivalent
- Tektronix DS1012B 示波器或等同产品

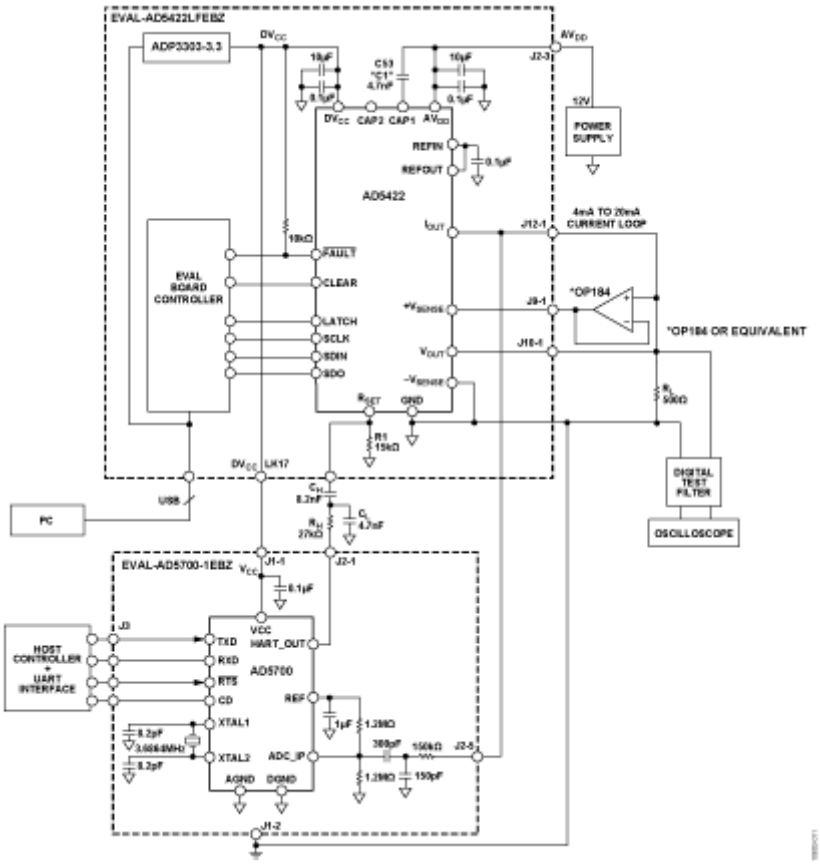

Figure 11. Test Setup Block Diagram

图 11. 测试设置框图

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Noise During Silence Measurements— AD5422 LFCSP

静默期间噪声测量 — AD5422 LFCSP

As described previously, for the output noise during silence tests, the AD5700 modem was not transmitting (silent). The AD5422 was set to output the required current and passed through the HART Communication Foundation band-pass filter. The output noise was then measured using a Tektronix TDS1012B oscilloscope and found to be within the HART Communication Foundation protocol specifications.

如前文所述，对于静默测试期间的输出噪声，AD5700 调制解调器并未在发射数据（静默）。AD5422 设置为输出所需的电流并通过 HART 通信基金会带通滤波器。接着使用 Tektronix TDS1012B 示波器测量输出噪声；结果显示输出噪声在 HART 通信基金会协议规范要求的范围内。

Analog Rate of Change Measurements— AD5422 LFCSP
模拟变化率测量 — AD5422 LFCSP

The analog rate of change specification ensures that when the AD5422 regulates current, the maximum rate of change of analog current does not interfere with HART communications. Step changes in current disrupt HART signaling. For this test, the AD5422 was programmed to output a cyclic waveform switching from 4 mA to 20 mA with no delay at either value to ensure the maximum rate of change. The slew rate settings used were SR clock = 3 and SR step = 2, with C1 set to 4.7 nF and C2 open circuit.

模拟变化率规范可确保当 AD5422 调节电流时，模拟电流的最大变化率不会干扰 HART 通信。电流的阶跃变化会扰乱 HART 信号。为进行这个测试，AD5422 被编程为输出一个 4 mA 至 20 mA 切换的周期波形，该波形在两个值上都没有延迟，以获得最大变化率。所用的压摆率设置为 SR 时钟= 3 和 SR 阶跃= 2，C1 设置为 4.7 nF，C2 保持开路。

Measurements were also completed whereby the slew rate was reduced even further by changing the SR clock setting to 5 rather than 3, and leaving all other settings and component values unchanged, the effects of which can be seen if Figure 9 and Figure 10 are compared.

此外，再将 SR 时钟设置改变为 5 而不是 3，并保持其它所有设置和元件值不变，从而进一步降低压摆率，由此另外进行测量；至于相关影响，可比较图 9 和图 10 来得出。

Noise During Silence Measurements—AD5422 TSSOP

静默期间噪声测量 — AD5422 TSSOP

Extra measurements were also taken in an effort to simulate the behavior of the AD5422 TSSOP package option in this configuration; however, without the capacitor on the CAP1 pin (C1) present (because the TSSOP version of this part does not contain a CAP1 pin).

另外还执行了额外测量，以模拟 AD5422 TSSOP 封装选项在这种配置下的表现；不过，没有连接在 CAP1 引脚的电容 (C1)（因为此器件的 TSSOP 版本没有 CAP1 引脚）。

While the results for output noise during silence tests were greater without C1 in place, than in the case of the LFCSP part with C1 in place, they were still within the HART Communication Foundation protocol specifications. Channel 2 in Figure 12 and Figure 13 shows the broadband noise results with the HCF_TOOL-31 filter in place, 530 µV rms for 4

mA I_{OUT} and 690 µV rms for 12 mA I_{OUT}. These plots can be compared with Figure 7 and Figure 8 to show the effect of the presence of C1.

虽然与有 C1 的 LFCSP 器件相比，没有 C1 时测得的静默期间输出噪声值更大，但还是在 HART 通信基金会协议规范要求的范围内。图 12 和图 13 中的通道 2 显示了有 HCF_TOOL-31 滤波器时的宽带噪声，I_{OUT} 为 4 mA 时结果为 530 µV rms，I_{OUT} 为 12 mA 时结果为 690 µV rms。可将这些曲线图与图 7 及图 8 进行比较，以体现有无 C1 的影响如何。

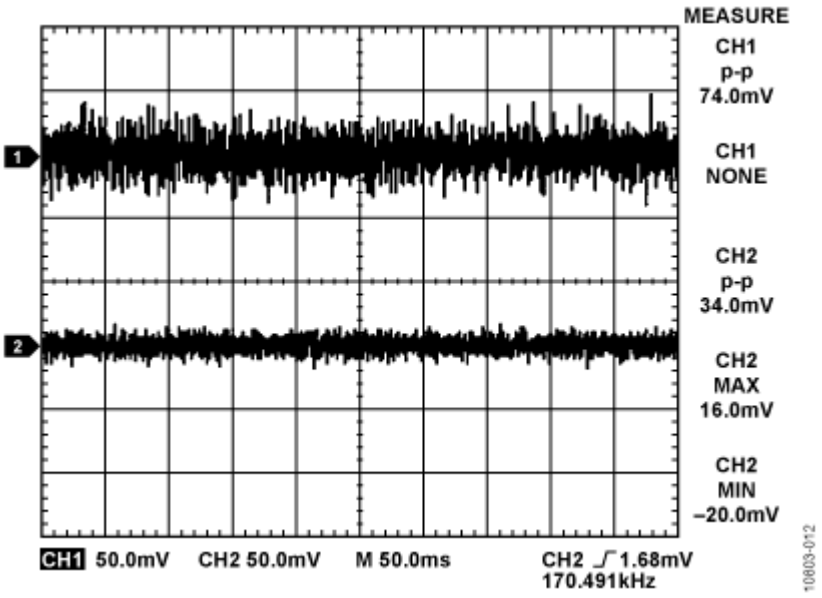

Figure 12. Noise at Input (CH1) and Output (CH2) of HART Filter with 4 mA Output Current, C1 Not in Place

图 12. 无 C1 且输出电流为 4 mA 时 HART 滤波器输入（通道 1）和输出（通道 2）端的噪声

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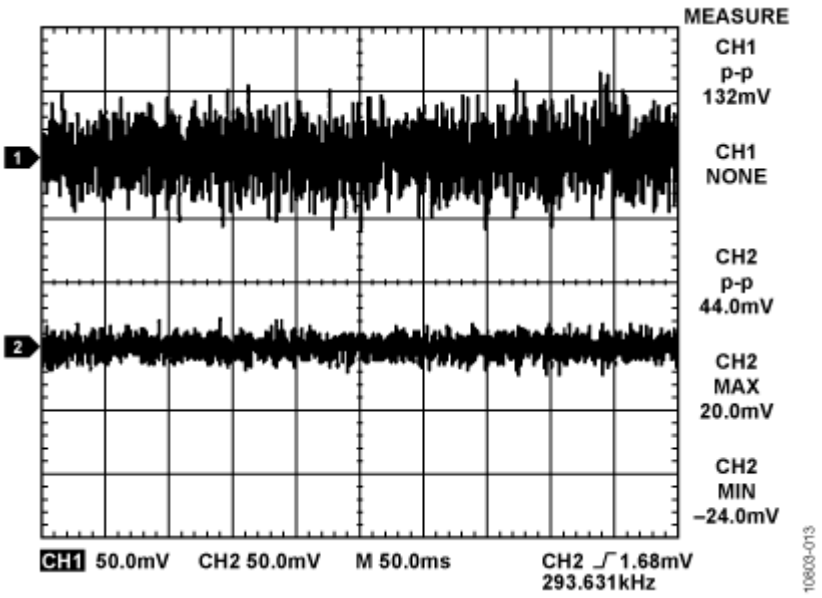

Figure 13. Noise at Input (CH1) and Output (CH2) of HART Filter with 12 mA Output Current, C1 Not in Place

图 13. 无 C1 且输出电流为 12 mA 时 HART 滤波器输入（通道 1）和输出（通道 2）端的噪声

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Analog Rate of Change Measurements— AD5422 TSSOP

模拟变化率测量 — AD5422 TSSOP

In terms of the analog rate of change test, the maximum peak result with and without C1 in place were similar. The main difference seen between the results was that without C1, the peak to peak noise floor was much larger. Figure 14 and Figure 15 show the analog rate of change plots for a slew rate of 120 ms (SR clock = 3 and SR step = 2) and 240 ms (SR clock = 5 and SR step = 2), respectively.

从模拟变化率测试的角度来看，无论有无 C1，最大峰值结果都相似。主要区别在于，没有 C1 时，峰峰值本底噪声要大得多。图 14 和图 15 分别是压摆率为 120 ms（SR 时钟= 3 和 SR 阶跃= 2）和 240 ms（SR 时钟= 5 和 SR 阶跃= 2）时的模拟变化率曲线图。

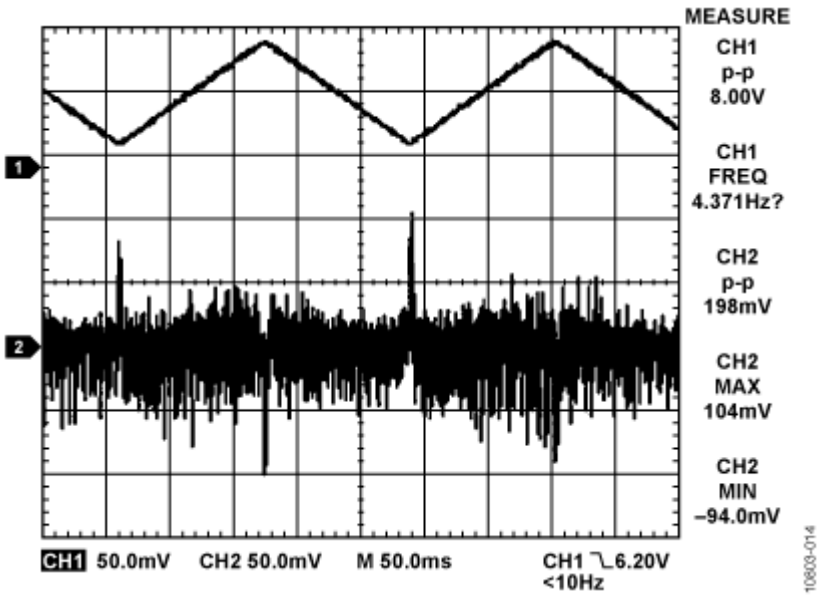

Figure 14. AD5422 Output (CH1) and HART Filter Output (CH2), SR Clock = 3, SR Step = 2, C1 = NC, C2 = NC

图 14. AD5422 输出（通道 1）和 HART 滤波器输出（通道 2），SR 时钟= 3，SR 阶跃= 2，C1 = NC，C2 = NC

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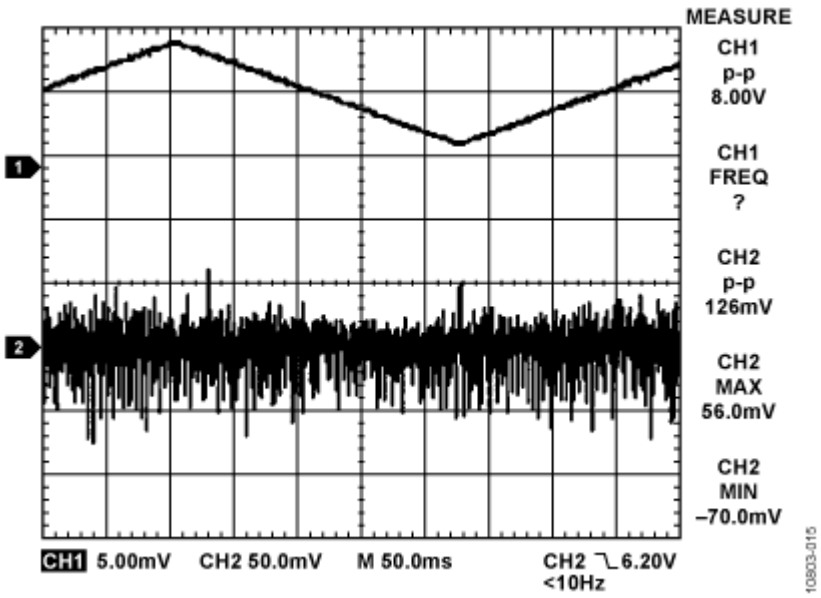

Figure 15. AD5422 Output (CH1) and HART Filter Output (CH2), SR Clock = 5, SR Step = 2, C1 = NC, C2 = NC

图 15. AD5422 输出（通道 1）和 HART 滤波器输出（通道 2），SR 时钟= 5，SR 阶跃= 2，C1 = NC，C2 = NC

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Again, these plots can be compared with Figure 9 and Figure 10 to show the effect of the presence of C1. While the HART-coupling technique used in this circuit configuration requires the use of the external R_{SET} resistor, note that even if the HART portion of this circuit is not implemented, the addition of the buffer causes a marginal degradation on I_{OUT} accuracy when the internal R_{SET} resistor is used. It is, therefore, recommended to use the external R_{SET} resistor when using this buffer configuration to tie the voltage and current output pins together.

同样，可将这些曲线图与图 9 及图 10 进行比较，以体现有无 C1 的影响如何。虽然这种电路配置中所用的 HART 耦合技术要求采用外部 R_{SET} 电阻，但请注意，即使该电路的 HART 部分未实施，添加缓冲器也会在使用内部 R_{SET} 电阻时造成 I_{OUT} 精度略微降低。因此，在使用这种缓冲器配置将电压和电流输出引脚连接在一起时，建议使用外部 R_{SET} 电阻。

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