A Smart Modem for Robust Wireless Data Transmission Over ISM Bands (433 MHz, 868 MHz, and 902 MHz)

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In the last few years, radio-frequency technology has advanced by leaps and bounds, resulting in a phenomenal number of new wireless applications. Most of these applications—Bluetooth^{*},¹ WLAN 802.11b,² and cordless telephones, for example—are appearing alongside the microwave oven in the license-free UHF band at 2.4 GHz. Because of the heavy traffic in the 2.4-GHz band, and its associated co-existence issues, interest has increased in the ISM (industrial, scientific, medical) UHF bands—available at the lower frequencies of 868 MHz and 433 MHz in Europe, and 902 MHz to 928 MHz in the United States.

Unlike at 2.4 GHz, however, there is no common global standard for the lower-UHF bands; this means that a manufacturer's system would have to be adaptable to each region's regulations. However, this burden has been eased considerably by the introduction of flexible ISM-band transceivers, such as the ADF7020,³ which allow operation from 433 MHz to 960 MHz.

Unfortunately, one cannot entirely eliminate the problem of interference and co-existence by simply switching to these lower-UHF bands. As might be expected, there are plenty of legacy systems already operating in these bands. In wireless systems, data will be corrupted if an interferer collides with the wanted signal—resulting in an insufficient signal-to-noise ratio (SNR) at the receiver. A traditional way of dealing with this problem is to use some sort of error-detection technique, e.g., *cyclic redundancy checking* (CRC). CRC can detect this corruption to a certain extent and trigger the retransmission of erroneous packets (this is usually called *automatic repeat request*, ARQ), but at the cost of considerable delay and loss of performance in real-time applications. This need to retransmit corrupted packets is not particularly onerous for a low-throughput system—one that sends a burst of data from a remote sensor once every few minutes, for example. But it does become a problem for applications such as wireless audio or video transmission, with their higher data rates, since the latency introduced by ARQ might be unacceptable. It also introduces problems in industrial process-control and telemetry systems, which must maintain throughput in a noisy environment without the need for many retransmissions. Such longer associated transmission times also increase the overall system power consumption.

A powerful solution to this dilemma lies in the use of *forward* error-correction (FEC) techniques, able to detect and correct errors over a large enough number of bits to compensate for partial packet loss and ensure service quality. A low-cost, yet powerful, processor such as the Blackfin^{*4} ADSP-BF531⁵ can be used to implement intensive error-correction techniques requiring millions of instructions per second (MIPS)—convolutional coding with bit-scrambling and interleaving, for example—to deliver a data rate of over 100 kbps with a transmission error rate of less than 10⁻⁶.

When used in conjunction with the ADF7020 ISM-band transceiver IC, with its typical range of several hundred meters (line of sight), this approach provides a robust solution for designers wanting to replace their current wire-line solutions without compromising quality of service. Thanks to its 400-MIPS (*million instruction-persecond*) and 800-MMACS (*million multiply-accumulate-per-second*) capabilities, the ADSP-BF531 can also accommodate protocols to support various wireless configurations and topologies, including point-to-point, multi-point, and broadcast, as well as sophisticated encryption and source coding and decoding algorithms such as Motion JPEG (MJPEG).

Figure 1 is a detailed circuit diagram of a wireless digital modem built around the ADF7020 ISM-band transceiver and its companion controller, the ADSP-BF531. The two main chips share the same power supply voltage (2.3 V<V_{CC}<3.6 V), and they are



Figure 1. Circuit diagram of the modem.

directly connected for *control* operations, using the ADSP-BF531 flags (digital I/Os) and *transmit/receive* operations, using one of the serial synchronous ports (SPORT0).

Data will be transmitted to—or received from—the modem, either asynchronously over the UART or synchronously with the remaining SPORT.

A Versatile Transceiver

The ADF7020 is a complete monolithic radio transceiver built using $0.25-\mu m$ CMOS technology. It is capable of operating in the 433-MHz and 868-MHz European ISM bands (ETSI EN300 220-1 standard),⁶ and the North American 902-to-928-MHz band—covered by FCC Part 15 regulations.⁷ Requiring few external components and offering a high degree of flexibility, it allows the user to configure the part for specific applications. For example, there is a choice among different modulation schemes, such as FSK, GFSK, ASK, and OOK. The user can also trade off between sensitivity and selectivity—a useful approach for systems that have tough linearity requirements. The maximum data rate for the ADF7020 is 200 kbps; its sister part, the ADF7025,⁸ has an even greater data rate: 384 kbps.

Like most recent ISM-band transceivers, the ADF7020 utilizes a fractional-N phase-locked-loop (PLL) synthesizer, which allows the selection of the channels at 433 MHz, plus any channel between 868 MHz and 928 MHz, with a resolution better than 1 kHz. This frequency agility allows the ADF7020 to be used in frequency-hopping systems—as specified in the US FCC Part 15

regulations—but it is also possible to operate on a single channel in the US band if the output power is below -1.5 dBm.

The high-resolution fractional-N synthesizer also forms part of a novel *automatic frequency-control* (AFC) loop, which compensates for incoming frequency errors and allows lower-tolerance, less-expensive, crystals to be used. The block diagram of the ADF7020 is shown in Figure 2. The PLL loop filter components can be determined with the help of the ADIsimPLL⁹ simulation software, available on the Analog Devices website.

Forward Error-Correction with the Blackfin Processor

While the use of a really high-performance processor in conjunction with a radio is common in digital cellular systems, it might at first glance seem inappropriate for meeting the goal of a low-cost digital modem. Implementing FEC operations at several hundred kilobits per second, however, requires computationally intensive digital signal-processing power comparable to that provided by the Blackfin ADSP-BF531. While a standard 8051 or ARM-based microcontroller, for example, can adequately handle the user interface, protocol stack, RF transceiver supervision, and power sequencing, it would not have the computation "horsepower" required for the FEC scheme. In addition to implementing the control functions, the computing power and real-time capabilities of the ADSP-BF531 allow it to: increase the effective channel data rate, reduce communication latency, compensate for channel propagation variations to maintain link quality, and ensure communication security.



Figure 2. Functional block diagram of the ADF7020.



Figure 3. Signal-processing functions.

Figure 3 illustrates the various functions to be carried out across the transmission channel, including processing functions handled for both *transmit* (Tx) and *receive* (Rx) operations. The Blackfin processor, when sitting on the transmitter side handles both data-rate control and data partitioning, so data is transmitted in packets at a quasi-constant rate. The data packets are processed for forward error-correction (FEC) before they modulate the carrier's frequency. This is achieved by adding redundant bits that the receiver will use to detect and correct errors. The bits added to the incoming packets will, of course, increase the required bandwidth for a given information bit rate.

Among the different applicable methods of FEC, *convolutional coding*, while quite simple to implement, gives good protection against channel Gaussian noise disturbances and helps meet minimum Hamming-distance criteria. A convolutional encoder is a finite state-machine comprising an L-stage shift register, N modulo-2 adders, and a multiplexer to convert the output into a serial bit stream. The connections between the shifter outputs and the adder inputs determine the polynomial code. Using two specifically applicable instructions, the Blackfin core performs all these operations very efficiently.

At the other end of the transmission channel, the decoder section implements the Viterbi algorithm (hard-input/hard-output). For maximum likelihood decoding, the Viterbi decoder compares all the possible code sequences to the received code vector. The code sequence whose Hamming distance from the received sequence is the shortest is the good one. For a code like (1/2, 7, 371, 247) with a constraint length, K = L + 1 of 7, the decoder can correct up to six consecutive erroneous bits. Depending upon the system requirements, constraint lengths (K) from 5 to 9 must be supported by the ADSP-BF531 in such wireless applications.

However, even a convolutional code with a constraint length of 9 does not protect against burst noise that might hit the transmitted packets over a longer length of time. The use of a complementary protection technique based on temporal diversity is mandatory. *Temporal diversity*, i.e., spreading the bits or symbols out over time, improves the performance of a coded communication system in the presence of multiple paths, fading, and burst noise. It thus reduces the probability of a consecutive number of bits being corrupted. Scrambling and simple block interleaving functions achieve this objective without employing more complex corrective codes (like Reed-Solomon). Here again, the ADSP-BF531 is helpful with two specific vector instructions—one that computes the Viterbit trellis butterflies and one that reconstructs data for the path-search (trace-back) operation.

This encoded data is then passed on to the ADF7020 transmitter section, which does some additional filtering and Gaussian frequency-shift-keying (GFSK) modulation. GFSK modulation has the advantage of reducing the occupied spectral bandwidth—a helpful operation when seeking to meet adjacent-channel requirements for the European 868-MHz bands.

On the receiver side, the ADF7020's internal preamble-matching circuitry helps to fulfill the critical packet-synchronization task. This hardware function permits the recognition or identification of a 12-, 16-, 20-, or 24-bit-long programmable synchronization word, or a packet preamble, without the intervention of the ADSP-BF531 core. Upon a valid preamble match, the circuitry asserts the ADF7020 INT/LOCK pin, which signals the beginning of a new packet to the serial port (RFS0) and triggers the Viterbi decoder. This unique circuitry is somewhat error-tolerant-in a sense, it even allows a valid match for up to three incorrect bits. This reduces the number of packets lost due to preamble misses, as the preamble is not encoded and is therefore not protected. To further reduce preamble misses, the receiver uses one of the ADSP-BF531 32-bit timers as a watchdog that generates the expected pulse on RFS0 if the INT/LOCK signal does not show up after a few symbols. This use of a hardware mechanism to retrieve packet synchronization markers was chosen in order to save a lot of processor MIPS-compared to a full implementation with software analysis and tracking.

Real-World Application–Wireless Video Over ISM

As noted earlier, efficient wireless digital-video transmission calls for robustness against channel failures. Video codecs are excellent candidates for applications with smart, reliable Blackfin processor-based wireless modems. Given the limitation of the ISM wireless channel bandwidth, a relatively high image/video compression ratio is required in order to deliver the expected frame rate and quality for a given image size without too much latency. Unfortunately, Motion JPEG and other video codecs require a very low transmission-error rate, typically 10⁻⁶, because the source-coding process removes most of the redundant information. This is particularly true with some efficient entropy coders, such as Huffman, where a single erroneous bit makes the original data impossible to decode. A required bit-error rate (BER) less than 10^{-6} places very stringent requirements on the radio, but it can be achieved by using a channel coding scheme like the one described above.



Figure 4. Video transmission system application.

A very low BER does not ensure that all the data packets will be entropy-decoded correctly. To improve the image quality, it is necessary to provide some mechanism to conceal part of an image if too many important bits in a packet are corrupted. For this purpose, every packet is segmented and entropy-coded separately. After the detection of an erroneous segment or block, its content is discarded. Depending upon the information lost, the dc and first two ac coefficients of the discrete cosine transform (DCT) of the corresponding image block are estimated from the coefficients of the neighboring blocks. The final low-pass 2D 3×3 de-blocking filter stage, designed to remove DCT blocking artifacts, helps to smooth resulting distortion.

The ADSP-BF531 has more than enough power to handle both the MJPEG encoding or decoding and the channel FEC processing. No external memory is required for frame sizes up to QCIF (176 pixels by 144 pixels) with a 4:2:2 video format. Larger frames are possible at the cost of an external SDRAM, which can also be used to store compressed video. This very low-cost processor can interface directly to CCIR-656-compatible low-cost CMOS image sensors or TFT displays via its *parallel peripheral interface* (see "Blackfin Processor's Parallel Peripheral Interface Simplifies LCD Connection in Portable Multimedia").¹⁰ Standard low-cost, low-power PCM audio codecs can be connected to the available serial port, SPORT1, to support digital transmission of speech or audio. Or, the processor can provide speech coding and decoding with moderate delay by executing a software codec similar to the FR-GSM (13 kbps).

With a raw data rate of 200 kbps it is possible to achieve "baseline" MJPEG transmission over ISM at a rate of about four QCIF 4:2:2 color-frames per second (fps), while leaving 20 kbps for speech. This is acceptable for simple low-cost consumer appliances, such as video baby monitors, video door phones, or wireless home-security cameras. The functional block diagram of such a point-to-point video transmission system (baby monitor)

is shown in Figure 4. The overall bill of materials (BOM) for this application is in the \$75 range; and the 2.5" LCD TFT display is the most expensive part.

The application code corresponding to the system block diagram shown at Figure 4 is available from Arbos Ingénierie (www.arbos-dsp.com),¹¹ a French DSP third-party partner of Analog Devices.

CONCLUSION

The unique combination of the ADF7020 ISM-band transceiver and the ADSP-BF531 Blackfin processor exhibits excellent radiolink performance at a very attractive cost, with demonstrable versatility in various ISM digital wireless transmission systems. Further improvements to this communications model can be anticipated with future members of the ADF702x RF transceiver family and new TCP/IP friendly Blackfin DSP processors, together with additional channel- and source-coding software modules.

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