Versatile Mixed-Signal Front Ends Speed Customized Design of Wireline Broadband Modems and Home Networks

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INTRODUCTION

The widespread growth of broadband modems (predominantly based on cable and DSL technology) has made broadband communications available to residential households throughout the world for use in applications such as Internet access, interactive gaming, and telecommuting. The number of households with multiple personal computers (PCs) is also on the rise. The ready availability of these facilities has led to the increasing popularity of home networking for sharing Internet access and printer resources for work, academics, and entertainment. Figure 1 shows a typical domestic network connected to the broadband gateway and to various devices inside the residence/office.

A variety of technologies have been developed to address high-speed communication between home computers and peripheral devices—and to interface to the hub (or gateway) for broadband access. Until recently, Ethernet has been the most viable method for providing networking within the home. The attractiveness of Ethernet has been the availability of inexpensive network interface cards based on proven technology. However, Ethernet suffers from one main disadvantage—the requirement of having Category 5 (CAT5) cable wired throughout the home. This almost always means that the homeowner must run new wires—a cumbersome and potentially expensive solution.

Wireless LAN provides an alternative to Ethernet that does not require installation of new wires. Despite the convenience of a wireless solution, it has achieved limited success due to higher cost, potential insecurity, multiple competing standards, lack of interoperability, and interference/robustness concerns. Recent advancements in the wireless standards within IEEE 802.11 and the emergence of the WiFi consortium have increased the prospects for wireless home networking. Nevertheless, the scarcity of frequency spectrum and the ubiquity of potent interferers—such as microwave ovens, garage door openers, etc.—will continue to pose numerous challenges to a wireless home network, including increased cost.

The newer preferred wireline technologies are those that require "no new wire"; they offer the homeowner a potentially better way of establishing a home network by avoiding the burden of installing new cabling, while providing comparable performance to that of Ethernet at an affordable price. The two choices for operating over the installed infrastructure involve either telephone or power-line wiring. Until recently, utilizing existing home wiring for broadband networking was impossible due to very poor channel quality. However, cost-effective broadband home networking is now a reality because of advances in signal-processing techniques, lowered costs resulting from perennial reduction of silicon fabrication geometries, and performance improvements in high-speed mixed-signal circuitry. The Home Phone Networking Alliance (HPNA) standard provides the framework for phone-line networking and allows data rates of up to 10 Mbits/s. And the HomePlug™ standard describes the specifications for implementing a power-line network system with data rates comparable to those of HPNA.

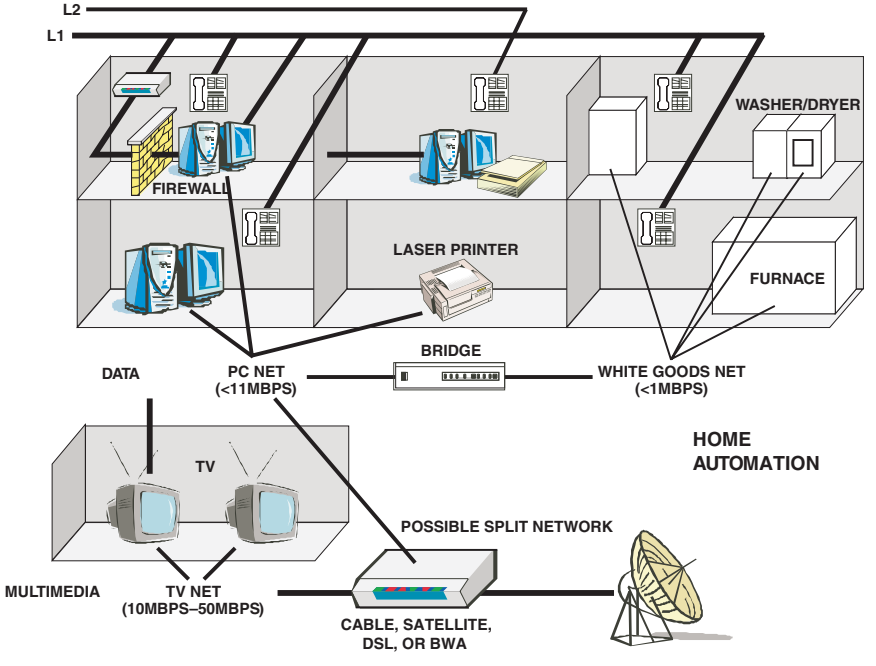


Figure 1. Home-networking/broadband access configuration.

These wireline home networking technologies, together with high-speed access technologies like DSL and cable, require mixed-signal interfacing between the transmission medium (power line, cable, twisted pair) and the digital baseband processors and controllers. Analog Devices has developed a family of monolithic mixed-signal front-end (MxFE™) integrated circuits (ICs) to bridge this gap (see *Analog Dialogue* Volume 35, Number 1, January–February, 2001 article, "AD9873 Mixed-Signal (MxFE) Front End for Broadband Digital Set-Top Boxes").

The recently introduced AD9875 and AD9876 MxFE devices, to be discussed in this article, were developed and aimed specifically at broadband home-networking and broadband access applications, both of which require high data rates or signal bandwidth up to 25 MHz and impose similar demands in functionality, performance, and cost. Given their flexibility, these parts can be used in modems for both home networking (HomePlug, HPNA) and high-speed data access (VDSL, power line). Developed for large volume, cost-sensitive, consumer-class applications, they offer exceptional value to providers of system solutions.

Figure 2 depicts the versatile role played by the MxFE chip. Its receive (Rx) circuitry accepts the (analog-domain) signals from the transmission medium, once they have been appropriately interfaced, and provides analog signal conditioning and A/D conversion to produce multiplexed digital signals that can be dealt with by the digital physical layer (PHY) and/or media access controller (MAC). It also accepts digital data from these entities, processes it and converts it to analog—and outputs this transmit (Tx) signal to the media interface. The device design is based on the objective of optimizing system performance—irrespective of the analog or digital nature of its I/O—as implemented in ADI's "smart-partitioning methodology" (see Appendix).

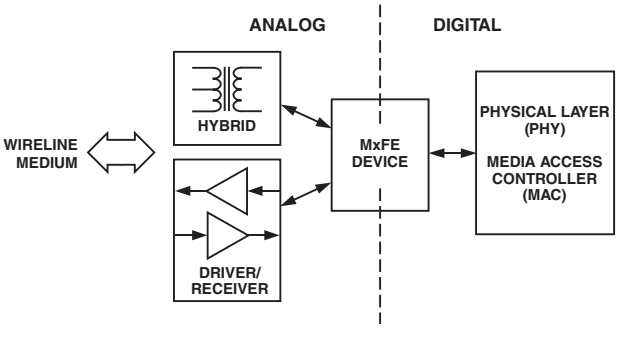


Figure 2. Typical wireline network node.

Figure 2 represents a typical wireline network node. The MxFE function may be connected to the wireline medium passively through a hybrid transformer block, or actively, with an amplifier on the receive side and a driver on the transmit side. On the digital side, the MxFE device needs to interface with the PHY and the MAC, which reside on a separate chip.

Critically important factors for the designer of MxFE circuitry for the home networking and high-speed access markets are performance, time to market, and low cost. In this type of emerging broadband communication application, discrete analog components can be prohibitively expensive, power-hungry, and demanding of board space. The combination of cost, performance, size, and power dissipation made possible by integrating the difficult mixed-signal, analog, digital, and signal processing functions on a single chip—such as the AD9875/AD9876—makes complex consumer-market communication products feasible. In fact, by implementing their intellectual property and design expertise in a digital gate array or ASIC, in conjunction with these devices, design engineers can develop new products and prototypes faster than ever to capitalize on rapidly changing markets.

Figure 3 shows a block diagram of the AD9875/AD9876 mixed-signal front end converter for broadband modems. On the analog side, the AD9875 and AD9876 combine the ADC, DAC, clock generation, programmable-gain amplification, and analog and digital filtering circuitry to provide a level of integration and performance usually implemented with discrete solutions costing significantly more. The ADC uses a pipelined multistage architecture to achieve high sample rates while consuming low power. In the AD9875, the receive path provides 9.5 ENOB @ 32 MSPS and 8.6 ENOB @ 50 MSPS. Comparable numbers for the AD9876 are 10.2 ENOB @ 32 MSPS and 9.3 ENOB @ 50 MSPS. The DACs in each device are, respectively, 10- and 12-bit interpolating TxDAC™ circuits.

On the digital side, the DAC inputs and ADC outputs are available on separate ports to accommodate both full-duplex and half-duplex operations. Each converter's port is multiplexed into high- and low nybbles to reduce the number of package pins. [A 10-bit half-duplex device, the AD9875-HD, available in summer 2002, will connect seamlessly to currently available HomePlug-compliant physical-layer digital ASICs that support multiplexed transmit and receive data ports.]

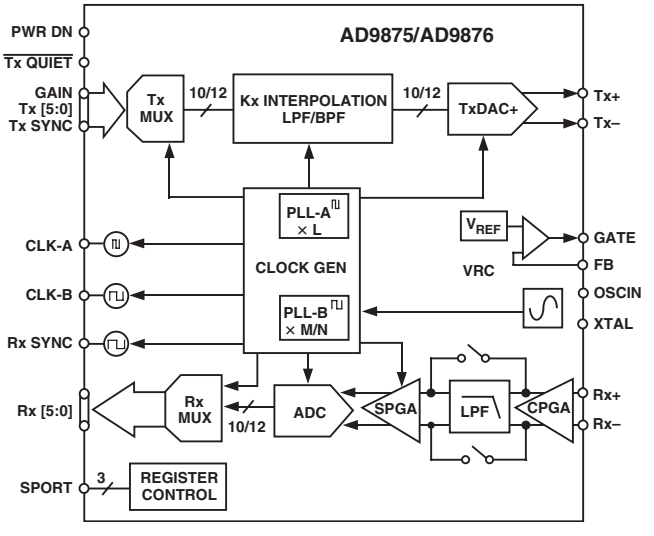


Figure 3. AD9875/AD9876 block diagram.

The availability of low-cost, flexible, high-performance, off-the-shelf mixed-signal front ends, such as these, with optimized functionality for broadband modem design using a variety of modulation formats—including OFDM—simplifies the ASIC design, specification, and testing process for both vendor and OEM and can substantially cut time to market. The unique features of the AD9875/AD9876 make these parts ideal for phone and power line networking as well as some xDSL applications.

Broadband wireline modems

Wideband signals with high peak-to-average ratios, commonly found in broadband modems—irrespective of the modulation scheme employed—put great demands on the system's analog- and mixed-signal processing components. Figure 2 and the

AD9875/AD9876 block diagram in Figure 3 together show details of a generic wireline broadband modem. Not every modem requires every block shown, although most of them do employ the same or similar functions, while others may even require additional functional blocks like additional analog filtering. The block-level components of a wireline modem can be grouped into three main functions; a transmit path, a line coupler or hybrid, and a receive path. Most of the transmit and receive blocks are addressed directly by the AD9875/AD9876 component.

The main function of the transmit path is to send the signal onto the line with sufficient fidelity to reach the far end of the wire with a high enough signal-to-noise ratio (SNR) to allow faithful decoding at the receiver end. Invariably, the transmitter must also do this while conforming to a spectral mask to ensure that the modem does not cause excessive noise outside its channel bandwidth. Meeting the requirements of a power spectral-density (PSD) mask usually drives the design and performance requirements of the transmit path components. The two converter parameters that get the most attention are the number of bits and the sampling rate.

For the DAC, the number of bits required will depend on the desired SNR, the signal's peak-to-average ratio (PAR) and the ratio of the signal bandwidth to the sample rate. For a given SNR requirement, higher-precision converters are required as signal bandwidths and PARs increase. Often the most demanding DAC performance parameter turns out to be its spurious-free dynamic range (SFDR). The spurs generated by the non-ideal DAC transfer function may show up anywhere in the spectrum. If the magnitudes of the spurs are high and fall close to the signal band, they may be impossible to filter adequately. The DAC's SFDR performance must be able to meet the system linearity requirements.

The AD9875/AD9876 incorporates a 10-/12-bit DAC and makes use of interpolation filters to oversample the input data. Oversampling, because it moves DAC image frequencies away from the frequency of the desired signal, may result in substantially simpler external analog filter requirements, which translate into lower complexity and cost. Ideally, the driver will be able to provide the transmit-path gain and deliver the required output power while maintaining the DAC linearity performance. In cases where the DAC's available peak output power is not sufficient, AD832x cable drivers or AD8xxx DSL drivers could provide the interface to the wire. To deliver high peak-output signal with low distortion requires high voltage rails and high bias currents in the amplifier's output stage, which conflicts with the need for low power consumption and CMOS integration.

The method of coupling the modem's analog front-end to the line depends on whether the type of modulation/demodulation (modem) is time-domain duplex (TDD) or frequency-domain duplex (FDD). A TDD modem will normally employ a simple transformer coupling to the line and a switch that connects either the transmitter or receiver to the transformer. The main concern is that the switching and settling times, when the connections are made, meet the system requirements. An FDD modem will normally employ a hybrid to connect the modem's analog front-end to the line. A hybrid is required because the modem can be transmitting large signals while the receiver is listening to greatly attenuated signals—which can be orders of magnitude smaller. In order to limit the amount of signal coupling from the transmitter to the receiver, some type of line matching, cancellation circuitry, and filtering is used. The AD9875/AD9876 integrates a low-pass analog receive filter (LPF in Figure 3) with variable cutoff to provide for various signal bandwidth requirements.

The effectiveness with which the receiver maintains the SNR of the incoming signal within the receive channel bandwidth will be the most important determinant of the modem's raw data rate. The SNR of the receive signal over the signal bandwidth, determined by the channel, puts a fundamental limit on the amount of data the channel will carry. Any degradation beyond this in the circuitry between the line interface and the digital output samples is considered implementation noise and is determined by the quality of the receiver. It is the receiver's job to eliminate out-of-band channel noise and compensate for signal attenuation, then digitize the analog signal for further digital signal processing.

The out-of-band noise and interference on the line reduce the receiver SNR in two ways. First, the noise present may be folded back into the signal band of interest by the sampling process, raising the existing noise floor. Second, if the noise and interference are orders of magnitude greater than the desired signal, this will reduce the gain that can be applied to the signal to compensate for signal attenuation—again resulting in lower SNR. Effective filtering is essential to reduce these effects. In order to optimize noise and distortion performance, a variable-gain amplifier is implemented on-chip. This function is shared by a continuous-time programmable gain stage (CPGA in Figure 3) and a discrete-time switched programmable gain stage (SPGA), sandwiching the LPF. Following the SPGA, a 12-/10-bit ADC digitizes the signal with sampling rates up to 50 MHz.

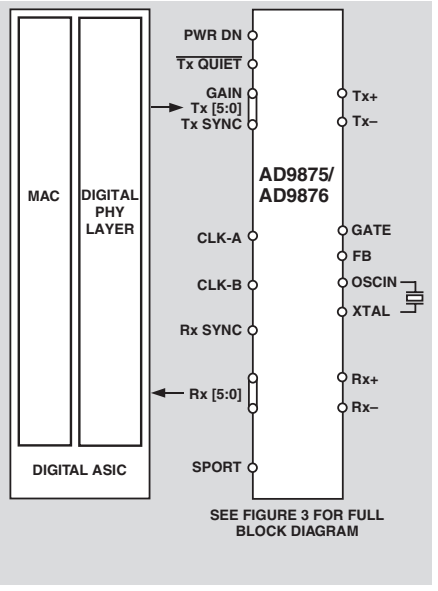
Several auxiliary function are also present on-chip. Two phase-locked-loop (PLL) blocks, a voltage-regulator control circuit, and a serial-port interface help reduce external component count and optimize performance.

Phone-line networking

Figures 4 and 5a show the AD9875 in a phone-line networking application that is capable of data rates up to 32 Mbps using QAM modulation. The separation of mixed-signal and digital circuitry allows the digital ASIC to be implemented on the most cost effective geometry possible. Because the modulation coding is located in the digital ASIC, designers can maximize their 'value added' while they minimize time to market.

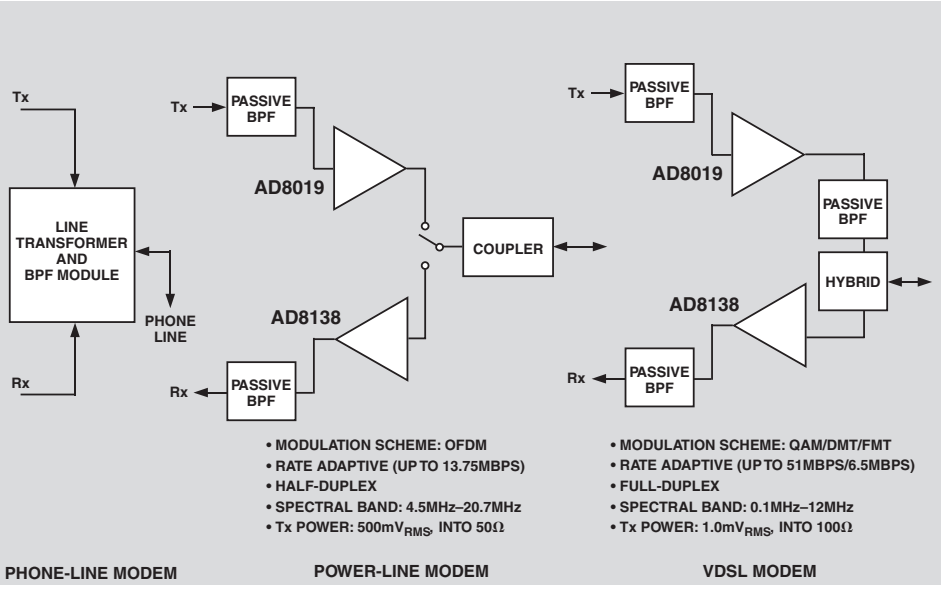
Power-line and VDSL modems

The AD9876 provides the optimum partitioning for a power-line or a VDSL modem, as illustrated in Figures 4 , 5b, and 5c. With its integrated programmable-gain amplifier, low-pass filter, and 12-bit ADC, in combination with 2×/4× interpolation filter and 12-bit TxDAC® D/A converter, the AD9876 provides nearly the entire analog portion of the signal chain-in a 48-lead LQFP package. By adding analog filters and line drivers, designers can bring a power-line or VDSL modem product to market quickly with an integrated single-chip solution. Compared with other, less-integrated, solutions in this type of application, component count can be reduced by as much as 50%; and the overall bill of materials can be reduced by more than the purchase price of the included integrated MxFE component. System costs can be reduced further by using the AD9875/AD9876's integrated 4× PLL clock multiplier and system clock outputs. They allow the entire system clock to be implemented with an inexpensive low-frequency crystal.



(a)

Figure 4. Mixed-signal and digital interface.



(b) (c)

Figure 5. Analog interfaces.

AD9875/AD9876 Key Features, Specifications, and Performance

- Low-cost 3.3V-CMOS mixed-signal front-end converter for broadband networking/modems
- 10-/12-bit 128-MSPS TxDAC+® D/A converter
- 64-/32-MSPS input word rate
- *2×/4× interpolation transmit LPF or BPF transmit*
- Flexible power-down modes
- 10-/12-bit, 50-MSPS ADC
- 4th-order low-pass filter 12- or 26-MHz with bypass
- –6-dB to 36-dB programmable-gain amplifier
- *Internal 4× clock multiplier (PLL) clock outputs*
- Voltage regulator controller
- 48-lead LQFP package

AD9875/AD9876 performance was characterized over the –40° to +85°C extended industrial temperature range.

The following two graphs (Figures 6 and 7) show the transmit-path performance in multi-tone applications of these parts and illustrate their exceptional linearity. Figure 6 shows intermodulation distortion of the AD9876; under the indicated conditions, it is less than –80 dB. Figure 7 shows the multi-tone power ratio of the transmit path: about 55 dB when transmitting 70 tones in the 4.5-MHz to 20.7-MHz frequency range, corresponding to the HomePlug frequency band.

The AD9876 12-bit ADC's performance meets the requirements for two-band VDSL and has been designed into system solutions for that application and for power line access modems. Figure 8 is a plot of THD as a function of ADC sampling rate for a 5-MHz sinusoidal input.

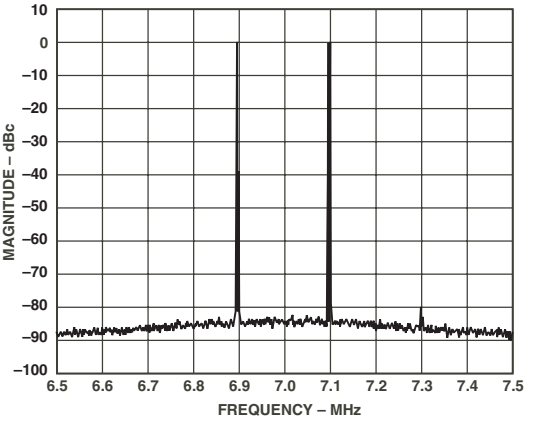


Figure 6. Dual-tone spectral plot of AD9876's 12-bit DAC @ f_{DATA} = 50 MSPS, f_{OUT} = 6.9 MHz, and 7.1 MHz.

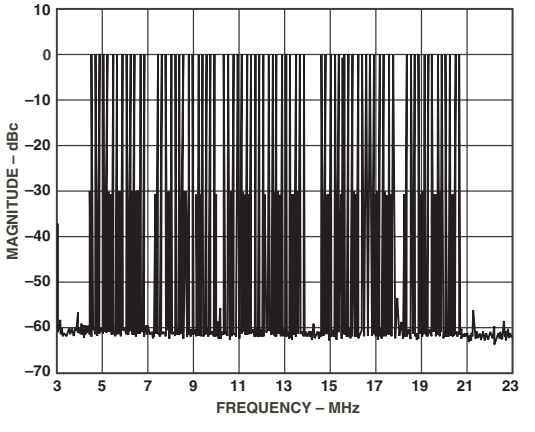


Figure 7. "In-band" multi-tone spectral plot of AD9876's 12-bit DAC @ f_{DATA} = 50 MSPS, f_{OUT} = k× 195 kHz, 2× LPF.

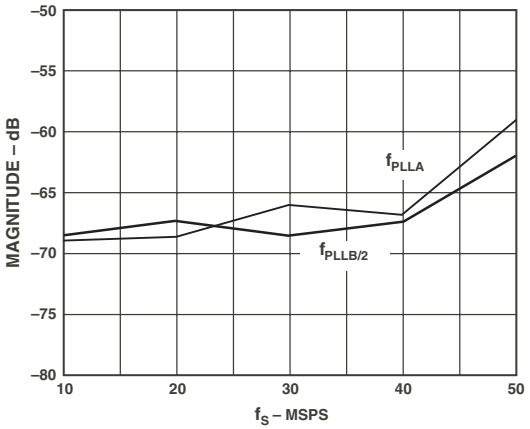


Figure 8. AD9876 12-bit ADC THD performance vs. f_{ADC} @ f_{IN} = 5 MHz.

The Rx LPF of the MxFE device has two frequency settings, one with a center frequency of about 10.8 MHz, the other at about 26 MHz. The filter transfer function is similar to that of a fourth-order Butterworth. The filters have a self-tuning feature that corrects for variation in device elements from part to part and for temperature drift. The center frequency can be adjusted over a 20% range if different cutoff frequencies are desired. Figure 9 shows LPF performance with the lower cutoff frequency selected.

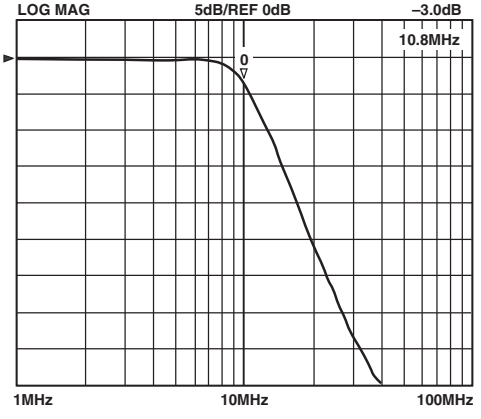


Figure 9. AD9876 Rx LPF frequency response, low f_C.

Evaluation Board and Software

The AD9875/AD9876 evaluation board (Figure 10), with its software, allows users to easily program and quickly evaluate the device for a specific modem application. The evaluation board provides connector access to the device's digital transmit and receive ports—which are buffered for reliable data transmission. The on-chip configuration registers can be programmed through the use of a PC serial port, which connects directly to a connector on the evaluation board; and the PC-resident evaluation-board software provides for a simple means of configuring the MxFE operation.

The analog output from the DAC, and the analog input to the ADC circuitry can be accessed through SMA connectors or pin headers on the evaluation board. The jumper-programmable interface configurations allow several different circuit options, to suit different testing methods. An on-board digital loopback feature allows the ADC and DAC to be tested simultaneously with the use of a signal source and spectrum analyzer. Also available is a daughter card, which can provide a phone-line compatible interface to the MxFE device.

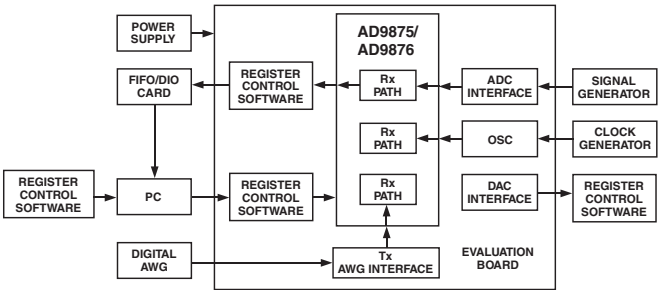


Figure 10. AD9875/AD9876 evaluation setup.

The AD9875-EB software provides a graphical user interface for easy programming and querying of the AD9875 registers. Three programming windows are available. The direct-register-access window allows AD9875 write- and readback in decimal, binary or hexadecimal data formats. The register-map window provides easy, function-oriented programming of the AD9875 registers. This window displays graphically all of the MxFE™ functions on the screen. The advanced-register-access window allows programming of sequences of register accesses.

Availability

The AD9875 and AD9876 were released to production in summer 2001. They are available in an economical, space-saving 48-lead LQFP and are priced at $9.24 and $14.45 (1000s), respectively. The AD9875 is priced at less than $5.00 (AD9876 <$7.00) in high volumes.

APPENDIX

These members of the Analog Devices MxFE family, the AD9875/AD9876, support *smart partitioning*, a mixed-signal design technique that partitions the signal path along lines that optimize system performance, rather than at analog/digital boundaries. This methodology complements the digital PHY (physical layer) and MAC (media access controller), which consist of several hundred thousand to well over a million gates fabricated on state-of-the-art 0.18-µm or finer geometry CMOS processes to take full advantage of the speed, power, and cost advantages that those processes offer. Meanwhile, at the heart of the AD9875/AD9876 are high-performance data-converter cores, fabricated on a well-established and cost-effective 0.35-µm CMOS process. To these cores are added both analog and digital signal-processing circuitry, to provide the necessary interfacing to both worlds, thus reducing complexity and cost of circuitry on the system board, without reducing flexibility. This combination of mixed-signal and digital functions provides overall system benefits by reducing component count and footprint without compromising performance.

Besides its performance and cost advantages, "smart partitioning" provides a logical place for the division of labor in developing complete physical-layer solutions. Companies whose core competencies are in the development of communications systems and algorithms can concentrate on those aspects of the digital design and capitalize on their differentiating technology. They can rest assured that their combined analog and mixed-signal solution is at the state of the art by partnering with a leader in the field, such as Analog Devices.